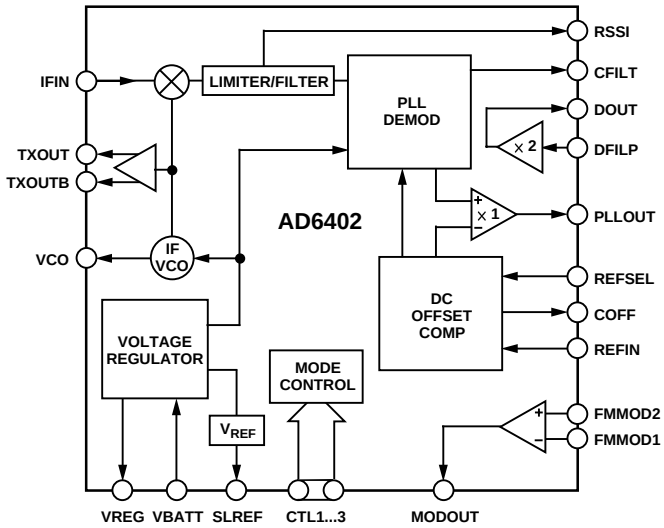
IF Transceiver Subsystem

AD6402

FEATURES
On-Chip Regulator
PLL Demodulator
On-Chip VCO
No Trims
Excellent Sensitivity
28-Lead SSOP Package

APPLICATIONS
DECT/PWT/WLAN
TDMA FM/FSK Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD6402 is a complete transceiver subsystem for use in high bit rate radio systems employing FM or FSK modulation. It is optimized for use in time domain multiple access (TDMA) systems with communications rates of approximately 1 MBPS. The AD6402 integrates key functions, including VCOs and a low drop-out voltage regulator. The AD6402 operates directly from an unregulated battery supply of 3.1 V to 4.5 V and provides a regulated voltage output which can be used for VCO supply regulation on a companion RF chip such as the AD6401.

The AD6402 transceiver consists of a mixer, integrated IF bandpass filter, IF limiter with RSSI detection, VCO, PLL demodulator and a low dropout voltage regulator. On receive, it downconverts an IF signal in the 110 MHz range to a second IF frequency, this frequency being determined by the demodulator reference divide ratios. It then filters, amplifies, and demodulates this signal. The AD6402 provides a filtered baseband data output. On transmit, it accepts a Gaussian Frequency Shift Keying (GFSK) baseband signal, low-pass filters the signal if required using the on-chip op amp and modulates the IF VCO by varying the bias voltage on an off-chip varactor diode used in the tank circuit.

The AD6402 has multiple power-down modes to maximize battery life. It operates over a temperature range of –25°C to +85°C and is packaged in a JEDEC standard 28-lead small-shrink outline (SSOP) surface-mount package.

REV. 0

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AD6402–SPECIFICATIONS

Parameter	Conditions	AD6402ARS Min	Typ	Max	Units
IF BANDPASS FILTER					
Center Frequency Rejection	REFIN = 13.824 MHz, REFSEL <0.2 V_{CC}		20.736		MHz
	F_O ±3.0 MHz		7		dBc
	F_O ±4.7 MHz		13		dBc
	F_O ±6.0 MHz		16		dBc
Stop Band Rejection			30		dBc
RECEIVER					
Sensitivity	FM Modulated 576 kHz, FM Deviation 288 kHz BT = 0.5, Demod Output SNR = 10 dB, R_S = 150 Ω		–80		dBm
RSSI					
Low	V_{OUT} = 0.2 V, R_S = 150 Ω		–85		dBm
High	V_{OUT} = 1.8 V, R_S = 150 Ω		–5		dBm
Slope	See Figure 4		20		mV/dB
Output Impedance			4		kΩ
DEMODULATOR					
Gain	At Data Filter Output	1.2		1.55	V/MHz
Offset	Referred to SLREF	–200		+200	mV
Lock Time	From SLEEP Mode		200		µs
	From RXLOCK Mode		20		µs
DATA FILTER OP AMP					
Gain			2		
Slew Rate	C_{LOAD} = 30 pF		8		V/µs
Gain Bandwidth	C_{LOAD} = 30 pF		15		MHz
Output Swing Low			0.2		V
Output Swing High			V_{CC}–0.2		V
Output Impedance			50		Ω
IF VCO					
Frequency	Note 1		131		MHz
SSB Phase Noise	@ 5 MHz Offset		–139		dBc/Hz
Output Power	Differential R_{LOAD} = 300 Ω		–12		dBm
2nd Harmonic			–22		dB
3rd Harmonic			–24		dB
TRANSMIT FILTER OP AMP					
Open Loop Gain			75		dB
Unity Gain Bandwidth	C_{LOAD} = 30 pF		12		MHz
Output Slew Rate	C_{LOAD} = 30 pF		5		V/µs
Minimum Input Voltage			1		V
Maximum Input Voltage			V_{CC}–0.2		V
Minimum Output Voltage			0.2		V
Maximum Output Voltage			V_{CC}–0.2		V
POWER CONTROL					
Logical High Threshold			0.8 × V_{CC}		V
Logical Low Threshold			0.2 × V_{CC}		V
Turn-On Response Time	V_{CC} Steady State		0.5		µs
VOLTAGE REFERENCE					
SLREF		1.3		1.5	V
SUPPLY REGULATOR					
Output Voltage	For Battery Voltages from 3.1 V to 4.5 V	2.75		2.95	V
Turn-On Time	1 mV Settling, C_{LOAD} = 100 nF		200		µs
Line Regulation	200 mV Battery Step; 5 mV Settling		1		µs
Load Regulation	10 µA to 30 mA Step; 5 mV Settling		200		µs
POWER SUPPLY	All V_{CC} at 2.85 V				
Supply Current	RXLOCKP		30		mA
	RXLOCK		17		mA
	RXDEMOD		26		mA
	TRANSMIT		6		mA
	STANDBY		300		µA
	SLEEP		10		µA

NOTES

[1]Using test tank circuit as shown.

Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

VBAT . . . . . 3.1 V–4.5 V
IFVCC1, IFVCC2, PLLVCC . . . . . .2.85 V
Operating Temperature Range . . . . . –25°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . +5.5 V
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering (60 sec) . . . . . .+300°C

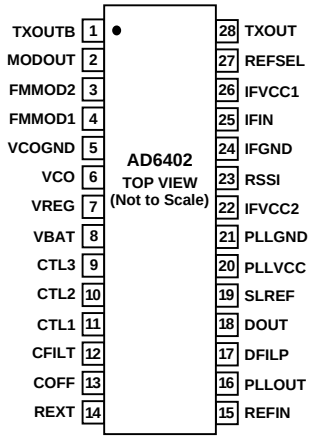
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

Thermal Characteristics:
28-lead SSOP package: θ_{JA} = 109°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD6402ARS	–25°C to +85°C	28-Lead SSOP
AD6402ARS-REEL	–25°C to +85°C	28-Lead SSOP

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	TXOUTB	Transmit IF VCO Buffer Inverting Output
2	MODOUT	Frequency Modulator Filter Op Amp Output
3	FMMOD2	Frequency Modulator Filter Op Amp Noninverting input
4	FMMOD1	Frequency Modulator Filter Op Amp Inverting input
5	VCOGND	IF VCO Ground
6	VCO	IF VCO Tank Connection
7	VREG	Regulated Supply Output for RF VCO (Supplies Internal IF VCO, Mode Control, Bandgap Reference, and COFF Buffer)
8	VBAT	Battery Supply Voltage Input to Internal Regulator and COFF Charge Pump
9	CTL3	Mode Control Input 3, CMOS Logical Level
10	CTL2	Mode Control Input 2, CMOS Logical Level
11	CTL1	Mode Control Input 1, CMOS Logical Level
12	CFILT	PLL Demodulator Loop Filter Capacitor
13	COFF	PLL Demodulator Frequency Offset Voltage Track/Hold Capacitor
14	REXT	External Current-Setting Resistor
15	REFIN	Baseband Reference Frequency Input, 100 mV p-p, AC Coupled
16	PLLOUT	PLL Demodulator Output
17	DFILP	Data Filter Voltage-Follower Input
18	DOUT	Data Filter Voltage-Follower Output
19	SLREF	PLL Demodulator Output DC Reference Voltage
20	PLLVCC	PLL Demodulator and Data Filter Supply Input
21	PLLGND	PLL Demodulator and Data Filter Ground
22	IFVCC2	IF Limiter Supply Input 1
23	RSSI	RSSI Output
24	IFGND	IF Stage, Mixer, Band Pass Filter, IF VCO Buffer, Tx Op Amp, Mode Control, and Regulator Ground
25	IFIN	IF Mixer Input, Z_O = 150 Z
26	IFVCC1	IF Mixer, Limiter 1, IF Filter, IF VCO Buffer
27	REFSEL	Reference Frequency Select; IF = 1.5× or 2.5× Reference Frequency, CMOS Logical Level Input
28	TXOUT	Transmit IF VCO Buffer Output

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6402 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

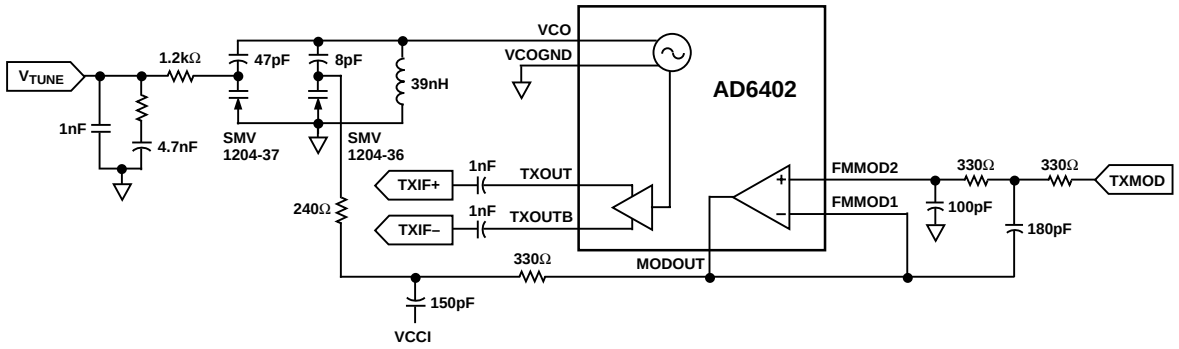


Figure 1.

OVERVIEW

The AD6402 forms the basis of a highly integrated RF transceiver with the benefits of increased sensitivity and wide dynamic range that a dual-conversion architecture provides. The IC contains a low dropout voltage regulator to isolate the IF and demodulator VCOs from variation in the battery voltage, such as power-supply transients caused by the PA. The AD6402 also provides control circuitry that allows subcircuits to be turned off and on as necessary to minimize power consumption.

Operation During Receive

The AD6402 contains the second mixer, integrated second-IF bandpass filter, logarithmic-limiting amplifier, and PLL demodulator. A SAW IF bandpass filter is usually required at the IF input in order to provide channel selectivity.

The placement of the SAW filter in the signal path between the AD6402 and the RF section and the partitioning of the receiver's RF and IF receive circuits minimizes the leakage around the SAW filter and maximizes the RF to IF isolation.

The output of the SAW filter enters the AD6402 via the second downconversion mixer. This mixer is a high gain, doubly-balanced Gilbert-cell type. The mixer downconverts the signal to the second IF, which is 1.5 × or 2.5 × the reference frequency. This multiple is determined by the state of the REFSEL pin. An on-chip two section bandpass filter provides additional selectivity to provide attenuation of adjacent channels. The VCO control voltage output of the PLL demodulator tunes this filter to the second IF.

The bandpass filter's output enters a successive-detection logarithmic-limiting IF amplifier. The RSSI detectors are distributed across the entire IF strip, including the mixer, and provide 80 dB RSSI range. The IF strip's limiting gain also exceeds 80 dB. The RSSI signal is low-pass filtered and proceeds off-chip to the baseband subsystem. The limited output of the logarithmic amplifier enters a PLL demodulator, which provides demodulation of the received signal. The PLL uses an integrated VCO with no external components.

Operation During Transmit

The transmit signal path consists of a low-pass filter that can be user configured for antialiasing of a baseband transmit signal. An IF VCO, which should be tuned to a frequency equal to the receive IF frequency plus the desired demodulator input frequency, may be open-loop modulated by the transmit signal for FM and FSK schemes. The receive IF mixer uses high side mixing and therefore the IF VCO should be set to a frequency equal to the sum of the IF frequency plus the frequency of the PLL demodulator input as defined by the reference clock divider ratios.

The transmit IF VCO uses an external tank circuit. This signal is upconverted to the transmit frequency in the RF mixer section of the radio. Using a transmit IF VCO prevents two problems: feedback from the PA at the RF frequency does not cause distortion in the modulating circuit because the frequencies are widely separated and the IF tank circuit can be optimized for modulation linearity.

The output of the transmit VCO passes through buffer amplifier and leaves the AD6402 via an optional LC filter between the RF and IF ICs. The output of the LC filter may then be fed to a transmit upconversion mixer for conversion to the final RF frequency.

Onboard Voltage Regulation

The AD6402 contains a low dropout voltage regulator to specifically isolate the VCOs and synthesizer from the voltage "kick" that occurs when a power amplifier switches on and the battery voltage abruptly drops. The AD6402 uses an integral vertical PNP pass transistor.

The regulator in the AD6402 IF IC supplies the voltage for the VCOs on both the RF section and AD6402. The other sections of the AD6402 should be powered from an independently regulated source at 2.85 V. Since the VCOs are isolated from this source, possible problems due to VCO supply pushing are considerably reduced.

Frequency Control

The AD6402 requires an external synthesizer to provide the control voltages for the tank circuit of the IF VCO. Normally this will be the IF section of a dual synthesizer controlling both IF and RF frequency generation.

It is recommended that the VCO on the RF section implement the channel selection on transmit and receive; the VCO on the AD6402 may therefore operate at a fixed frequency. This accomplishes two goals: first, the IF VCO being modulated can be optimized for modulation linearity and the RF VCO can be optimized for tuning range, and second, feedback from the PA at will not couple into the modulating circuit to cause spurious responses.

All key sections of the AD6402 may be powered up or down as necessary to minimize power consumption and maximize battery life.

Table I. Power Management Functionality

TL1	CTL2	CTL3	PLL BIAS	PLL LOCK	PLL DMOD	REF	REG	RX	VCO	MODE
0	0	0	–	–	–	OFF	OFF	–	–	SLEEP
0	0	1	–	–	–	OFF	ON	–	–	STANDBY
0	1	0	ON	ON	OFF	ON	ON	OFF	ON	RXLOCK
1	X	0	ON	OFF	ON	ON	ON	ON	ON	RXDMOD
1	0	1	OFF	OFF	OFF	ON	ON	OFF	ON	TRANSMIT
1	1	1	ON	ON	OFF	ON	ON	ON	ON	RXLOCKP

The AD6402 has six operating modes: SLEEP, STANDBY, RXLOCK, RXDMOD, TRANSMIT and RXLOCKP. These are summarized in Table I. The blocks referred to in Table I are shown also in Figure 4. These modes are described as follows:

SLEEP: The entire device is shut down.

STANDBY: All functions except the regulator are shut down.

RXLOCK: The device locks to a local reference clock using the lock PLL. The lock charge pump and dividers are powered up. The VCO is also powered up.

RXDMOD: In this mode the lock charge pump and loop dividers are shut down. The receive mixer, IF strip, reference and demodulator are powered up.

TRANSMIT: This mode enables the VCO and transmit op amp. The reference and regulator are also enabled.

RXLOCKP: This mode may be used in a “prior to” timeslot, i.e., the slot before the actual active receive timeslot. In this mode, after lock has been achieved in the RXLOCK mode, the receive mixer, VCO and IF strip may then be independently powered up from the demodulator loop. This can result is power savings, since the demodulator may be powered down during the IF VCO lock acquisition time.

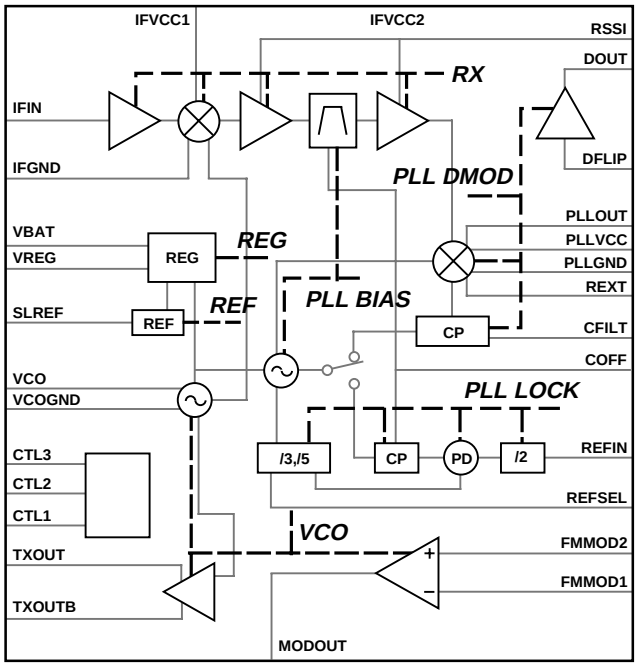


Figure 2. Power Management Scheme

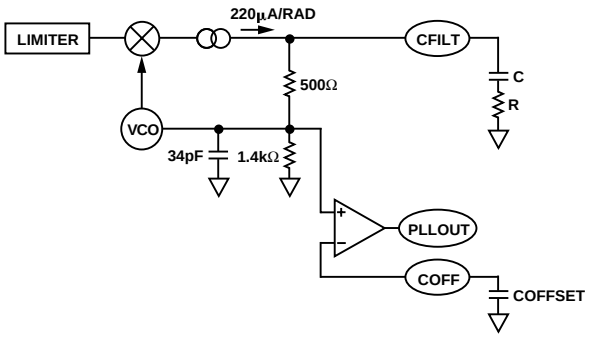


Figure 3a. Demodulator Block Diagram (Lock Mode)

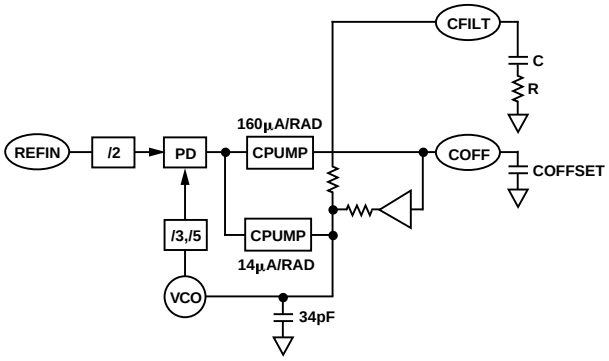


Figure 3b. Demodulator Block Diagram (Dmod Mode)

Demodulator Operation

The PLL itself uses two loops: one for rapid frequency acquisition and a second for demodulation. The first, or frequency-acquisition loop, locks the VCO to a noninteger multiple of the system clock, either 3/2 or 5/2 (using one fixed /2 and one programmable /3 or /5 divider). This allows not only a choice of IF and system clocks but also prevents blocking of the receiver by keeping integer multiples of the system clock out of the IF passband.

Once locked, this loop voltage is stored on an external capacitor and this sets the free-running frequency of the VCO during demodulation. The first loop is opened and, using the second loop and phase detector, the PLL compares the free-running frequency of its VCO to the frequency of the incoming IF. The VCO is then fast frequency locked, and slow phase locked to the incoming IF. Preconditioning of the PLL to the local reference clock facilitates the fast frequency lock to the received IF. The PLL now generates a baseband voltage proportional to the frequency deviation of the received signal.

The demodulator uses a third-order PLL to track the incoming modulation signal. A simplified diagram of the demodulator is shown in Figures 3a and 3b. The loop bandwidth and damping factor can be adjusted by changing the values of C and R as indicated. An internal pole is present on the demodulator loop at approximately 9 MHz. For a loop ω_n of 800 kHz, values of 910 pF and 330 Ω respectively are optimum. The loop bandwidth will approximately scale inversely as the square root of the value of C. To preserve a satisfactory damping factor, R should be adjusted linearly with the loop bandwidth. At low loop bandwidths however the value of C offset must also be increased to enable the loop to lock to the reference frequency during prior to receive time slots.

APPLICATIONS

The AD6402 is optimized for use in applications where a data rate of the order of 1 megabit per second is required and the modulation scheme employed is constant envelope, i.e., FM or FSK. Because the demodulator uses a track and hold technique that locks to an externally supplied reference clock, the device is optimized for use in TDMA systems. If used in continuous demodulation applications, the dc offset hold voltage on the demodulator differential amplifier will ultimately leak away, resulting in the average dc value of the demodulator output eventually limiting against the supply rail. In a TDMA system, the voltage on the capacitor is refreshed just before the active timeslot, thereby enabling a very accurate dc offset compensation of system frequency errors.

The on-chip IF filter has been designed to provide some rejection of adjacent channel signals for channel bandwidths in the 1 MHz–2 MHz range. This filter has the benefit of reducing the contribution of broadband noise through the IF strip, hence improving the overall sensitivity of the receiver for a given demodulator output signal to noise ratio.

It is also possible to use the AD6402 in applications where non-constant envelope modulation schemes are used, such as QPSK. In these applications the amplitude information will be lost through the limiting action of the IF strip, but in certain applications, sufficient eye-opening will be observed in the demodulated signal to allow the use of hard decision bit-slicers as in the FM or FSK case. The actual performance of the subsystem in the presence of a QPSK signal will depend on factors such as bit rate, modulation index and BT employed.

Figure 4 shows the RSSI response to a DECT signal at the IF port. It can be seen from the plot that the AD6402 can detect signals below –85 dBm and continues to detect linearly up to and above –5 dBm.

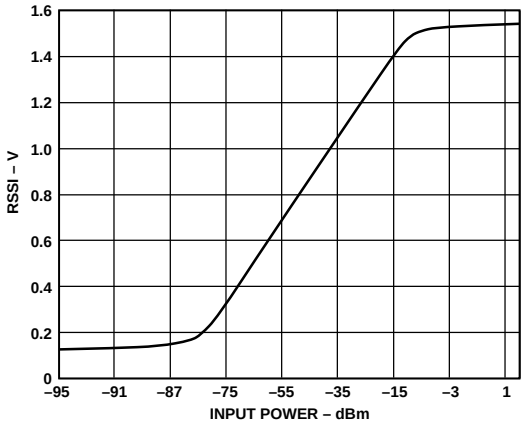


Figure 4. RSSI Response

Figure 5 shows an implementation for a DECT IF subsystem. DECT is a 1.152 megabit/second radio, employing Gaussian FSK modulation at a BT = 0.5 and uses a channel spacing of 1.728 MHz. It is a TDMA/TDD system. The IF frequency used in this application is 110.592 MHz. The AD6402's flexible power management scheme enables the part to operate at low

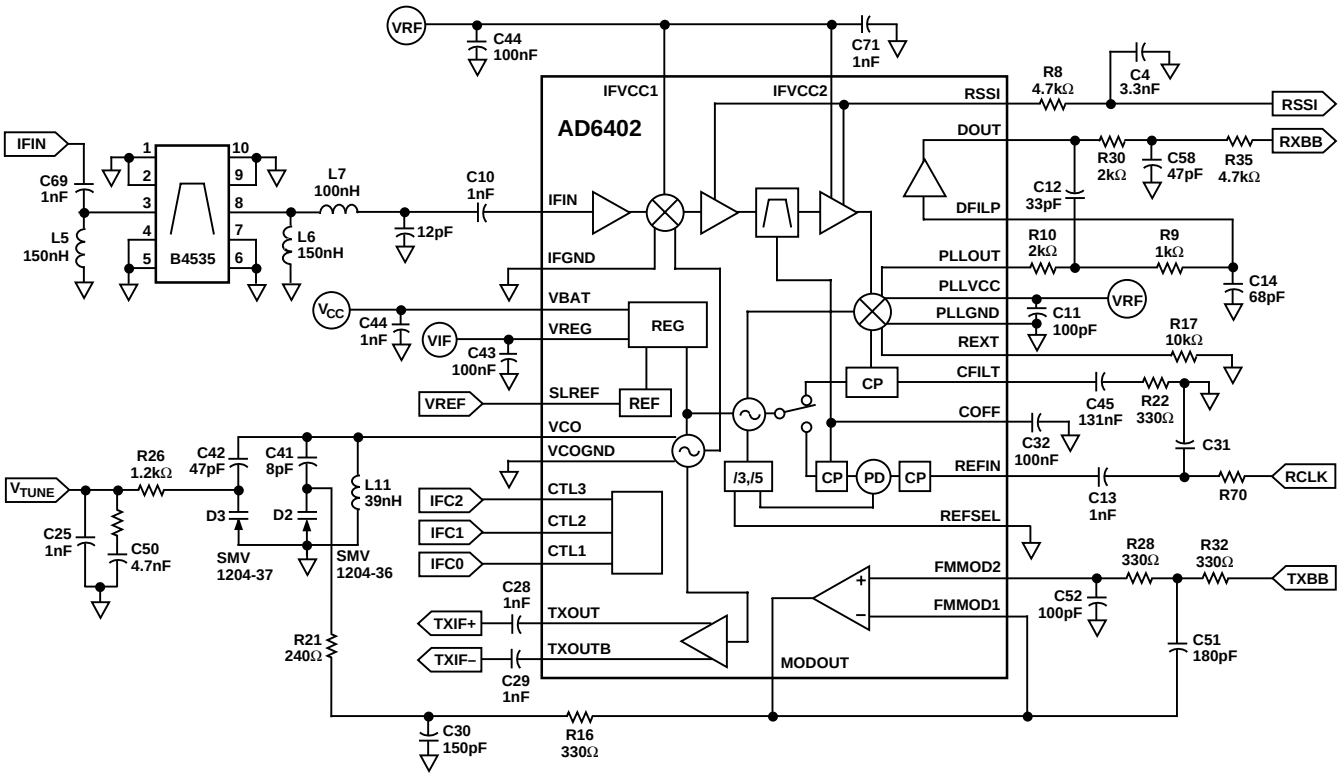


Figure 5. Application Circuit for DECT GFSK Transceiver

supply current levels when not allocated to an active transmit or receive timeslot in a TDMA system.. The respective transmit and receive blocks can be turned on only as needed thereby reducing power consumption and extending battery life of handheld terminals.

The component selection in Figure 5 is explained as follows: The IF input is driven from the output of a SAW filter via an impedance matching circuit as shown. This matching minimizes the insertion loss of the filter and follows the filter manufacturers recommendations. The tank circuit shown uses two varactor diodes. One diode (D3) is biased by the output of the IF PLL loop filter and ensures that the IF VCO frequency is correctly centered. The second diode is provided to enable a modulation signal, which is generated at the output of the on-chip op amp (MODOUT), to be coupled into the VCO tank and thereby implement a modulation of the VCO frequency. In the case of DECT, the IF VCO control loop is opened while the VCO is being modulated by the transmit bit stream. The loop is opened by tri-stating the output of the IF VCO PLL charge pump.

The exact component values used around the modulation amplifier will be determined by the amount of attenuation required for suppression of baseband transmit spurii and images. These artifacts are usually present if the baseband FSK signal is generated by a ROMDAC. In most instances a second or third order Bessel or Butterworth filter will be required.

A capacitor to ground is required to be connected to COFF. This capacitor stores the demodulator charge-pump voltage required to lock the demodulator VCO to the reference frequency. The dynamic response of the demodulator loop is controlled by selection of the values for C45 and R22 which are connected in series to CFILT. These components determine the transfer characteristic of the loop filter and hence the lock time, settling time and bandwidth of the loop. REXT should use the recommended value as shown.

Finally, the demodulator is followed by a voltage follower, which is configured as a data filter. This data filter is used to bandlimit the FM noise generated in the demodulator. It also attenuates undesired adjacent channel interferers. The component values chosen will be a trade-off between the amount of band limiting required and attenuation of the in-band desired signal.

DECT Application Circuit Notes (Figure 5)

1. Signal Description
   VRF: Regulated Supply Voltage; Nominal Value 2.85 V.

   V_{CC}: Unregulated battery voltage; 3.1 V–4.5 V

   VTUNE: Synthesizer Control Voltage; Range dependent on loop filter and synth charge pump compliance.

   TXBB: Baseband transmit modulation voltage; typically SLREF ±0.7 V

   RCLK: Reference clock for PLL demodulator; 13.824 MHz

   (2nd IF frequency = (N/M) × Frclk where N = 3 or 5, and M = 2. Maximum 2nd IF = c.26 MHz)
2. Typical IF input sensitivity referred to the input of SAW filter for the above application will be –72 dBm.
3. TxBB filter is user configurable. In the above application, the filter is implemented to remove images generated by ROM DAC baseband signal generators. Other implementations are possible including passive pulse shaping circuits which eliminate the need for such filtering.

EVALUATION BOARD

An evaluation board is available for the AD6402. This board facilitates test and measurement of the subsystem. Parameters such as sensitivity, ACI, CCI, demodulator gain, demodulator offset, etc., can be quickly evaluated using this board. Contact your local ADI sales office or ADI representative for further details on pricing and availability of the evaluation boards.

Header connections details are shown in Figure 6 and available signals are shown in Figure 7. A schematic for the evaluation board is shown in Figure 8.

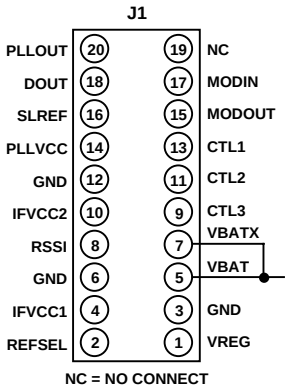


Figure 6. Evaluation Board Header

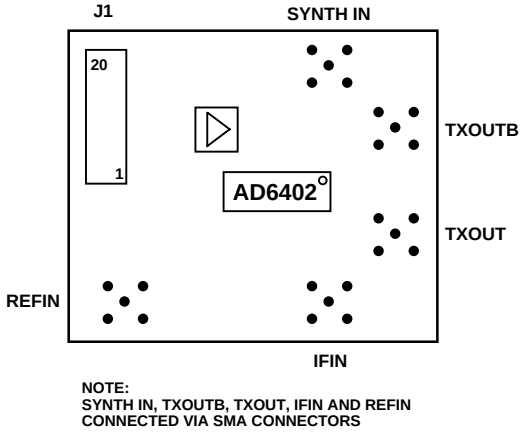


Figure 7. Evaluation Board Connectors

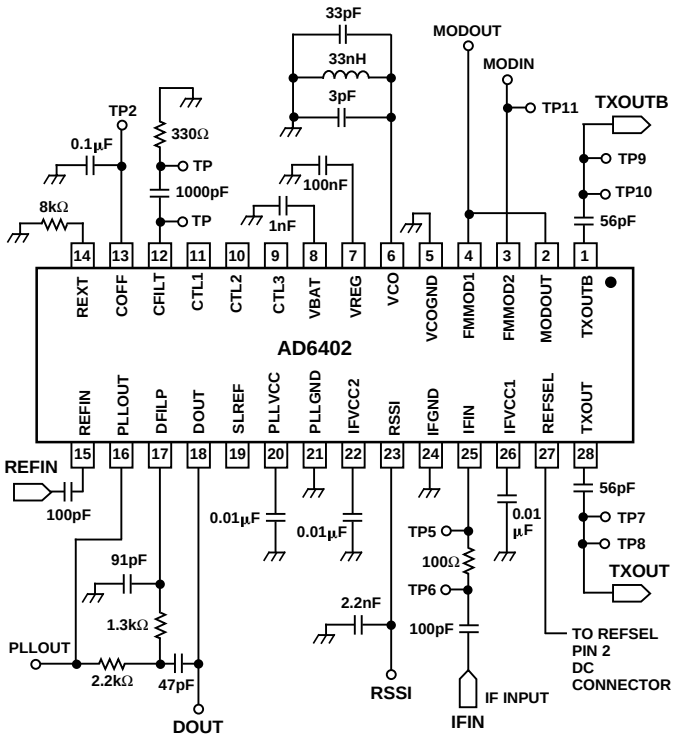


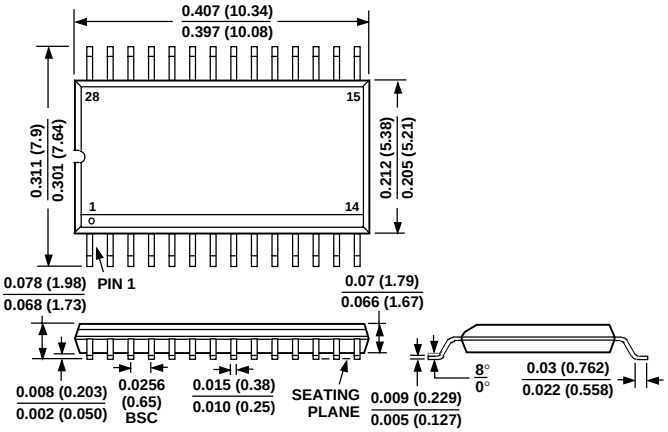
Figure 8. Evaluation Board Schematic

C3155–12–7/97

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Small Shrink Outline Package (RS-28)



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