

**10-Bit, 12-Bit, Multiplying D/A Converters**

The AD7520 and AD7521 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Intersil's thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

**Features**

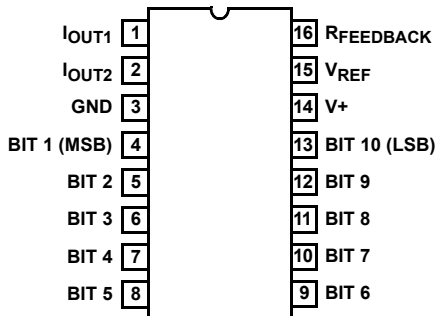
- AD7520, 10-Bit Resolution; 8-Bit Linearity
- AD7521, 12-Bit Resolution; 10-Bit Linearity
- Low Power Dissipation (Max) . . . . . 20mW
- Low Nonlinearity Tempco at 2ppm of FSR/°C
- Current Settling Time to 0.05% of FSR . . . . . 1.0μs
- Supply Voltage Range . . . . . ±5V to +15V
- TTL/CMOS Compatible
- Full Input Static Protection

**Ordering Information**

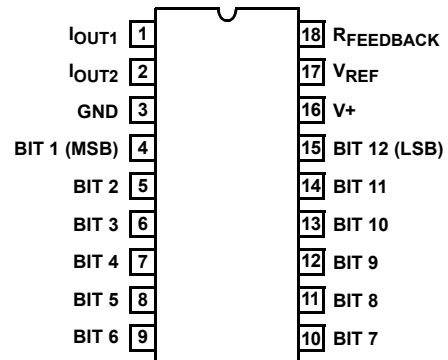
PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7520JN	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7521LN	0.05% (10-Bit)	0 to 70	18 Ld PDIP	E18.3

**Pinouts**

**AD7520 (PDIP)**  
TOP VIEW



**AD7521 (PDIP)**  
TOP VIEW



# AD7520, AD7521

## Absolute Maximum Ratings

Supply Voltage (V+ to GND) .....	+17V
V <sub>REF</sub> .....	±25V
Digital Input Voltage Range .....	V+ to GND
Output Voltage Compliance .....	-100mV to V+

## Operating Conditions

Temperature Ranges	
JN, LN Versions .....	0°C to 70°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.*

*Do not apply voltages higher than V<sub>DD</sub> or less than GND potential on any terminal except V<sub>REF</sub> and R<sub>FEEDBACK</sub>.*

1.  $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 Ld PDIP Package	90	N/A
18 Ld PDIP Package	80	N/A
Maximum Junction Temperature (Plastic Packages) .....	150°C	
Maximum Storage Temperature Range .....	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s) .....	300°C	

## Electrical Specifications V+ = +15V, V<sub>REF</sub> = +10V, T<sub>A</sub> = 25°C Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	AD7520			AD7521			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SYSTEM PERFORMANCE</b> (Note 2)									
Resolution			10	10	10	12	12	12	Bits
Nonlinearity	J	(Note 3) (Figure 2) -10V ≤ V <sub>REF</sub> ≤ +10V	-	-	±0.2 (8-Bit)	-	-	-	% of FSR
	L	-10V ≤ V <sub>REF</sub> ≤ +10V (Figure 2)	-	-	±0.05 (10-Bit)	-	-	±0.05 (10-Bit)	% of FSR
Nonlinearity Tempco		-10V ≤ V <sub>REF</sub> ≤ +10V (Notes 3, 4)	-	-	±2	-	-	±2	ppm of FSR/°C
Gain Error			-	±0.3	-	-	±0.3	-	% of FSR
Gain Error Tempco			-	-	±10	-	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)		Over the Specified Temperature Range	-	-	±200	-	-	±200	nA
<b>DYNAMIC CHARACTERISTICS</b>									
Output Current Settling Time		To 0.05% of FSR (All Digital Inputs Low To High And High To Low) (Note 4) (Figure 7)	-	1.0	-	-	1.0	-	μs
Feedthrough Error		V <sub>REF</sub> = 20V <sub>P-P</sub> , 100kHz All Digital Inputs Low (Note 4) (Figure 6)	-	-	10	-	-	10	mV <sub>P-P</sub>
<b>REFERENCE INPUT</b>									
Input Resistance		All Digital Inputs High I <sub>OUT1</sub> at Ground	5	10	20	5	10	20	kΩ
<b>ANALOG OUTPUT</b>									
Output Capacitance	I <sub>OUT1</sub>	All Digital Inputs High (Note 4) (Figure 5)	-	200	-	-	200	-	pF
	I <sub>OUT2</sub>		-	75	-	-	75	-	pF
	I <sub>OUT1</sub>	All Digital Inputs Low (Note 4) (Figure 5)	-	75	-	-	75	-	pF
	I <sub>OUT2</sub>		-	200	-	-	200	-	pF
Output Noise		Both Outputs (Note 4) (Figure 4)	-	Equivalent to 10kΩ	-	-	Equivalent to 10kΩ	-	Johnson Noise
<b>DIGITAL INPUTS</b>									
Low State Threshold, V <sub>IL</sub>		Over the Specified Temperature Range V <sub>IN</sub> = 0V or +15V	-	-	0.8	-	-	0.8	V
High State Threshold, V <sub>IH</sub>			2.4	-	-	2.4	-	-	V
Input Current, I <sub>IL</sub> , I <sub>IH</sub>			-	-	±1	-	-	±1	μA
Input Coding		See Tables 1 and 2	Binary/Offset Binary						

# AD7520, AD7521

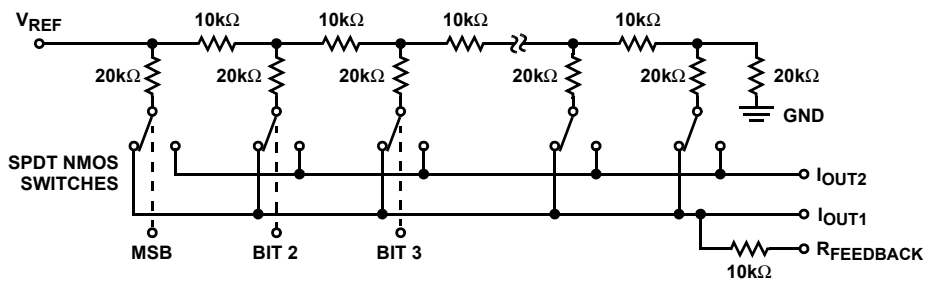
## Electrical Specifications $V_+ = +15V$ , $V_{REF} = +10V$ , $T_A = 25^\circ C$ Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	AD7520			AD7521			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>POWER SUPPLY CHARACTERISTICS</b>								
Power Supply Rejection	$V_+ = 14.5V$ to $15.5V$ (Note 3) (Figure 3)	-	$\pm 0.005$	-	-	$\pm 0.005$	-	% FSR/% $\Delta V_+$
Power Supply Voltage Range		+5 to +15			+5 to +15			V
$I_+$	All Digital Inputs at 0V or $V_+$ Excluding Ladder Network	-	$\pm 1$	-	-	$\pm 1$	-	$\mu A$
	All Digital Inputs High or Low Excluding Ladder Network	-	-	2	-	-	2	mA
Total Power Dissipation	Including the Ladder Network	-	20	-	-	20	-	mW

**NOTES:**

2. Full Scale Range (FSR) is 10V for Unipolar and  $\pm 10V$  for Bipolar modes.
3. Using internal feedback resistor  $R_{FEEDBACK}$ .
4. Guaranteed by design, or characterization and not production tested.
5. Accuracy not guaranteed unless outputs at GND potential.
6. Accuracy is tested and guaranteed at  $V_+ = 15V$  only.

## Functional Diagram



**NOTES:**

Switches shown for Digital Inputs "High".  
Resistor values are typical.

## Pin Descriptions

AD7520	AD7521	PIN NAME	DESCRIPTION
1	1	IOUT1	Current Out summing junction of the R2R ladder network.
2	2	IOUT2	Current Out virtual ground, return path for the R2R ladder network.
3	3	GND	Digital Ground. Ground potential for digital side of D/A.
4	4	Bits 1(MSB)	Most Significant Digital Data Bit.
5	5	Bit 2	Digital Bit 2.
6	6	Bit 3	Digital Bit 3.
7	7	Bit 4	Digital Bit 4.
8	8	Bit 5	Digital Bit 5.
9	9	Bit 6	Digital Bit 6.
10	10	Bit 7	Digital Bit 7.
11	11	Bit 8	Digital Bit 8.
12	12	Bit 9	Digital Bit 9.
13	13	Bit 10	Digital Bit 10 (AD7521). Least Significant Digital Data Bit (AD7520).
-	14	Bit 11	Digital Bit 11 (AD7521).
-	15	Bit 12	Least Significant Digital Data Bit (AD7521).
14	16	$V_+$	Power Supply +5V to +15V.
15	17	$V_{REF}$	Voltage Reference Input to set the output range. Supplies the R2R resistor ladder.
16	18	$R_{FEEDBACK}$	Feedback resistor used for the current to voltage conversion when using an external Op Amp.

**Definition of Terms**

**Nonlinearity:** Error contributed by deviation of the DAC transfer function from a “best straight line” through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

**Resolution:** It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of N bits can resolve output changes of  $2^{-N}$  of the full-scale range, e.g.,  $2^{-N} V_{REF}$  for a unipolar conversion. Resolution by no means implies linearity.

**Settling Time:** Time required for the output of a DAC to settle to within specified error band around its final value (e.g.,  $1/2$  LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

**Gain Error:** The difference between actual and ideal analog output values at full scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

**Feedthrough Error:** Error caused by capacitive coupling from  $V_{REF}$  to  $I_{OUT1}$  with all digital inputs LOW.

**Output Capacitance:** Capacitance from  $I_{OUT1}$  and  $I_{OUT2}$  terminals to ground.

**Output Leakage Current:** Current which appears on  $I_{OUT1}$  terminal when all digital inputs are LOW or on  $I_{OUT2}$  terminal when all digital inputs are HIGH.

**Detailed Description**

The AD7520 and AD7521 are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or

current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in the *Functional Diagram*. The NMOS SPDT switches steer the ladder leg currents between  $I_{OUT1}$  and  $I_{OUT2}$  buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduce offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with positive feedback from the output of the second to the first, see Figure 1. This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

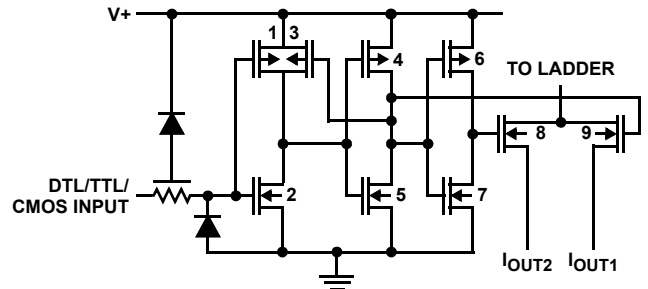


FIGURE 1. CMOS LEVEL SHIFTER AND SWITCH

**Test Circuits** The following test circuits apply for the AD7520. Similar circuits are used for the AD7521.

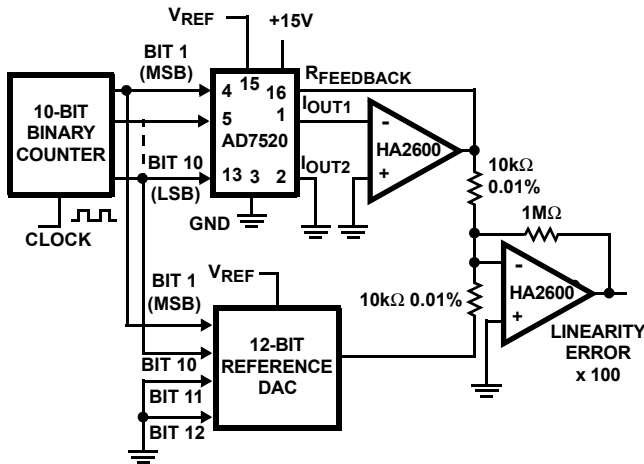


FIGURE 2. NONLINEARITY

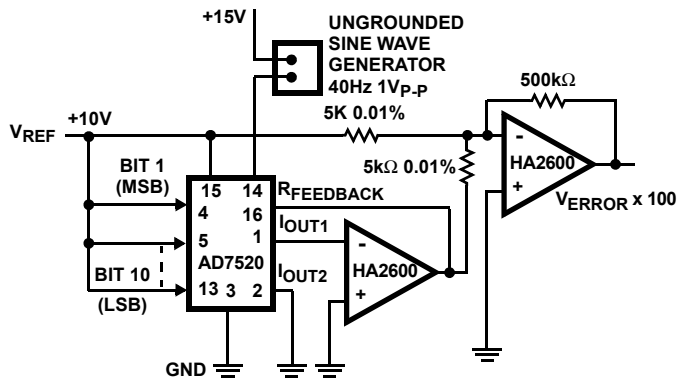


FIGURE 3. POWER SUPPLY REJECTION

**Test Circuits** The following test circuits apply for the AD7520. Similar circuits are used for the AD7521. (Continued)

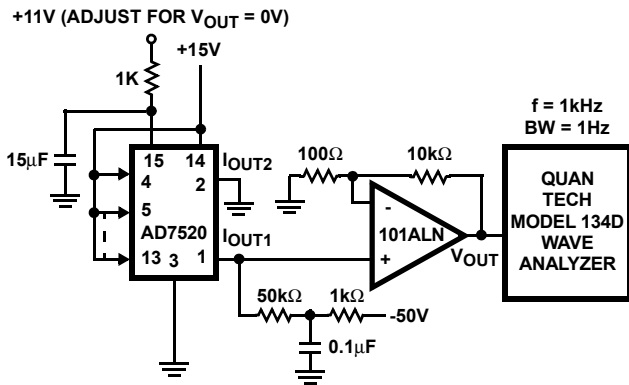


FIGURE 4. NOISE

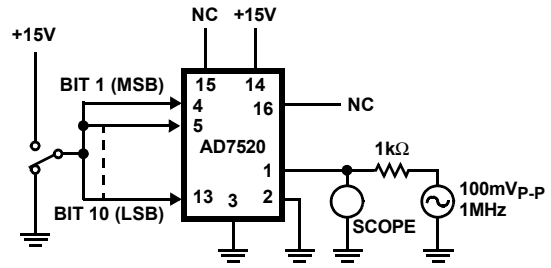


FIGURE 5. OUTPUT CAPACITANCE

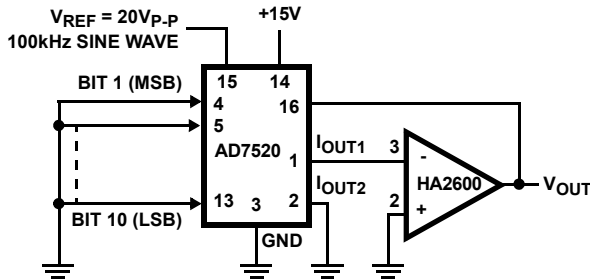


FIGURE 6. FEEDTHROUGH ERROR

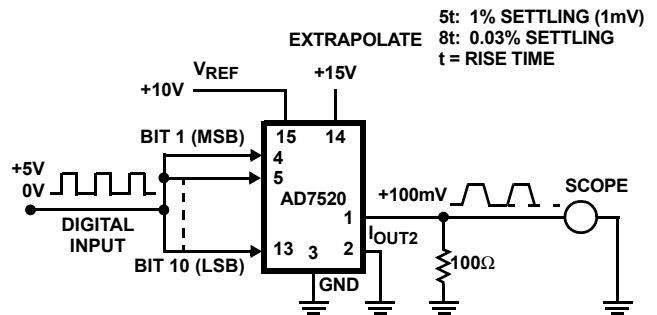


FIGURE 7. OUTPUT CURRENT SETTLING TIME

**Applications**

**Unipolar Binary Operation**

The circuit configuration for operating the AD7520 in unipolar mode is shown in Figure 8. Similar circuits can be used for AD7521. With positive and negative  $V_{REF}$  values the circuit is capable of 2-Quadrant multiplication. The *Digital Input Code/Analog Output Value* table for unipolar mode is given in Table 1.

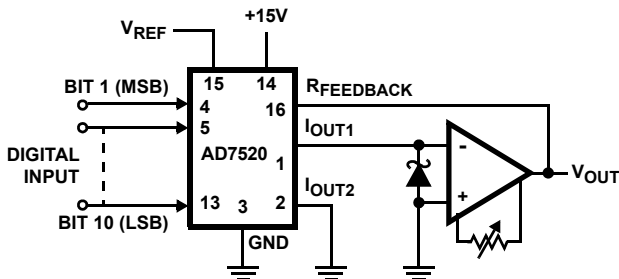


FIGURE 8. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

TABLE 1. CODE TABLE - UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF} (1-2^{-N})$
1000000001	$-V_{REF} (1/2 + 2^{-N})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF} (1/2-2^{-N})$
0000000001	$-V_{REF} (2^{-N})$
0000000000	0

NOTES:

1.  $LSB = 2^{-N} V_{REF}$ .
2.  $N = 8$  for 7520  
 $N = 10$  for 7521.

**Zero Offset Adjustment**

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V at  $V_{OUT}$ .

**Gain Adjustment**

1. Connect all digital inputs to  $V+$ .
2. Monitor  $V_{OUT}$  for a  $-V_{REF} (1-2^{-N})$  reading. ( $N = 8$  for AD7520 and  $N = 10$  for AD7521).

- To decrease  $V_{OUT}$ , connect a series resistor (0 to 250 $\Omega$ ) between the reference voltage and the  $V_{REF}$  terminal.
- To increase  $V_{OUT}$ , connect a series resistor (0 to 250 $\Omega$ ) in the  $I_{OUT1}$  amplifier feedback loop.

**Bipolar (Offset Binary) Operation**

The circuit configuration for operating the AD7520 in the bipolar mode is given in Figure 9. Similar circuits can be used for AD7521. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

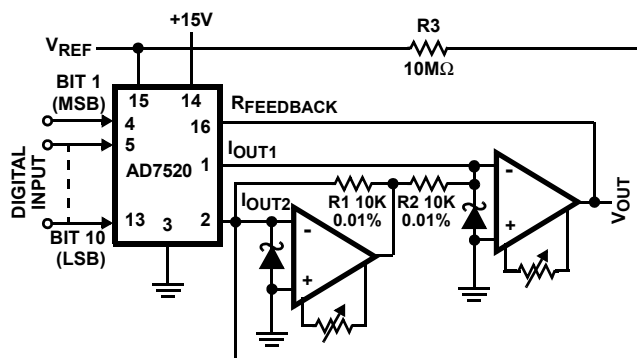


FIGURE 9. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

TABLE 2. BIPOLAR (OFFSET BINARY) CODE TABLE

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF} (1-2^{-(N-1)})$
1000000001	$-V_{REF} (2^{-(N-1)})$
1000000000	0
0111111111	$V_{REF} (2^{-(N-1)})$
0000000001	$V_{REF} (1-2^{-(N-1)})$
0000000000	$V_{REF}$

NOTES:

- LSB =  $2^{-(N-1)} V_{REF}$ .
- N = 8 for 7520  
N = 10 for 7521.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", all other bits = "Logic 0"), is corrected by using an external resistor, (10M $\Omega$ ), from VREF to IOUT2.

**Offset Adjustment**

- Adjust  $V_{REF}$  to approximately +10V.
- Connect all digital inputs to "Logic 1".
- Adjust  $I_{OUT2}$  amplifier offset adjust trimpot for  $0V \pm 1mV$  at  $I_{OUT2}$  amplifier output.
- Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
- Adjust  $I_{OUT1}$  amplifier offset adjust trimpot for  $0V \pm 1mV$  at  $V_{OUT}$ .

**Gain Adjustment**

- Connect all digital inputs to  $V+$ .
- Monitor  $V_{OUT}$  for a  $-V_{REF} (1-2^{-(N-1)})$  volts reading. (N = 8 for AD7520, and N = 10 for AD7521.)
- To increase  $V_{OUT}$ , connect a series resistor of up to 250 $\Omega$  between  $V_{OUT}$  and RFEEDBACK.
- To decrease  $V_{OUT}$ , connect a series resistor of up to 250 $\Omega$  between the reference voltage and the  $V_{REF}$  terminal.

**Die Characteristics**

**DIE DIMENSIONS:**

101 mils x 103 mils (2565µm x 2616µm)

**METALLIZATION:**

Type: Pure Aluminum  
 Thickness: 10 ±1kÅ

**PASSIVATION:**

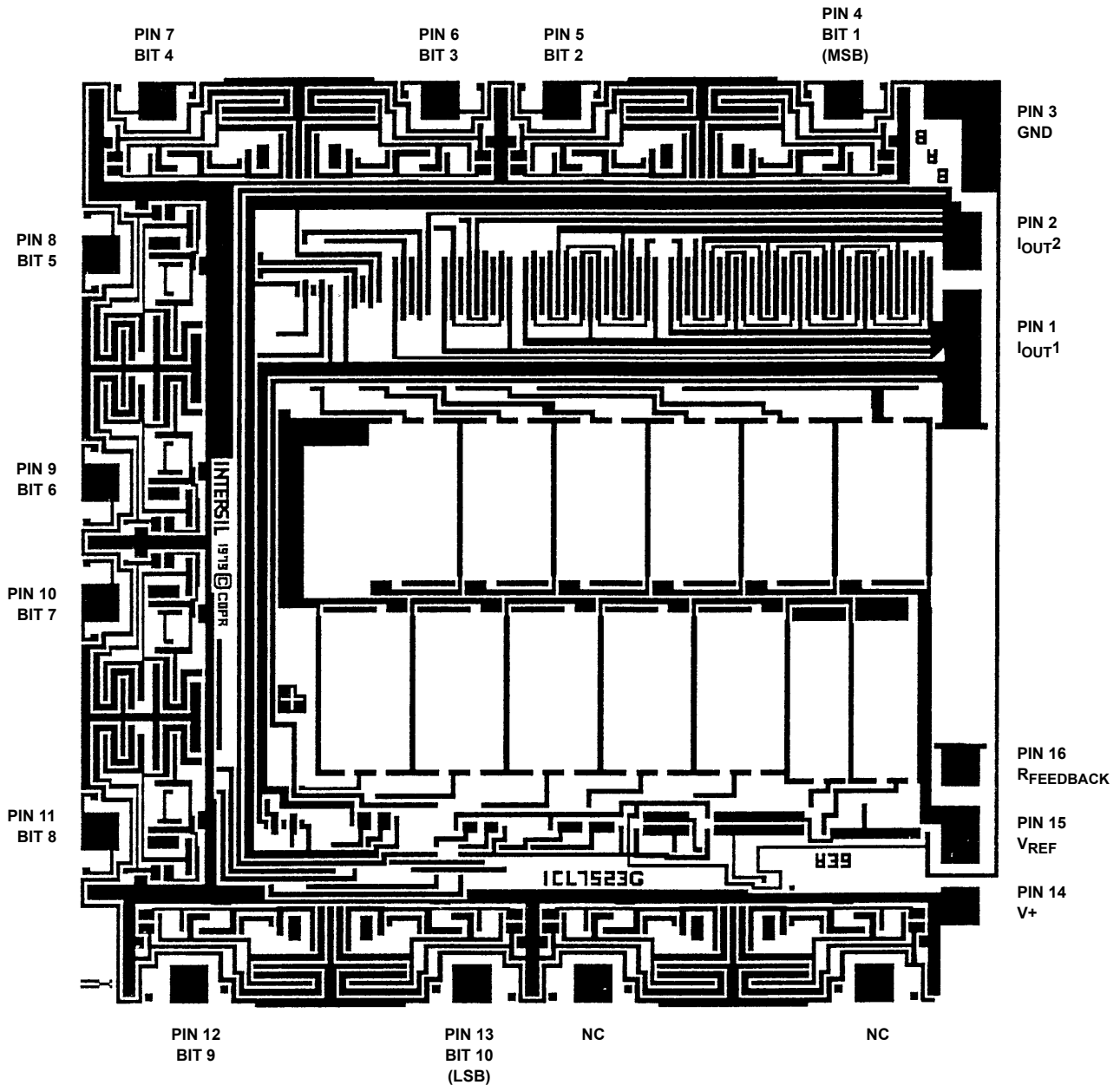
Type: PSG/Nitride  
 PSG: 7 ±1.4kÅ  
 Nitride: 8 ±1.2kÅ

**PROCESS:**

CMOS Metal Gate

**Metallization Mask Layout**

AD7520



**Die Characteristics**

**DIE DIMENSIONS:**

101 mils x 103 mils (2565µm x 2616µm)

**METALLIZATION:**

Type: Pure Aluminum  
 Thickness: 10 ±1kÅ

**PASSIVATION:**

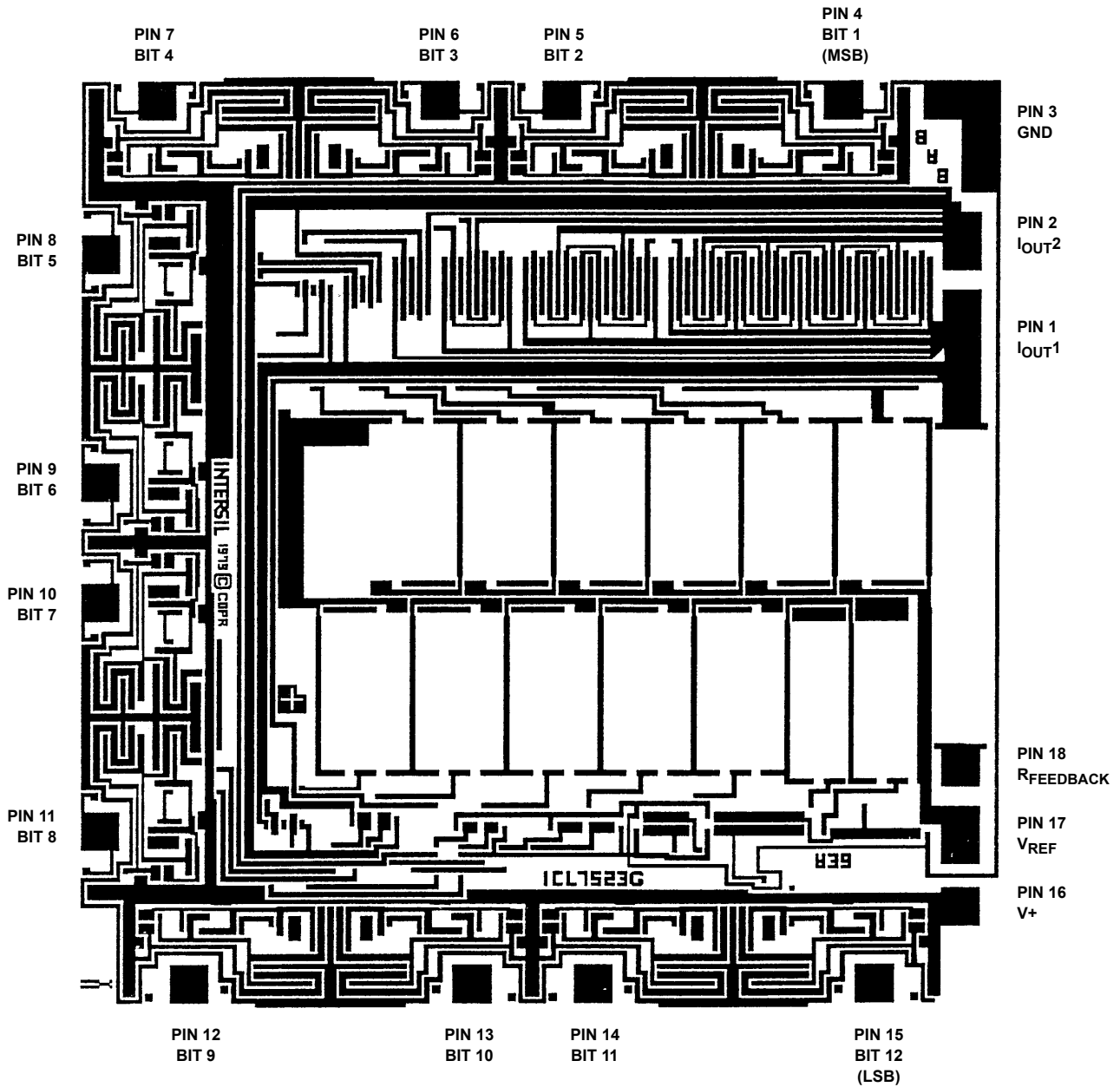
Type: PSG/Nitride  
 PSG: 7 ±1.4kÅ  
 Nitride: 8 ±1.2kÅ

**PROCESS:**

CMOS Metal Gate

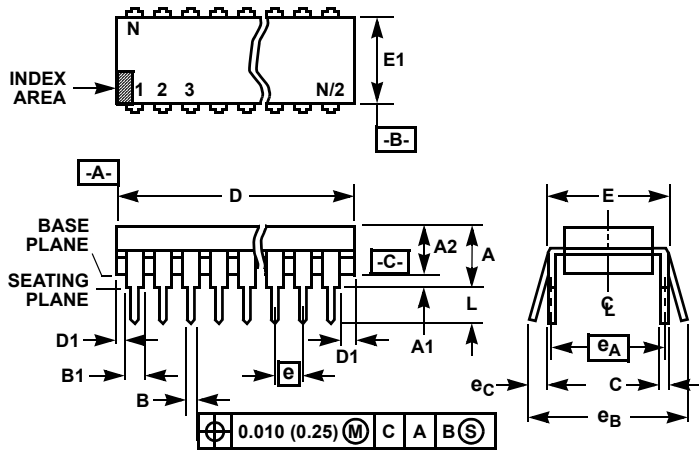
**Metallization Mask Layout**

AD7521





Dual-In-Line Plastic Packages (PDIP)



NOTES:

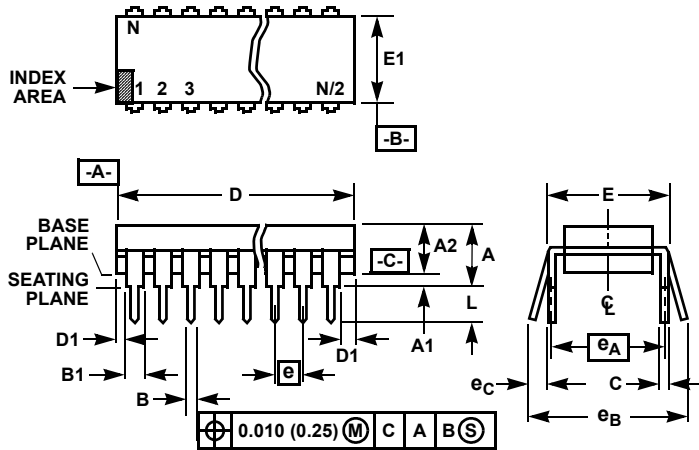
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum [-C-].
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum [-C-].
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E18.3 (JEDEC MS-001-BC ISSUE D)  
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

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