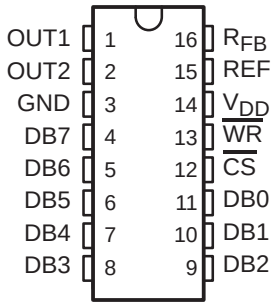
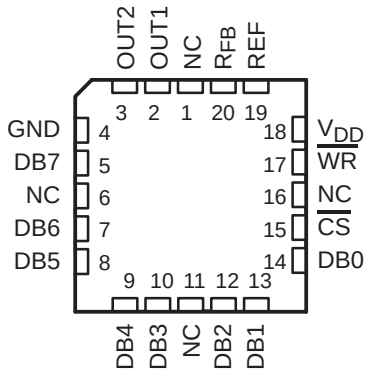
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to Be interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface With SMJ320**

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The AD7524M is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524M is an 8-bit multiplying DAC with input latches and with a load cycle similar to the write cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most-significant bits, which produce the highest glitch impulse. The AD7524M provides accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524M interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524M an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524M is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)
–55°C to 125°C	AD7524MFK	AD7524MJ

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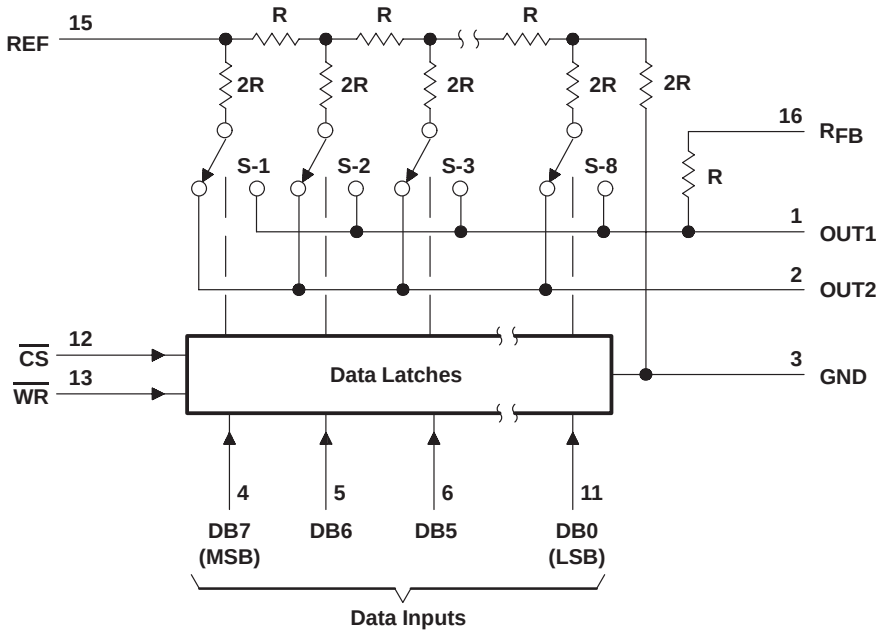
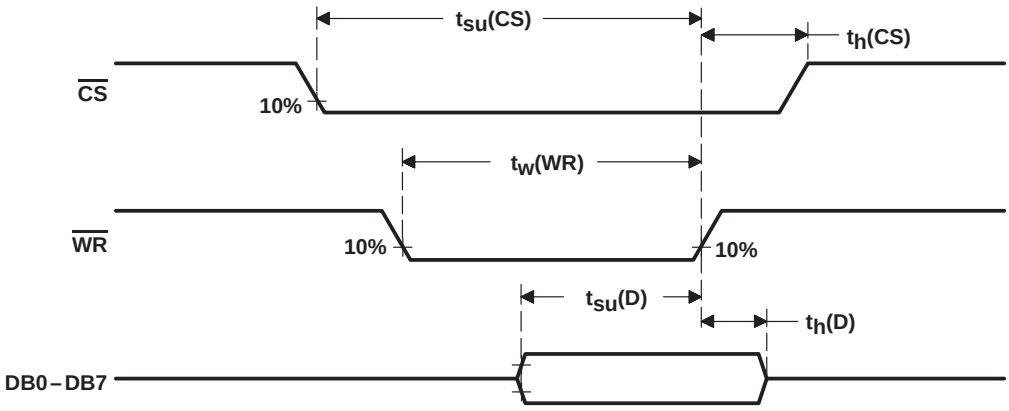
functional block diagram



operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.3 V to 17 V
Voltage between R_{FB} and GND . . . . . ±25 V
Digital input voltage range, V_I . . . . . –0.3 V to V_{DD}+0.3 V
Reference voltage range, V_{ref} . . . . . ±25 V
Peak digital input current, I_I . . . . . 10 µA
Operating free-air temperature range, T_A . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	V_{DD} = 5 V			V_{DD} = 15 V			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}		±10			±10		V
High-level input voltage, V_{IH}	2.4			13.5			V
Low-level input volage, V_{IL}			0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$	40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$	0			0			ns
Data bus input setup time, $t_{su(D)}$	25			25			ns
Data bus input hold time, $t_{h(D)}$	10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$	40			40			ns
Operating free-air temperature, T_A	–55		125	–55		125	°C

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$	Full-range			10			10	µA
				25°C			1			1	
I_{IL}	Low-level input current		V_I = 0	Full-range			–10			–10	µA
				25°C			–1			–1	
I_{pkg}	Output leakage current	OUT1	$\overline{DB0}$–DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V	Full-range			±400			±200	nA
			V_{ref} = ±10 V	25°C			±50			±50	
		OUT2	$\overline{DB0}$–DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0	Full-range			±400			±200	
			V_{ref} = ±10 V	25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0–DB7 at V_{IH}min or V_{IL}max				2			2	mA
		Standby	DB0–DB7 at 0 V or V_{DD}	Full-range			500			500	µA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, $\Delta gain/\Delta V_{DD}$		ΔV_{DD} = 10%	Full-range			0.16			0.04	%/%
				25°C		0.002	0.02		0.001	0.02	pF
C_i	Input capacitance, DB0–DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0				5			5	pF
C_o	Output capacitance	OUT1	DB0–DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0–DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC} = 5 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 1	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0–DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} – 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0–DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524M is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source 1/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524M D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524M analog output responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the CS signal or WR signal goes high, the data on the DB0–DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524M is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

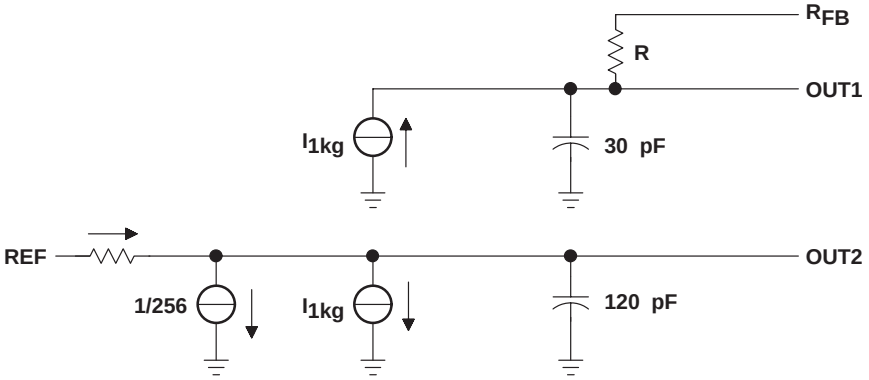


Figure 1. AD7524M Equivalent Circuit With All Digital Inputs Low

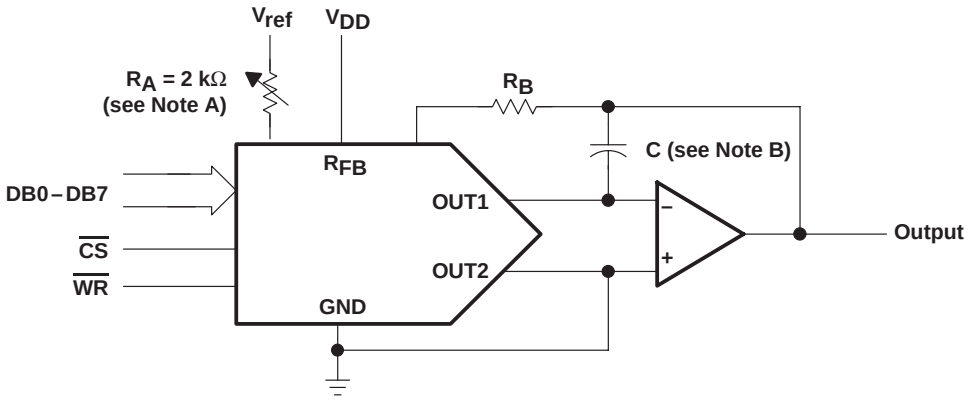


Figure 2. Unipolar Operation (2-Quadrant Multiplication)

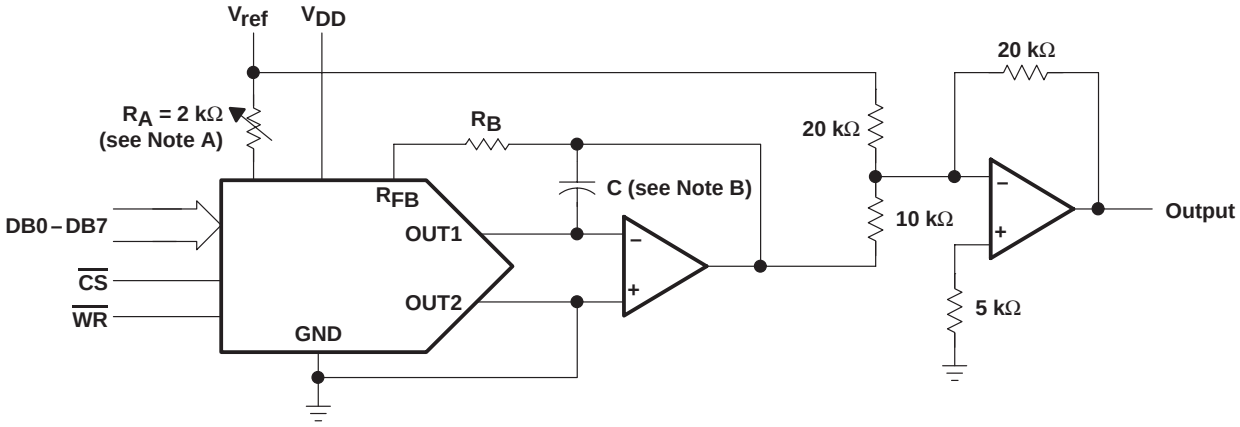


Figure 3. Bipolar Operation (4-Quadrant Operation)

NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10 – 15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (see NOTE 3)		ANALOG OUTPUT
MSB	LSB	
11111111		$-V_{ref}$ (255/256)
10000001		$-V_{ref}$ (129/256)
10000000		$-V_{ref}$ (128/256) = $-V_{ref}$ /2
01111111		$-V_{ref}$ (127/256)
00000001		$-V_{ref}$ (1/256)
00000000		0

NOTES: 3. LSB = 1/256 (V_{ref}).

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (see NOTE 4)		ANALOG OUTPUT
MSB	LSB	
11111111		V_{ref} (127/128)
10000001		V_{ref} (128)
10000000		0
01111111		$-V_{ref}$ (128)
00000001		$-V_{ref}$ (127/128)
00000000		$-V_{ref}$

NOTES: 4. LSB = 1/128 (V_{ref}).

microprocessor interfaces

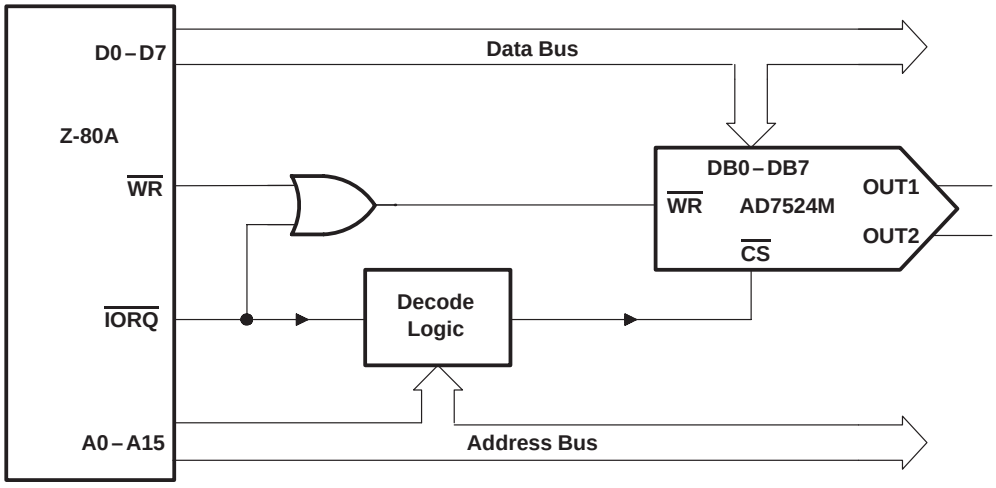


Figure 4. AD7524M – Z-80A Interface

PRINCIPLES OF OPERATION

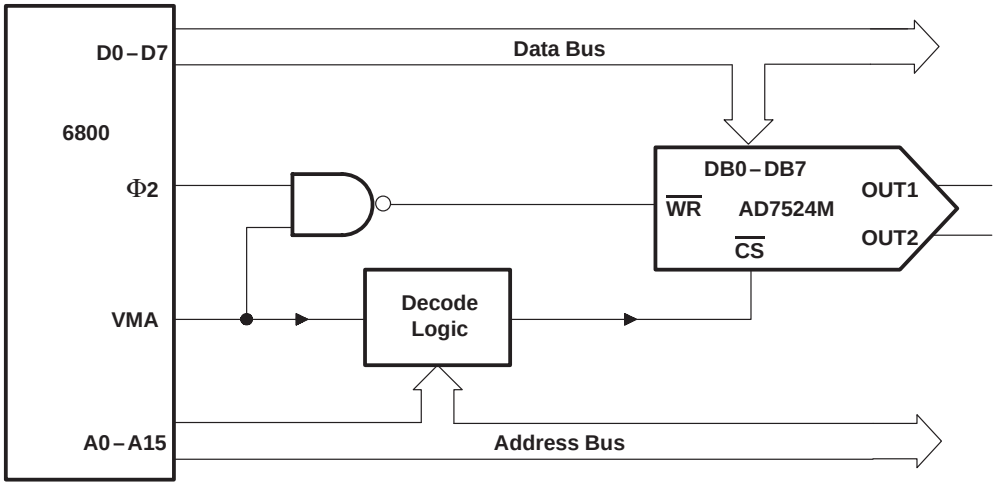


Figure 5. AD7524M – 6800 Interface

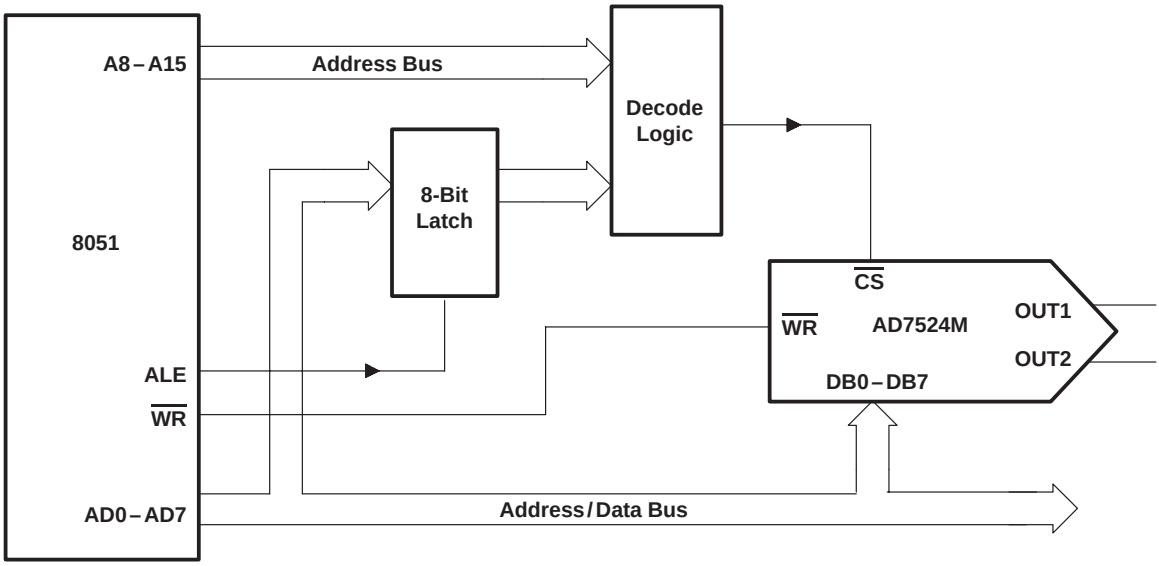


Figure 6. AD7524M–8051 Interface

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-87700012A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
5962-8770001EA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
AD7524MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
AD7524MJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
AD7524MJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

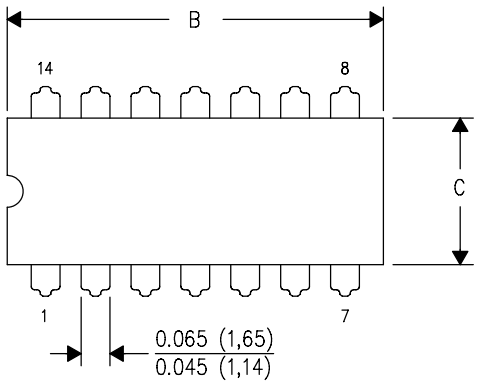
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

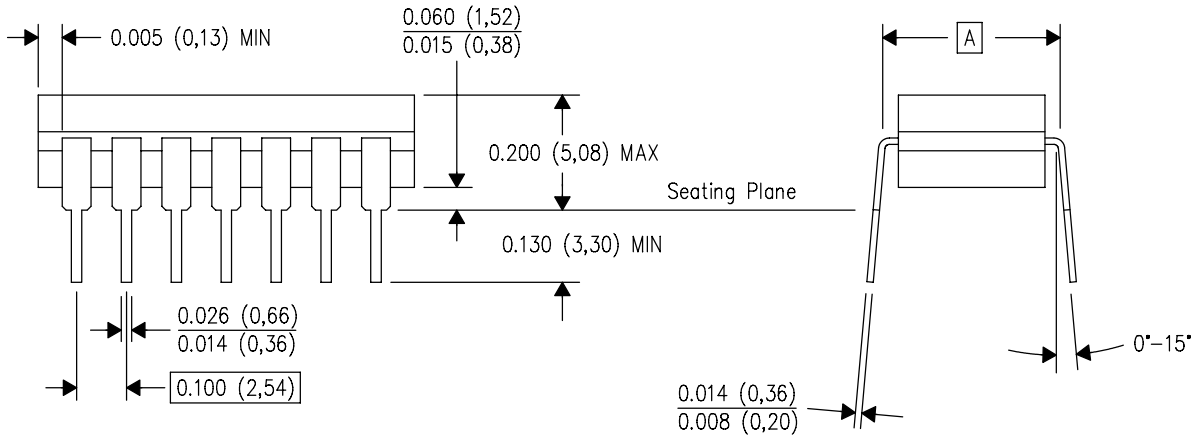
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

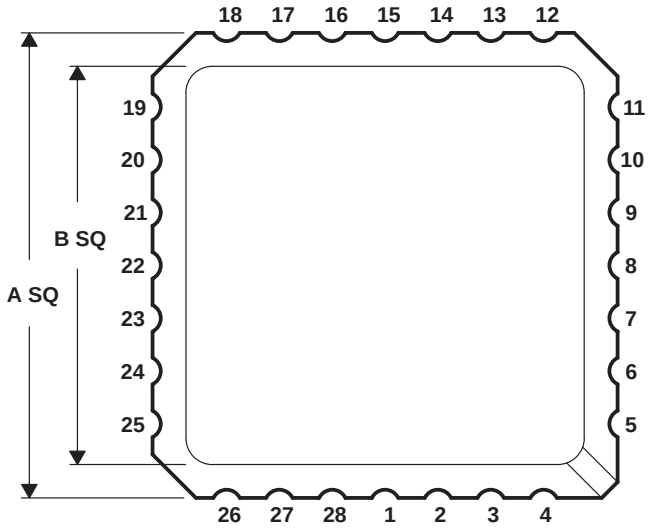


4040083/F 03/03

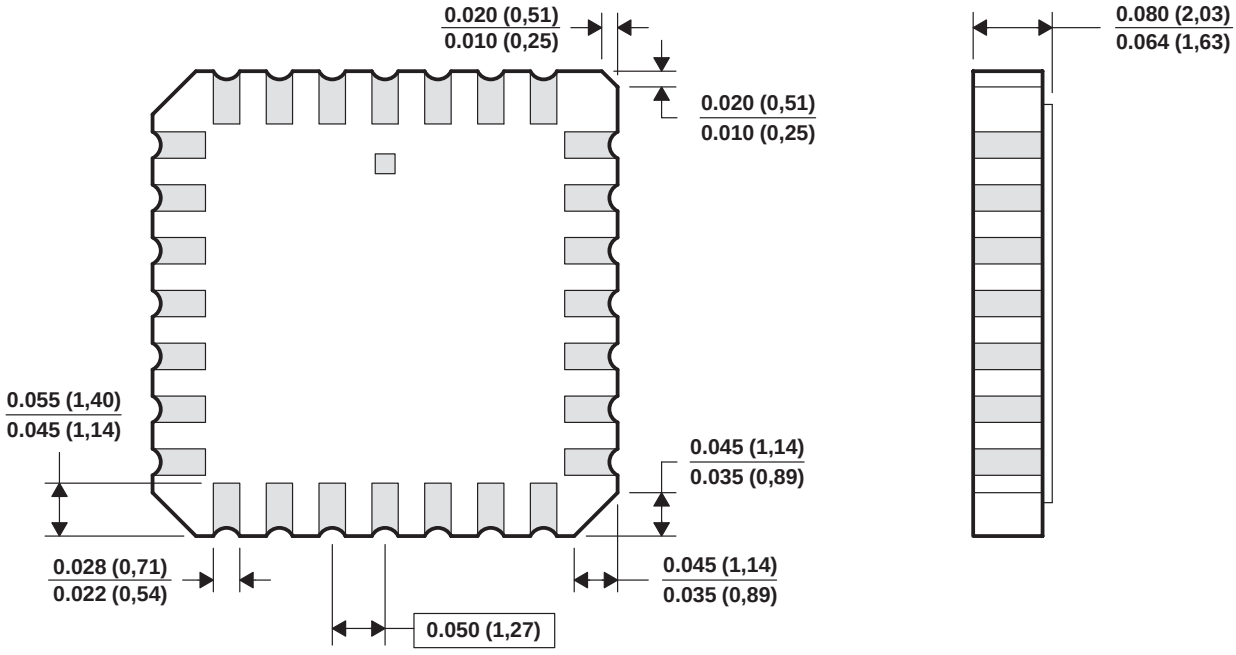
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

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