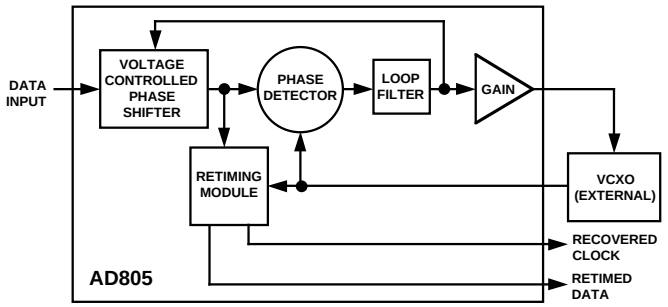
Data Retiming Phase-Locked Loop

AD805*

FEATURES
155 Mbps Clock Recovery and Data Retiming
Permits CCITT G.958 Type A Jitter Tolerance
Permits CCITT G.958 Type B Jitter Transfer
Random Jitter: 0.6° rms
Pattern Jitter: Virtually Eliminated
Jitter Peaking: Fundamentally None
Acquisition: 30 Bit Periods
Accepts NRZ Data without Preamble
Single Supply Operation: –5.2 V or +5 V
10 KH ECL Compatible

CLOCK RECOVERY AND DATA RETIMING APPLICATION



PRODUCT DESCRIPTION

The AD805 is a data retiming phase-locked loop designed for use with a Voltage Controlled Crystal Oscillator (VCXO) to perform clock recovery and data retiming on Nonreturn to Zero (NRZ) data. The circuit provides clock recovery and data retiming on standard telecommunications STS-3 or STM-1 data (155.52 Mbps). A Vectron C0-434Y Series VCXO circuit is used with the AD805 for specification purposes. Similar circuit performance can be obtained using other commercially available VCXO circuits. The AD805-VCXO circuit used for clock recovery and data retiming can also be used for large factor frequency multiplication.

The AD805-VCXO circuit meets or exceeds CCITT G.958 regenerator specifications for STM-I Type A jitter tolerance and STM-1 Type B jitter transfer. The simultaneous Type A, wide-band jitter tolerance and Type B, narrow-band jitter transfer allows the use of the AD805-VCXO circuit in a regenerative application to overcome optical line system interworking limitations based on signal retiming using Type A passive tuned device technology such as Surface-Acoustic-Wave (SAW) or dielectric resonator filters, with Type B active devices such as Phase-Locked Loops (PLLs).

The circuit VCXO provides a stable and accurate clock frequency signal with or without input data. The AD805 works with the VCXO to dynamically adjust the recovered clock frequency to the frequency associated with the input data. This frequency control loop tracks any low frequency component of jitter on the input data. Since the circuit uses the VCXO for clock recovery, it has a high Q for excellent wideband jitter attenuation. The jitter transfer characteristic of the circuit is within the jitter transfer requirements for a CCITT G.958 STM-1 Type B regenerator, which has a corner frequency of 30 kHz.

The AD805 overcomes the higher frequency jitter tolerance limitations associated with traditional high Q, PLL based clock and data recovery circuits through the use of its data retiming loop. This loop, made up of the AD805's voltage-controlled phase shifter, phase detector, and loop filter, act to align input data phase errors to the stable recovered clock provided by the VCXO. The range of the voltage-controlled phase shifter, at least 2 Unit Intervals (UI), and the bandwidth of this loop, at roughly 3 MHz, provide the circuit with its wideband jitter tolerance characteristic.

The circuit can acquire lock to input data very quickly, within 44 bit periods, due to the accuracy of the VCXO and the action of the data retiming loop. Typical integrated second-order PLLs take at least several thousand bit periods to acquire lock. This is due to their having a wide tuning range VCO. Decreasing the loop damping of a traditional second-order PLL shortens the length of the circuit's acquisition time, but at the expense of greater jitter peaking.

The AD805-VCXO circuit is a second- order PLL that has no jitter peaking. The zero used to stabilize the control loop of the traditional second-order PLL effects the closed-loop transfer function, causing jitter peaking in the jitter transfer function. In the AD805-VCXO circuit, the zero needed to stabilize the loop is implemented in the feedback path, in the voltage-controlled phase shifter. Placing the zero in the feedback path results in fundamentally no jitter peaking since the zero is absent from the closed-loop transfer function.

Output jitter, determined primarily by the VCXO, is a very low 0.6° rms. Jitter due to variations in input data density, pattern jitter, is virtually eliminated in the circuit due to the AD805's patented phase detector.

The data retiming loop of the AD805 can be used with a passive tuned circuit (155.52 MHz) such as a bandpass or a SAW filter for clock recovery and data retiming. The data retiming loop acts to servo the phase of the input data to the phase of the recovered clock from the passive tuned circuit in this type of application (see APPLICATIONS).

The AD805 uses 10 KH ECL levels and consumes 375 mW from a +5 V or a –5.2 V supply. The device is specified for operation over the industrial temperature range of –40°C to +85°C and is available in a 20-pin plastic DIP.

*Protected by U.S. Patent No. 5,036,298

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AD805–SPECIFICATIONS (V_{EE} = V_{MIN} to V_{MAX}, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

Parameter	Condition	AD805BN Min	Typ	Max	Units
NOMINAL DATA RATE[1]			155.52		Mbps
TRACKING RANGE/CAPTURE RANGE[1]		±50	±70		ppm of Nominal Data Rate
STATIC PHASE ERROR[1]	2^7–1 PRN Sequence 2^{23}–1 PRN Sequence		7 7	33 33	Degrees Degrees
OUTPUT JITTER[1]	2^7–1 PRN Sequence 2^{23}–1 PRN Sequence		0.6 0.6	1.0 1.0	Degrees rms Degrees rms
JITTER TOLERANCE[1]	f = 10 Hz f = 30 Hz f = 300 Hz f = 6.5 kHz f = 65 kHz f = 650 kHz f = 1.3 MHz	375 125 12.5 2.2 2.2 0.84 0.65	440 147 16 3.2 3.0 1.4 0.85		Unit Intervals p-p Unit Intervals p-p Unit Intervals p-p Unit Intervals p-p Unit Intervals p-p Unit Intervals p-p Unit Intervals p-p
JITTER TRANSFER[1] Peaking Bandwidth	2^7–1 PRN Sequence		 0 10	 0.1[2]	 dB kHz
RECOVERED CLOCK SKEW	T_{RCS}	0.2	0.6	1.1	ns
TRANSITIONLESS DATA RUN[1]			1000	500	Bit Periods
ACQUISITION TIME	2^7–1 PRN Sequence		30	44	Bit Periods
VCXO CONTROL OUTPUT RESISTANCE VCXO Control Voltage High Level (V_{CC} – V_{OH}) VCXO Control Voltage Low Level (V_{OL} – V_{EE})	 No Load No Load		1000 1 0.8	 1.3 1.15	Ω Volts Volts
POWER SUPPLY Voltage (V_{MIN} to V_{MAX}) Current	 T_A = +25°C, V_{EE} = –5.2 V	 –4.5 	 –5.2 70	 –5.5 90 95	 Volts mA mA
INPUT VOLTAGE LEVELS Input Logic High, V_{IH} Input Logic Low, V_{IL}	T_A = +25°C	 –1.08 –1.95	 	 –0.72 –1.59	 Volts Volts
OUTPUT VOLTAGE LEVELS Output Logic High, V_{OH} Output Logic Low, V_{OL}	T_A = +25°C	 –1.08 –1.95	 	 –0.72 –1.60	 Volts Volts
INPUT CURRENT LEVELS Input Logic High, I_{IH} Input Logic Low, I_{IL}	T_A = +25°C			 125 80	 µA µA
OUTPUT SLEW TIMES Rise Time (t_R) Fall Time (t_F)	T_A = +25°C 20%–80% 80%–20%		 0.75 0.75	 1.5 1.5	 ns ns
BUFFERED CLOCK DISTORTION (DUTY CYCLE DISTORTION) Recovered Clock Output	 ρ = 1/2, T_A = +25°C, V_{EE} = –5.2 V		 ±0.5		 %
OPERATING TEMPERATURE RANGE[1] (T_{MIN} to T_{MAX})		 –40		 +85	 °C

VCXO CIRCUIT SPECIFICATIONS

Parameter	Condition	Min	Typ	Max	Units
CENTER FREQUENCY			155.52		MHz
CONTROL VOLTAGE		–4		–1	Volts
VCXO TUNING RANGE		±50	±70		ppm of Center Frequency
MODULATION BANDWIDTH		100	500		kHz
TRANSFER FUNCTION		Positive, Monotonic			N/A

NOTES
[1]These specifications reflect the performance of the circuit shown in Figure 12. VCXO circuit parameters critical to overall circuit performance are listed above.
[2]This specification results from tests accurate to ±0.1 dB, and from statistical analysis of the test results distribution. The AD805-VCXO circuit has no jitter peaking. Reference the discussion in the THEORY OF OPERATION section.

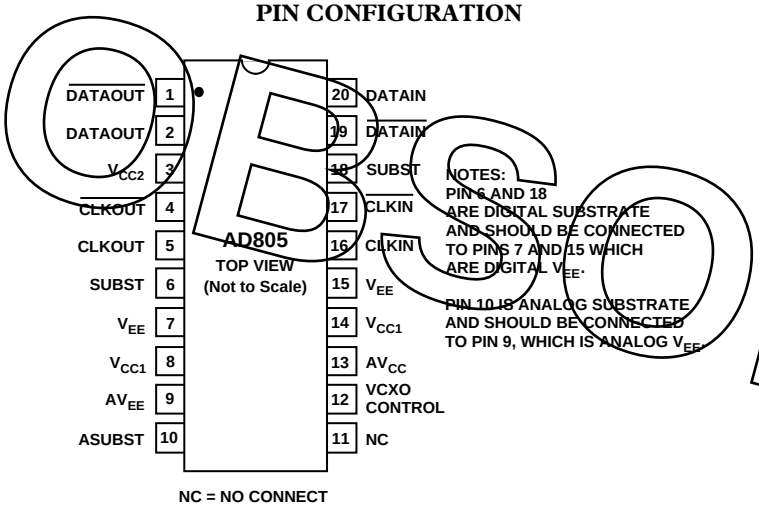
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –6 V
Input Voltage (Pin 19 or 20 to V_{EE}) . . . . . V_{EE} to +300 mV
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature
Plastic DIP Package . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 60 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to an absolute maximum rating condition for an extended period may adversely affect device reliability.

PIN CONFIGURATION



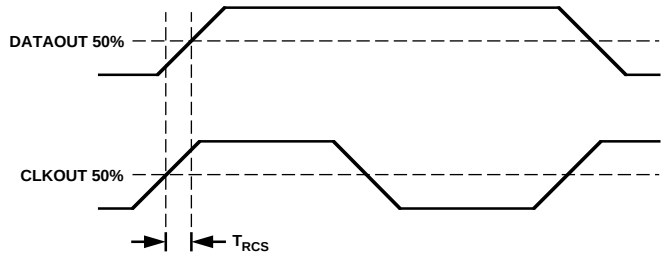


Figure 1. Recovered Clock Skew (See Specifications Page)

PIN DESCRIPTIONS

Number	Mnemonic	Description
1	$\overline{\text{DATAOUT}}$	Differential Retimed Data Output
2	DATAOUT	Differential Retimed Data Output
3	V_{CC2}	Digital Ground
4	$\overline{\text{CLKOUT}}$	Differential Recovered Clock Output
5	CLKOUT	Differential Recovered Clock Output
6	SUBST	Substrate
7	V_{EE}	Digital V_{EE}
8	V_{CC1}	Digital Ground
9	AV_{EE}	Analog V_{EE}
10	ASUBST	Analog Substrate
11	NC	No Connection
12	VCXO CONTROL	VCXO Control Voltage Output
13	AV_{CC}	Analog Ground
14	V_{CC1}	Digital Ground
15	V_{EE}	Digital V_{EE}
16	CLKIN	Differential Clock Input
17	$\overline{\text{CLKIN}}$	Differential Clock Input
18	SUBST	Substrate
19	$\overline{\text{DATAIN}}$	Differential Data Input
20	DATAIN	Differential Data Input

ORDERING GUIDE AND THERMAL CHARACTERISTICS

Device	Description	Operating Temperature	θ_{JA}	Package Option
AD805BN	20-Pin Plastic DIP	–40°C to +85°C	80°C/W	N-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD805 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GLOSSARY

AD805 performance is specified using a Vectron C0-434Y ECL Series Hybrid VCXO, SCD No. 434Y2365.

Nominal Data Rate
This is the data rate that the circuit is specified to operate on. The data format is Nonreturn to Zero (NRZ).

Operating Temperature Range (T_{MIN} to T_{MAX})
This is the operating temperature range of the AD805 in the circuit. Each of the additional components of the circuit is held at 25°C, nominal. The operating temperature range of the circuit can be extended to the operating temperature range of the AD805 through the selection of circuit components that operate from T_{MIN} to T_{MAX}.

Tracking Range
This is the range of input data rates over which the circuit will remain in lock. The VCXO CONTROL voltage range and the VCXO frequency range determine circuit tracking range.

Capture Range
This is the range of frequencies over which the circuit can acquire lock. The VCXO CONTROL voltage range and the VCXO frequency range determine circuit capture range.

Static Phase Error
This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error and IC input and output signals prohibit direct measurement of static phase error.

Recovered Clock Skew, T_{RCS}
This is the time difference, in ns, between the recovered clock signal rising edge midpoint and midpoint of the rising or falling edge of the output data signal. Refer to Figure 1.

Data Transition Density, ρ
This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to clock periods.

Transitionless Data Run
This is measured by interrupting an input data pattern with ρ = 1/2 with a block of data bits without transitions, and then reapplying the ρ = 1/2 input data. The circuit will handle this sequence without making a bit error. The length of the block of input data without transitions that an AD805-VCXO circuit can handle is a function of the VCXO K_0. The VCXO in the circuit of Figure 12 has a K_0 of 60 radians/volt, nominally.

Jitter
This is the dynamic displacement of digital signals from their long term average positions, measured in degrees rms, or Unit Intervals (UI). Jitter on the input data can cause dynamic phase errors on the recovered clock. Jitter on the recovered clock causes jitter on the retimed data.

Output Jitter
This is the jitter on the retimed data, in degrees rms, due to a specific pattern or some pseudo-random input data sequence (PRN Sequence). The random output jitter of the VCXO contributes to Output Jitter.

Jitter Tolerance
Jitter tolerance is a measure of the circuit's ability to track a jittery input data signal. Jitter on the input data is best thought of as phase modulation and is usually specified in Unit Intervals (UI). The circuit will have a bit error rate less than 1×10^{-10} when in lock and retiming input data that has the specified jitter applied to it.

Refer to the THEORY OF OPERATION section for a description of the jitter tolerance of the AD805-VCXO circuit.

Jitter Transfer
The circuit exhibits a low-pass filter response to jitter applied to its input data. The circuit jitter transfer characteristics are measured using the method described in CCITT Recommendation G.958, Geneva 1990, Section 6.3.2. This method involves applying sinusoidal input jitter up to the jitter tolerance mask level for an STM-1 Type A regenerator.

Bandwidth
This describes the frequency at which the circuit attenuates sinusoidal input jitter by 3 dB.

Peaking
This describes the maximum jitter gain of the circuit in dB.

Acquisition Time
This is the transient time, measured in bit periods, required for the circuit to lock on input data from its free-running state.

Buffered Clock Distortion
This is a measure of the duty cycle distortion at the AD805 CLKOUT signals relative to the duty cycle distortion at the AD805 CLKIN signals.

Bit Error Rate vs. Signal-to-Noise Ratio
The AD805 is intended to operate with standard ECL signal levels at the data input. Although not recommended, smaller input signals are tolerable. Figure 6 shows the bit error rate performance versus input signal-to-noise ratio for input signal amplitudes of full 900 mV ECL, and decreased amplitudes of 80 mV and 20 mV. Wideband amplitude noise is summed with the data signals as shown in Figure 2. The full ECL, 80 mV, and 20 mV input signals give virtually indistinguishable results.

The axes used for Figure 6 are scaled so that the theoretical Bit Error Rate vs. Signal to Noise Ratio curve appears as a straight line. The curve that fits the actual data points has a slope that matches the slope of the theoretical curve for all but the higher values of signal-to-noise ratio and lower values of bit error rate. For high values of signal-to-noise ratio, the noise generator used clips, and therefore is not true Gaussian. The extreme peaks of the noise cause bit errors for high signal to noise ratios and low bit error rates. The clipping of the noise waveform limits bit errors in these cases.

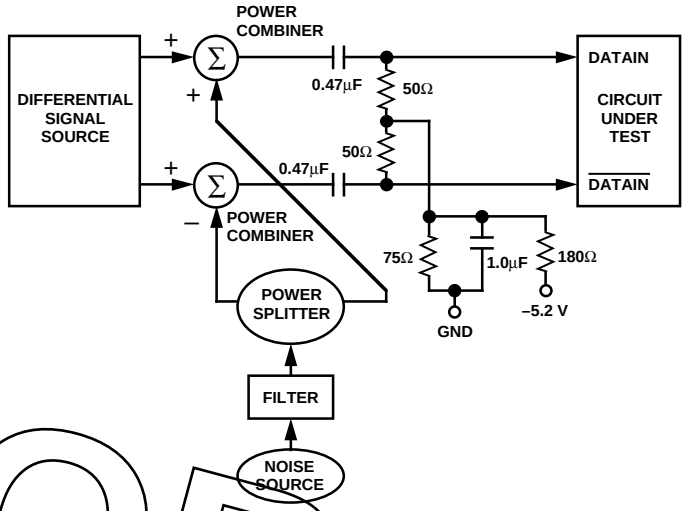


Figure 2. Bit Error Rate vs. Signal-to-Noise Ratio Test: Block Diagram

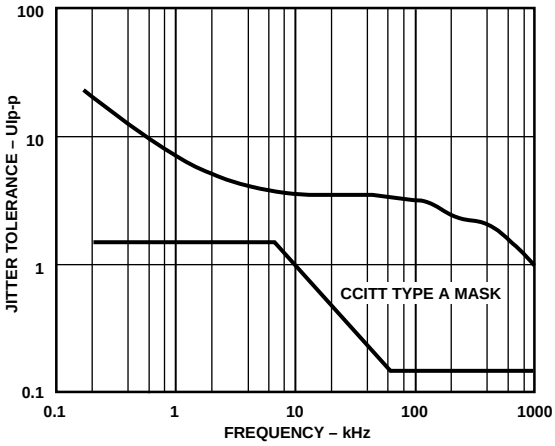


Figure 5. Jitter Tolerance

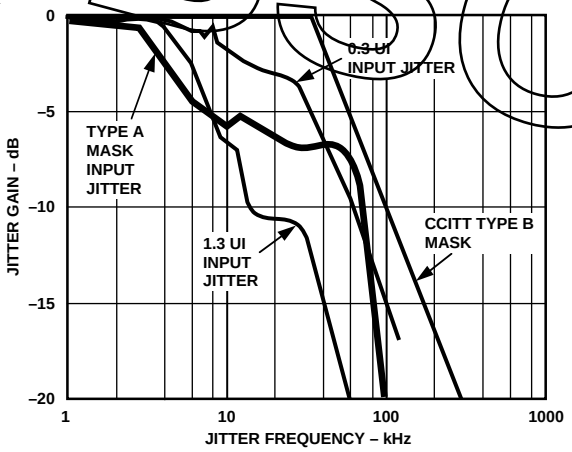


Figure 3. Jitter Transfer – Bandwidth

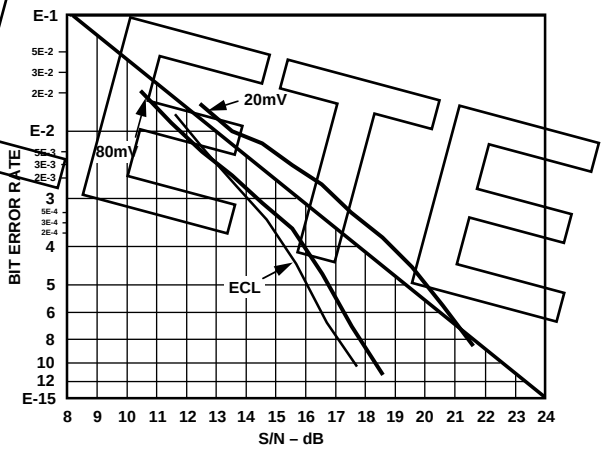


Figure 6. Bit Error Rate vs. Signal-to-Noise Ratio

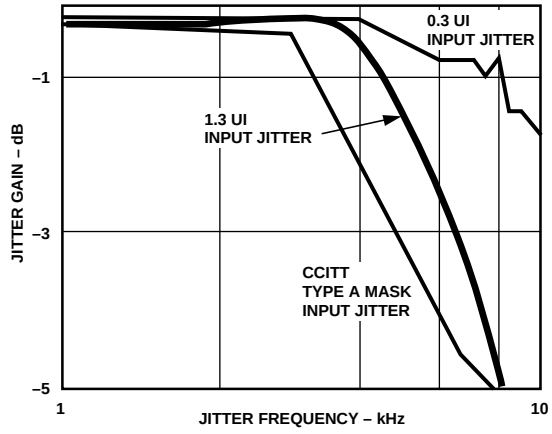


Figure 4. Jitter Transfer – Peaking

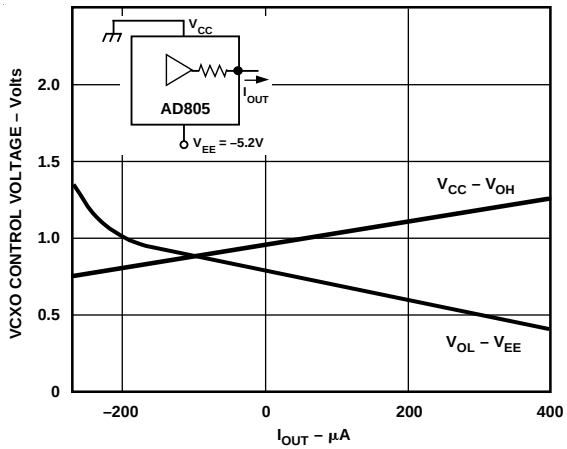


Figure 7. VCXO Control Voltage vs. Load

THEORY OF OPERATION

The AD805 is a delay- and phase- locked loop circuit for clock recovery and data retiming from an NRZ-encoded data stream. Figure 8 is a block diagram of the device shown with an external VCXO. The AD805-VCXO circuit tracks the phase of the input data using two feedback loops that share a common control voltage. A high speed delay-locked loop path uses an on-chip voltage-controlled phase shifter (VCPS) to track the high frequency components of jitter on the input data. A separate frequency control loop, using the external VCXO, tracks the low frequency components of jitter on the input data.

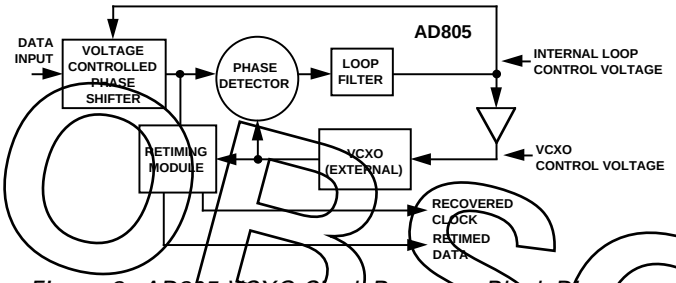


Figure 8. AD805-VCXO Clock Recovery Block Diagram

The two loops work together to null out phase error. For example, when the clock is behind the data, the phase detector drives the VCXO to a higher frequency and also increases the delay through the VCPS. These actions serve to reduce the phase error. The faster clock picks up phase while the delayed data loses phase. When considering a static phase error, it is easy to see that since the control voltage is developed by a loop integrator, the phase error will eventually reduce to zero.

Another view of the circuit is that the AD805 VCPS implements the zero that is required to stabilize a second order phase-locked loop and that the zero is placed in the feedback path so it does not appear in the closed-loop transfer function. Jitter peaking in an ordinary second order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since the AD805-VCXO circuit is free of any zero in its closed-loop transfer function, the circuit is free of jitter peaking.

A linearized block diagram of the AD805-VCXO circuit is shown in Figure 9. The two loops simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering.

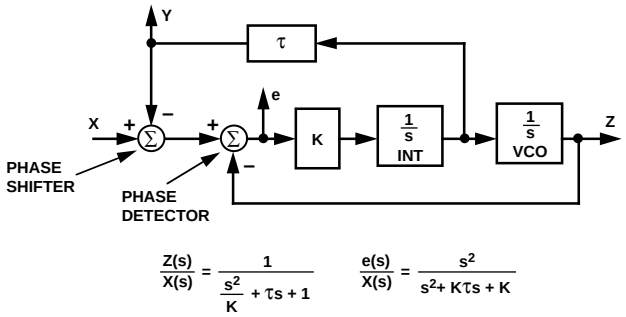


Figure 9. AD805-VCXO Circuit Linearized Block Diagram

The jitter transfer function, Z(s)/X(s), is second order and low pass, providing excellent filtering. Note that the jitter transfer function has no zero, unlike ordinary second-order phase-locked loops. This means that the circuit has fundamentally no jitter peaking (see Figure 10). Having no jitter peaking makes this circuit ideal for signal regeneration applications where jitter peaking in any regenerative stage can contribute to hazardous jitter accumulation.

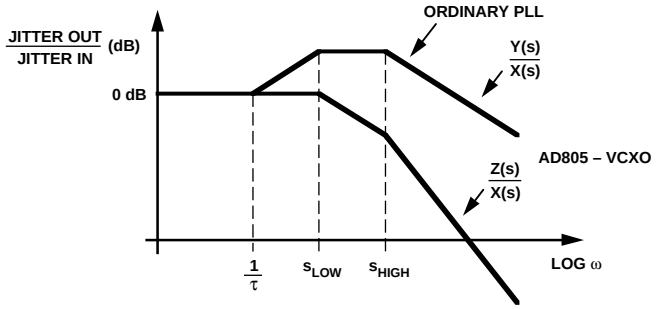


Figure 10. Circuit Jitter Transfer Functions

The error transfer function, e(s)/X(s), has the same high pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation since the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering. The circuit has an error transfer bandwidth of 3 MHz and a jitter transfer bandwidth of 10 kHz.

The circuit's two loops contribute to overall jitter accommodation. At low frequencies, the integrator provides high gain so that large jitter amplitudes can be tracked with small phase errors between inputs of the phase detector. In this case, the VCXO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCXO tuning range. A wider tuning range corresponds to increased accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the VCPS remains close to the center of its range, contributing little to jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCXO are not enough to track input jitter. In this case the VCXO control voltage input starts to hit the rails of its maximum voltage swing and the VCXO frequency output spends most of the time at one or the other extreme of its tuning range. The size of the VCXO tuning range therefore has a small effect on the jitter accommodation. The AD805 internal loop control voltage is now larger, so the VCPS takes on the burden of tracking input jitter. The VCPS range (in UI) is seen as the plateau on the jitter tolerance curve (Figure 11). The VCPS has a minimum range of 2 UI.

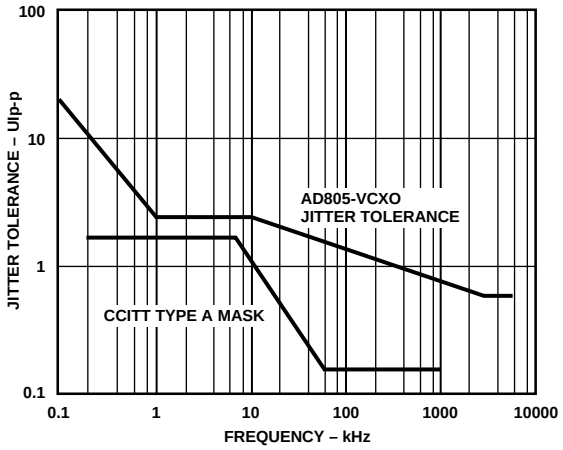


Figure 11. Jitter Accommodation Design Limit

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences between the phase detector inputs are needed to make the internal loop control voltage big enough to tune the range of the VCPS. Large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the loop integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation decreases with increasing jitter frequency. At the highest frequencies, the loop gain is very small and little tuning of the VCPS can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error and the residual loop jitter. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the 3 MHz closed-loop bandwidth of the AD805's internal delay-locked loop.

USING THE AD805

Ground Planes

Use of two ground planes, an analog ground plane and a digital ground plane, is recommended. This will isolate noise that may be on the digital ground plane from the analog ground plane.

Power Supply Connections

Power supply decoupling should take place as close to the IC as possible. This will keep noise that may be on a power supply from affecting circuit performance.

Use of a 10 μF tantalum capacitor between V_{EE} and ground is recommended.

Use of 0.1 μF ceramic capacitors between IC power supply or substrate pins and either analog or digital ground is recommended. Refer to schematic, Figure 12, for advised connections. The ceramic capacitors should be placed as close to the IC pins as possible.

Connections from V_{EE} to load resistors for DATAIN, DATAOUT, CLKIN, and CLKOUT signals should be individual, not daisy chained. This will avoid crosstalk on these signals.

Transmission Lines

Use of 50 Ω transmission lines are recommended for DATAIN, DATAOUT, CLKIN, and CLKOUT signals.

Terminations

Termination resistors should be used for DATAIN, CLKIN, DATAOUT, and CLKOUT signals. Metal, thick film, 1% tolerance resistors are recommended. Termination resistors for the DATAIN and CLKIN signals should be placed as close as possible to the DATAIN and CLKIN pins.

Input Buffer

Use of an input buffer, such as a 10H116 Line Receiver IC, is suggested for an application where the DATAIN signals do not come directly from an ECL gate, or where noise immunity on the DATAIN signals is an issue.

APPLICATIONS

155.52 MBPS CLOCK RECOVERY AND DATA RETIMING USING AT&T 157-TYPE VHF VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR

The AD805 design can be used with any VCXO circuit that has a gain of roughly 1×10^6 rad/volt-sec, a frequency pull range of at least ±50 ppm, a positive slope (a greater VCXO control voltage corresponds to a greater output frequency) and a modulation bandwidth of 500 kHz. These VCXO parameters contribute to overall circuit low frequency jitter tolerance and jitter transfer.

The output jitter of the overall circuit is largely determined by the output jitter of the VCXO. The AD805 adds little jitter since it just buffers the VCXO frequency output, adding distortion (duty cycle distortion) of only ±0.5%.

Overall circuit jitter bandwidth is determined by the slope of the VCXO output frequency vs. control voltage curve. A greater slope corresponds to a greater jitter bandwidth.

Figure 12 shows a schematic of the AD805 in a 155.52 Mbps clock recovery and data retiming application with an AT&T 157-Type VCXO (see insert). Figures 15 and 16 show typical jitter tolerance and jitter transfer curves for the circuit.

Note that the 157-Type VCXO control voltage bandwidth (modulation bandwidth) varies with respect to control voltage from 80 kHz to 500 kHz. The low value of this modulation bandwidth causes some jitter peaking when used with the AD805. The limited modulation bandwidth introduces excess phase in the frequency control loop through the VCXO. This causes the frequency control loop to become less damped. Jitter peaking of 1 dB or 2 dB results in the jitter transfer function. The compensation network on the VCXO control voltage between the AD805 and the 157-Type VCXO shown in Figure 12, effectively reduces the high frequency loop gain through the frequency control loop. The addition of this compensation network eliminates jitter peaking. The compensation network 1 kΩ resistor works with the AD805 VCXO CONTROL 1 kΩ output impedance to halve the loop crossover frequency. This avoids excess phase caused by the limited modulation bandwidth of the 157-Type VCXO.

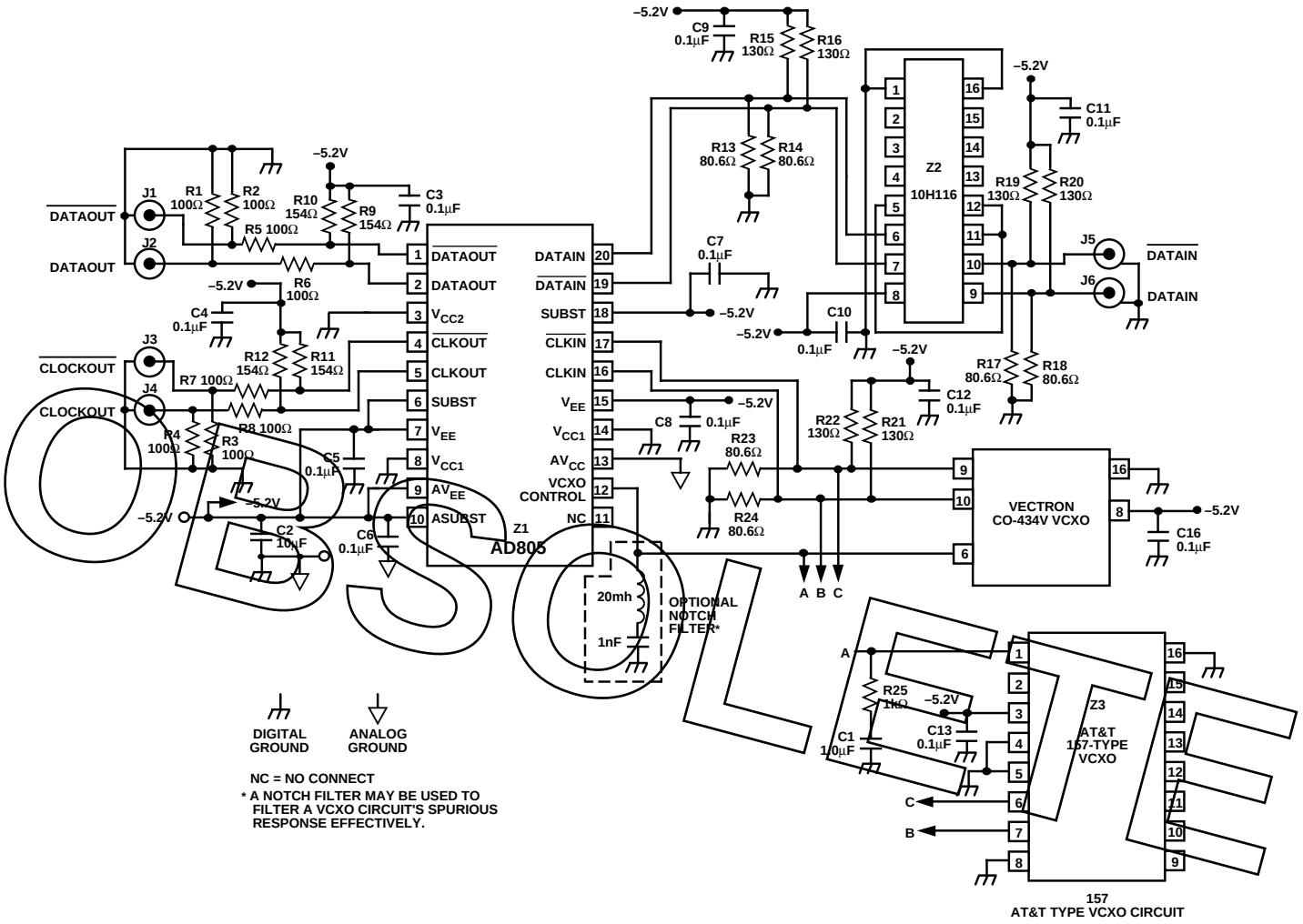


Figure 12. Evaluation Board Schematic, Negative Supply

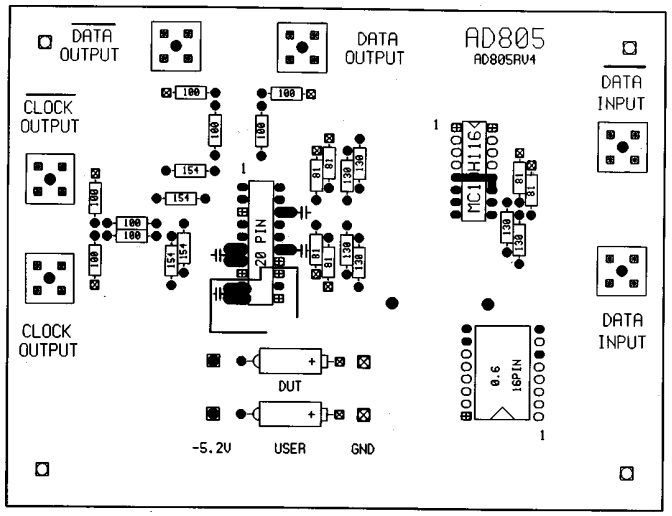


Figure 13. Evaluation Board, Component Side

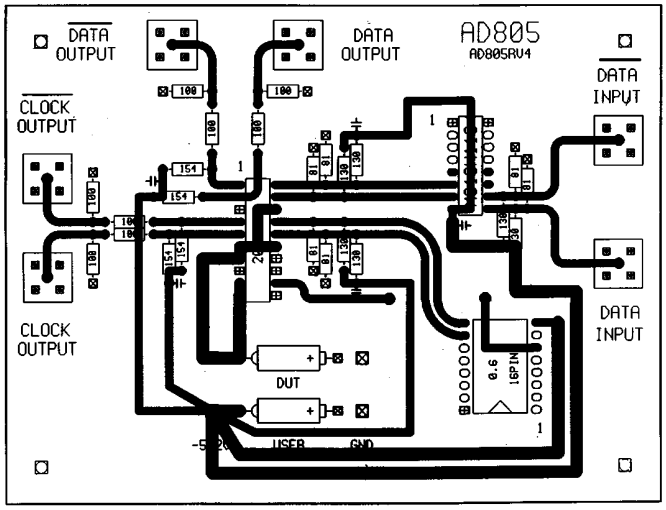


Figure 14. Evaluation Board, Solder Side

Table I. Evaluation Board, Negative Supply: Components List

Reference Designator	Description	Quantity
R1–8	Resistor, 100 Ω, 1%	8
R9–12	Resistor, 154 Ω, 1%	4
R13, 14, 17, 18, 23, 24	Resistor, 80.6 Ω, 1%	6
R15, 16, 19–22	Resistor, 130 Ω, 1%	6
C2	10 μF, Tantalum	1
C3–12, C15	0.1 μF, Ceramic Chip	11
Z1	AD805	1
Z2	10H116, ECL Line Receiver	1
	Vectron CO-434Y VCXO	1
Z3	AT&T 157-Type VCXO	1

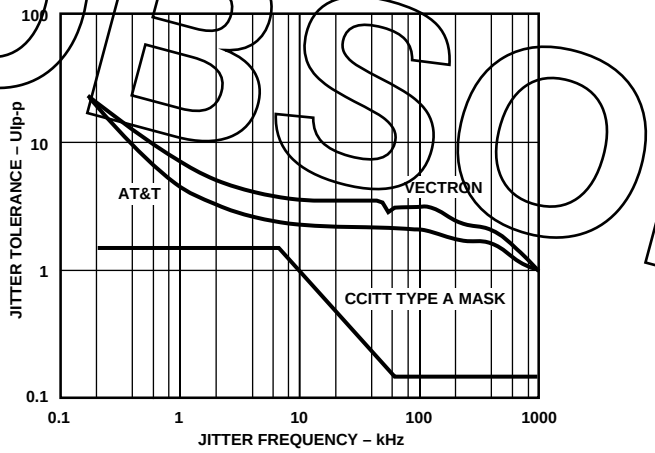


Figure 15. AD805-VCXO Circuit Jitter Tolerance

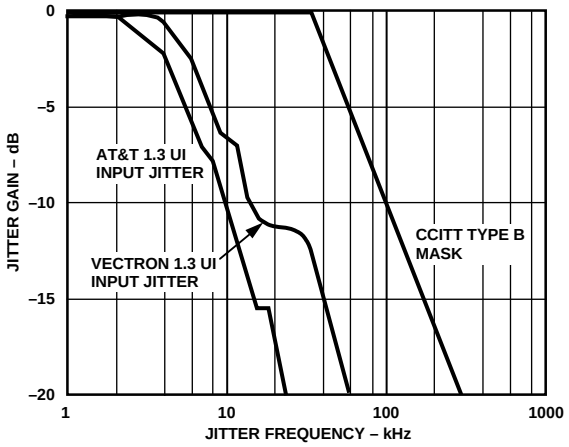


Figure 16. AD805-VCXO Circuit Jitter Transfer

155.52 MBPS CLOCK RECOVERY AND DATA RETIMING USING A SURFACE ACOUSTIC WAVE (SAW) FILTER

The AD805 can be used with a 155.52 MHz SAW filter circuit for clock recovery and data retiming. In this type of application (refer to Figure 17), the SAW filter circuit is used to generate a 155.52 MHz clock from the input data. The AD805 data retiming loop formed by the voltage-controlled phase shifter, the phase detector and the loop filter, act to servo the phase of the input data to the phase of the recovered clock. The AD805 can compensate up to ±180° phase variance through the SAW filter circuit. The AD805 replaces the D Flip-Flop and phase shifter components found in traditional SAW filter-based clock recovery and data retiming circuits. Use of the AD805 eliminates the phase shifter to SAW filter matching needed to get traditional SAW filter-based circuits to perform over operating conditions.

The jitter bandwidth and the output jitter of the overall circuit is determined largely by the SAW filter used. The AD805 retimes the input data to the recovered clock and buffers the recovered clock from the SAW filter circuit. The AD805 plays a role in the jitter accommodation of the overall circuit. The AD805's phase shifter range and the bandwidth of the data retiming loop provide for at least 2 UI p-p jitter tolerance to 1 MHz. The length of a transitionless block of data that will not cause the circuit to lose lock or start making bit errors is determined by the Q of the SAW filter used.

Figure 17 shows a schematic of the AD805 used with a Toyocom TQS-610J-6R SAW filter. The circuit that precedes the SAW filter feeds the filter with a pulse at each data transition. The line receiver circuit that immediately follows the SAW filter provides gain to the SAW filter output to drive the AD805 CLKIN signals.

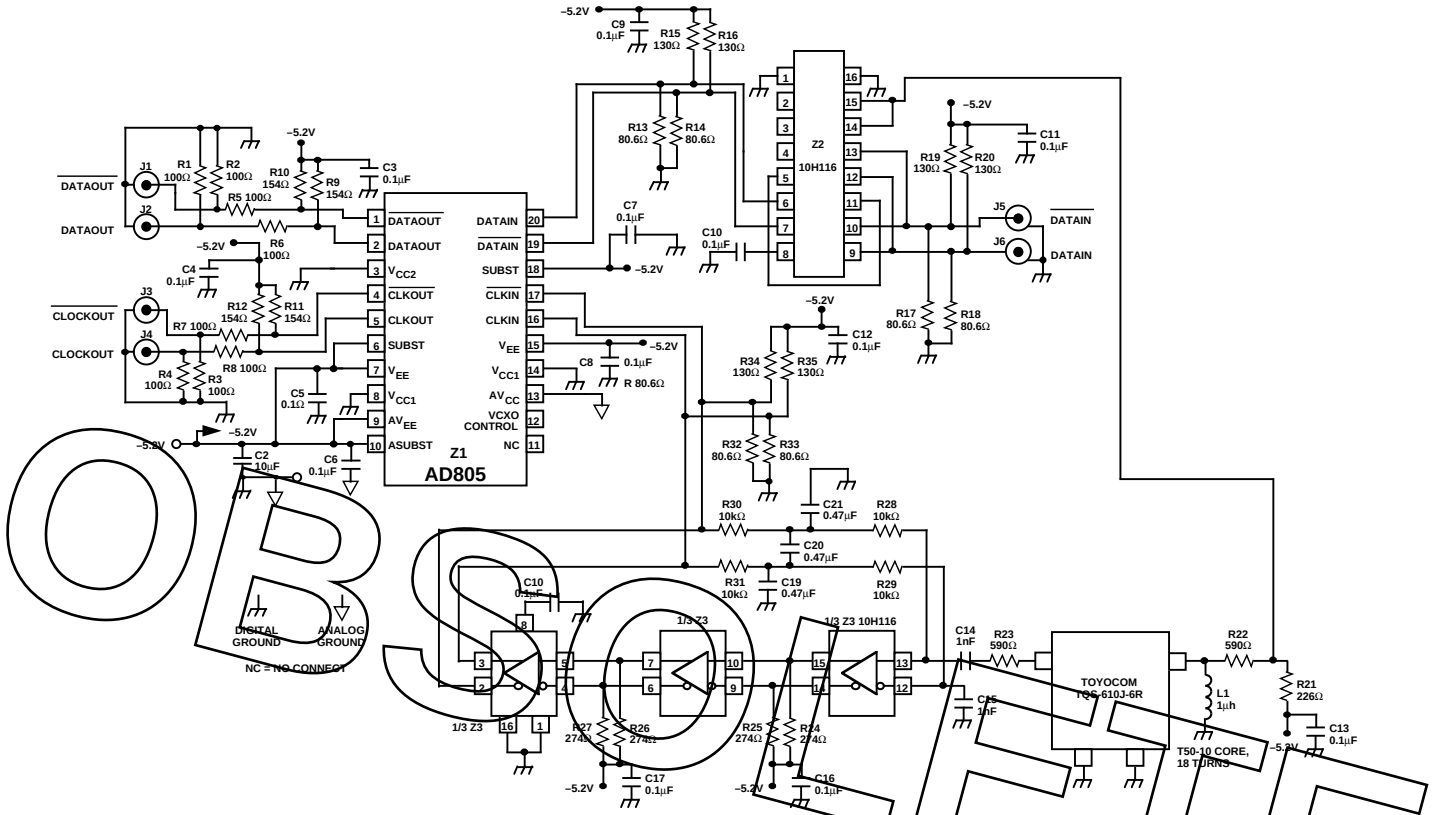


Figure 17. AD805-SAW Filter Clock Recovery and Data Retiming Circuit Schematic

Table II. AD805-SAW Filter Clock Recovery and Data Retiming Components List

Reference Designator	Description	Quantity
R1–R8	Resistor, 100 Ω, 1%	8
R9–R12	Resistor, 154 Ω, 1%	4
R13, R14, R17, R18, R32, R33	Resistor, 80.6 Ω, 1%	6
R15, R16, R19, R20, R34, R35	Resistor, 130 Ω, 1%	6
R21	Resistor, 226 Ω, 1%	1
R22, R23	Resistor, 590 Ω, 1%	2
R24–R27	Resistor, 274 Ω, 1%	4
R28–R31	Resistor, 10 kΩ, 1%	4
C2	10 µF, Tantalum	1
C3–C13, C16–C18	0.1 µF, Ceramic Chip	14
C14, C15	1 nF	2
C19–C21	0.47 mF	3
L1	1 µh, T50-10 Core, 18 Turns, Micrometals, Inc.	1
Z1	AD805	1
Z2, Z3	1OH116, ECL Line Receiver	2
Z4	Toyocom TQS-610J-6R SAW	1

LARGE FACTOR FREQUENCY MULTIPLICATION — TO 155.52 MHZ

The AD805-VCXO combination can be used to multiply a frequency at the AD805's DATAIN by a large integer multiple. This is useful for generating a 155.52 MHz bit clock from a 19.44 MHz byte clock (multiplication factor of 8). The highly accurate center frequency of the VCXO makes even larger factor frequency multiplication possible. The VCXO will not lock on a false harmonic even for large multiplication factors. For example, a VCXO with center frequency accuracy of 100 ppm will allow frequency multiplication by a factor as large as 5000. This is because the 5000th harmonic of 31.104 kHz is 155.52 MHz, and the 4999th and the 5001st harmonics are 200 ppm away from the VCXO center frequency. Since the accuracy and tuning range of the VCXO constrain its output frequency to within 100 ppm of center frequency, the circuit will reliably pick the 5000th harmonic.

Frequency multiplication by an odd factor is possible using the AD805-VCXO combination. This is not obvious. Consider a 51.84 MHz input multiplied by a factor of 3 to get to 155.52 MHz. In this case, the edge spacing of the 51.84 MHz signal is 9.65 ns, or 1-1/2 periods of the expected 155.52 MHz output. In theory, every other edge of the 51.84 MHz at the AD805's DATAIN is interpreted as 180° out of phase. In practice, however, the inherent loop jitter dithers these edges to give +179° then –179° out of phase measurements on alternate edges. Measurements on these alternate edges cancel. The circuit phase locks to the other set of alternate edges. The very low gain of the VCXO and the narrow bandwidth of the jitter transfer function gives an output that has low jitter even though alternate input edges are out of phase. When multiplying by a factor of 3, the DATAOUT will have a repeating 110 or 100 pattern. Either pattern can occur since either the rising or falling edges of the 51.84 MHz signal at the DATAIN can be the out of phase set of alternate edges.

Figure 18 shows the output jitter performance of an AD805-VCXO circuit for different integer frequency multiplication factors.

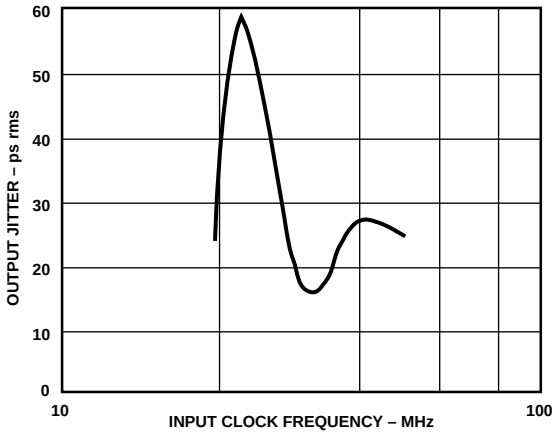


Figure 19. AD805-VCXO Circuit Clock Output Jitter vs. Integer Multiplier

DESKEWING ISOCHRONOUS 155.52 MBPS DATA STREAMS

The AD805 can be used for deskewing a 155.52 Mbps data stream to a reference 155.52 MHz clock when the clock is isochronous with the data. Figure 19 shows a diagram of an AD805 in a deskewing application. The data input to the AD802-155 clock recovery circuit and the data input to the AD805 were generated using the same 155.52 MHz clock. The AD805 data retiming loop formed by the voltage-controlled phase shifter, the phase detector, and the loop filter act to align the phase of the input data to the phase of the recovered clock. This eliminates skew that can exist between two isochronous data paths.

The AD805 will track ±180° change in skew after initial locking without bit errors. If the skew changes by more than ±180° after lock, it is possible to exceed the range of the voltage controlled phase shifter. Exceeding the phase shifter range will force the AD805 data retiming loop to reacquire to the center of the phase shifter. During this reacquisition, it is possible to make 3000 bit errors.

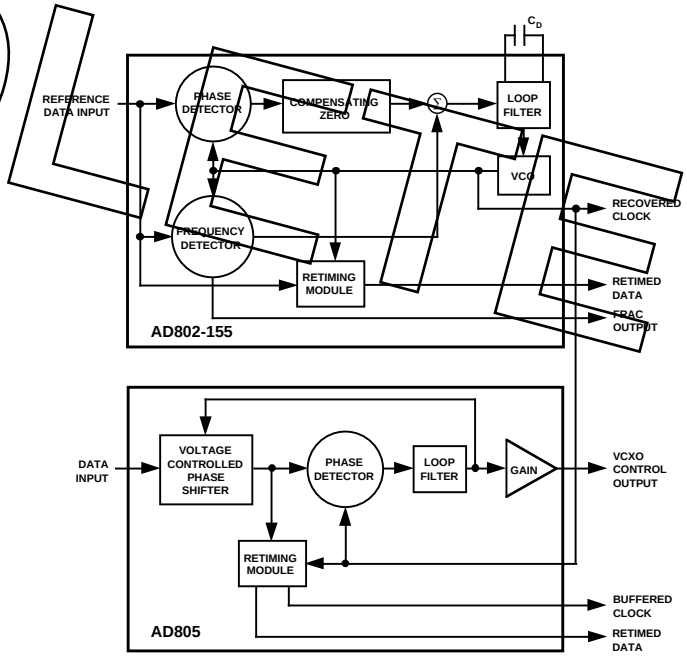
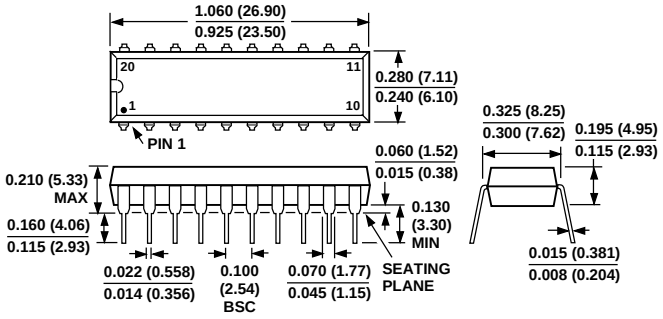


Figure 19. AD805 Deskewing Circuit Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Plastic Dual In-Line Package
(N-20)



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