ANALOG DEVICES

Low-Cost, High-Speed Rail-to-Rail Amplifiers

AD8091/AD8092

FEATURES
Low-Cost Single (AD8091), Dual (AD8092)
Voltage Feedback Architecture
Fully Specified at +3 V, +5 V, and ±5 V Supplies
Single-Supply Operation
  Output Swings to within 25 mV of Either Rail
  Input Voltage Range
    –0.2 V to +4 V; V_S = +5 V
High-Speed and Fast Settling on +5 V
  110 MHz –3 dB Bandwidth (G = +1)
  145 V/μs Slew Rate
  50 ns Settling Time to 0.1%
Good Video Specifications (G = +2)
  Gain Flatness of 0.1 dB to 20 MHz; R_L = 150 Ω
  0.03% Differential Gain Error; R_L = 1 kΩ
  0.03° Differential Phase Error; R_L = 1 kΩ
Low Distortion
  –80 dBc Total Harmonic @ 1 MHz; R_L = 100 Ω
Outstanding Load Drive Capability
  Drives 45 mA, 0.5 V from Supply Rails
  Drives 50 pF Capacitive Load (G = +1)
**Low Power of 4.4 mA/Amplifier**

APPLICATIONS
Coaxial Cable Driver
Active Filters
Video Switchers
Professional Cameras
CCD Imaging Systems
CD/DVD

CONNECTION DIAGRAMS

SOIC-8
(R-8)


```
NC    1  AD8091  8  NC
–IN   2          7  +Vs
+IN   3          6  VOUT
–Vs   4          5  NC
```
NC = NO CONNECT

μSOIC-8 and SOIC-8
(RM-8, R-8)


```
OUT1  1  AD8092  8  +Vs
–IN1  2          7  OUT
+IN1  3          6  –IN2
–Vs   4          5  +IN2
```

SOT23-5
(RT-5)


```
VOUT  1  AD8091  5  +Vs
–Vs   2          4  –IN
+IN   3
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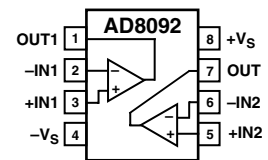
PRODUCT DESCRIPTION

The AD8091 (single) and AD8092 (dual) are low-cost, voltage feedback, high-speed amplifiers designed to operate on +3 V, +5 V, or ±5 V supplies. They have true single-supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

Despite their low cost, the AD8091/AD8092 provide excellent overall performance and versatility. The output voltage swing extends to within 25 mV of each rail, providing the maximum output dynamic range with excellent overdrive recovery. This makes the AD8091/AD8092 useful for video electronics, such as cameras, video switchers, or any high-speed portable equipment. Low distortion and fast settling make them ideal for active filter applications.
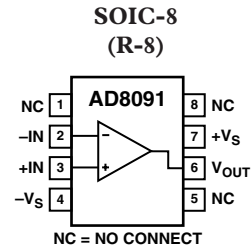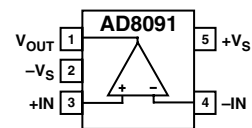
The AD8091/AD8092 offer a low-power supply current and can operate on a single +3 V power supply. These features are ideally suited for portable and battery-powered applications where size and power are critical.

The wide bandwidth and fast slew rate make these amplifiers useful in many general-purpose, high-speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed.

All of this low-cost performance is offered in an 8-lead SOIC (AD8091/AD8092), along with a tiny SOT23-5 package (AD8091) and a μSOIC package (AD8092).

REV. A

AD8091/AD8092–SPECIFICATIONS (@ T_A = 25°C, V_S = +5 V, R_L = 2 kΩ to +2.5 V, unless otherwise noted.)

Parameter	Conditions	AD8091A/AD8092A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = –1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p,				
	R_L = 150 Ω to +2.5 V,				
	R_F = 806 Ω		20		MHz
Slew Rate	G = –1, V_O = 2 V Step	100	145		V/μs
Full Power Response	G = +1, V_O = 2 V p-p		35		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		50		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion*	f_C = 5 MHz, V_O = 2 V p-p, G = +2		–67		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to +2.5 V		0.09		%
	R_L = 1 kΩ to +2.5 V		0.03		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to +2.5 V		0.19		Degrees
	R_L = 1 kΩ to +2.5 V		0.03		Degrees
Crosstalk	f = 5 MHz, G = +2		–60		dB
DC PERFORMANCE					
Input Offset Voltage			1.7	10	mV
	T_{MIN} to T_{MAX}			25	mV
Offset Drift			10		μV/°C
Input Bias Current			1.4	2.5	μA
	T_{MIN} to T_{MAX}			3.25	μA
Input Offset Current			0.1	0.75	μA
Open-Loop Gain	R_L = 2 kΩ to +2.5 V	86	98		dB
	T_{MIN} to T_{MAX}		96		dB
	R_L = 150 Ω to +2.5 V	76	82		dB
	T_{MIN} to T_{MAX}		78		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			–0.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to +3.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to +2.5 V		0.015 to 4.985		V
	R_L = 2 kΩ to +2.5 V	0.100 to 4.900	0.025 to 4.975		V
	R_L = 150 Ω to +2.5 V	0.300 to 4.625	0.200 to 4.800		V
Output Current	V_{OUT} = +0.5 V to +4.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short Circuit Current	Sourcing		80		mA
	Sinking		130		mA
Capacitive Load Drive	G = +1		50		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.4	5	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	70	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

*Refer to TPC 7.

Specifications subject to change without notice.

REV. A

SPECIFICATIONS (@ T_A = 25°C, V_S = +3 V, R_L = 2 kΩ to +1.5 V, unless otherwise noted.)

Parameter	Conditions	AD8091A/AD8092A			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = –1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p,				
	R_L = 150 Ω to 2.5 V,				
	R_F = 402 Ω		17		MHz
Slew Rate	G = –1, V_O = 2 V Step	90	135		V/μs
Full Power Response	G = +1, V_O = 1 V p-p		65		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion*	f_C = 5 MHz, V_O = 2 V p-p,				
	G = –1, R_L = 100 Ω to +1.5 V		–47		dB
Input Voltage Noise	f = 10 kHz		16		nV/√H̄z̄
Input Current Noise	f = 10 kHz		600		fA/√H̄z̄
Differential Gain Error (NTSC)	G = +2, V_{CM} = +1 V				
	R_L = 150 Ω to +1.5 V		0.11		%
	R_L = 1 kΩ to +1.5 V		0.09		%
Differential Phase Error (NTSC)	G = +2, V_{CM} = +1 V				
	R_L = 150 Ω to +1.5 V		0.24		Degrees
	R_L = 1 kΩ to +1.5 V		0.10		Degrees
Crosstalk	f = 5 MHz, G = +2		–60		dB
DC PERFORMANCE					
Input Offset Voltage			1.6	10	mV
	T_{MIN} to T_{MAX}			25	mV
Offset Drift			10		μV/°C
Input Bias Current			1.3	2.6	μA
	T_{MIN} to T_{MAX}			3.25	μA
Input Offset Current			0.15	0.8	μA
Open-Loop Gain	R_L = 2 kΩ	80	96		dB
	T_{MIN} to T_{MAX}		94		dB
	R_L = 150 Ω	74	82		dB
	T_{MIN} to T_{MAX}		76		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			–0.2 to +2.0		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to +1.5 V		0.01 to 2.99		V
	R_L = 2 kΩ to +1.5 V	0.075 to 2.9	0.02 to 2.98		V
	R_L = 150 Ω to +1.5 V	0.20 to 2.75	0.125 to 2.875		V
Output Current	V_{OUT} = +0.5 V to +2.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short Circuit Current	Sourcing		60		mA
	Sinking		90		mA
Capacitive Load Drive	G = +1		45		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.2	4.8	mA
Power Supply Rejection Ratio	ΔV_S = +0.5 V	68	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

*Refer to TPC 7.

Specifications subject to change without notice.

Parameter	Conditions	AD8091A/AD8092A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		MHz
	G = −1, +2, V_O = 0.2 V p-p		50		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p,				
	R_L = 150 Ω,				
	R_F = 1.1 kΩ		20		MHz
Slew Rate	G = −1, V_O = 2 V Step	105	170		V/μs
Full Power Response	G = +1, V_O = 2 V p-p		40		MHz
Settling Time to 0.1%	G = −1, V_O = 2 V Step		50		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2		−71		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.02		%
	R_L = 1 kΩ		0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.11		Degrees
	R_L = 1 kΩ		0.02		Degrees
Crosstalk	f = 5 MHz, G = +2		−60		dB
DC PERFORMANCE					
Input Offset Voltage			1.8	11	mV
	T_{MIN} to T_{MAX}			27	mV
Offset Drift			10		μV/°C
Input Bias Current			1.4	2.6	μA
	T_{MIN} to T_{MAX}			3.5	μA
Input Offset Current			0.1	0.75	μA
Open-Loop Gain	R_L = 2 kΩ	88	96		dB
	T_{MIN} to T_{MAX}		96		dB
	R_L = 150 Ω	78	82		dB
	T_{MIN} to T_{MAX}		80		dB
INPUT CHARACTERISTICS					
Input Resistance			290		kΩ
Input Capacitance			1.4		pF
Input Common-Mode Voltage Range			−5.2 to +4.0		V
Common-Mode Rejection Ratio	V_{CM} = −5 V to +3.5 V	72	88		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ		−4.98 to +4.98		V
	R_L = 2 kΩ	−4.85 to +4.85	−4.97 to +4.97		V
	R_L = 150 Ω	−4.45 to +4.30	−4.60 to +4.60		V
Output Current	V_{OUT} = −4.5 V to +4.5 V		45		mA
	T_{MIN} to T_{MAX}		45		mA
Short Circuit Current	Sourcing		100		mA
	Sinking		160		mA
Capacitive Load Drive	G = +1 (AD8091/AD8092)		50		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current/Amplifier			4.8	5.5	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	68	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . 12.6 V
Power Dissipation . . . . See Figure 1
Common-Mode Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . ± 2.5 V
Output Short Circuit Duration . . . . See Figure 1
Storage Temperature Range . . . . –65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause perma-
nent damage to the device. This is a stress rating only; functional operation of the
device at these or any other conditions above those indicated in the operational
section of this specification is not implied. Exposure to absolute maximum rating
conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8091/AD8092
package is limited by the associated rise in junction temperature
(T_J) on the die. The plastic encapsulating the die will locally reach
the junction temperature. At approximately 150°C, which is the
glass transition temperature, the plastic will change its properties.
Even temporarily exceeding this temperature limit may change the
stresses that the package exerts on the die, permanently shifting the
parametric performance of the AD8091/AD8092. Exceeding a
junction temperature of 175°C for an extended period of time can
result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package (θ_{JA}), ambient
temperature (T_A), and the total power dissipated in the package
(P_D) can be used to determine the junction temperature of the die.
The junction temperature can be calculated as follows:

$$T_J = T_A + \left(P_D \times \theta_{JA}\right)$$

The power dissipated in the package (P_D) is the sum of the quies-
cent power dissipation and the power dissipated in the package
due to the load drive for all outputs. The quiescent power is the
voltage between the supply pins (V_S) times the quiescent current
(I_S). Assuming the load (R_L) is referenced to midsupply, then the
total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in
the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference
between the total drive power and the load power is the drive
power dissipated in the package.

$$P_D = quiescent\ power + (total\ drive\ power - load\ power)$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \left(\frac{V_{OUT}^2}{R_L}\right)$$

RMS output voltages should be considered. (If R_L is referenced
to V_{S-}, as in single-supply operation, then the total drive power is
$V_S \times I_{OUT}$.)

If the rms signal levels are indeterminate, then consider the
worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = \left(V_S \times I_S\right) + \frac{\left(\frac{V_S}{4}\right)^2}{R_L}$$

(In single-supply operation with R_L referenced to V_{S-}, worst case is
$V_{OUT} = V_S/2$.)

Airflow will increase heat dissipation, effectively reducing θ_{JA}. Also,
more metal directly in contact with the package leads from metal
traces, through holes, ground, and power planes will reduce the θ_{JA}.
Care must be taken to minimize parasitic capacitances at the input
leads of high-speed op amps as discussed in the board layout
section.

Figure 1 shows the maximum safe power dissipation in the package
versus the ambient temperature for the SOIC-8 (125°C/W),
SOT23-5 (180°C/W), and μSOIC-8 (150°C/W) packages on a
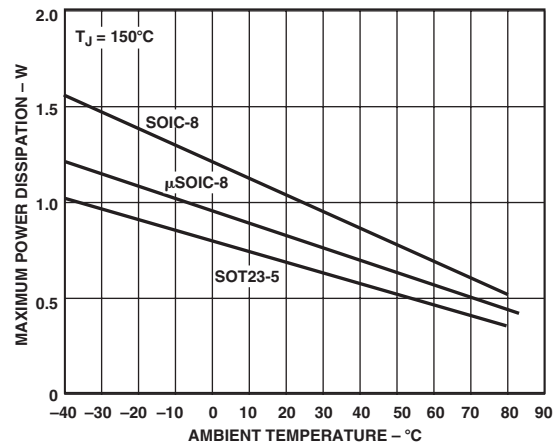JEDEC standard four-layer board.

Figure 1. Maximum Power Dissipation vs. Temperature
for a Four-Layer Board

AD8091/AD8092

Model	Temperature Range	Package Description	Package Outline	Branding Information
AD8091AR	−40°C to +85°C	8-Lead SOIC	SO-8	
AD8091AR-REEL	−40°C to +85°C	8-Lead SOIC	13" Tape and Reel	
AD8091AR-REEL7	−40°C to +85°C	8-Lead SOIC	7" Tape and Reel	
AD8091ART-REEL	−40°C to +85°C	5-Lead SOT-23	RT-5, 13" Tape and Reel	HVA
AD8091ART-REEL7	−40°C to +85°C	5-Lead SOT-23	RT-5, 7" Tape and Reel	HVA
AD8092AR	−40°C to +85°C	8-Lead SOIC	SO-8	
AD8092AR-REEL	−40°C to +85°C	8-Lead SOIC	13" Tape and Reel	
AD8092AR-REEL7	−40°C to +85°C	8-Lead SOIC	7" Tape and Reel	
AD8092ARM	−40°C to +85°C	8-Lead μSOIC	RM-8	HWA
AD8092ARM-REEL	−40°C to +85°C	8-Lead μSOIC	13" Tape and Reel	HWA
AD8092ARM-REEL7	−40°C to +85°C	8-Lead μSOIC	7" Tape and Reel	HWA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8091/AD8092 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

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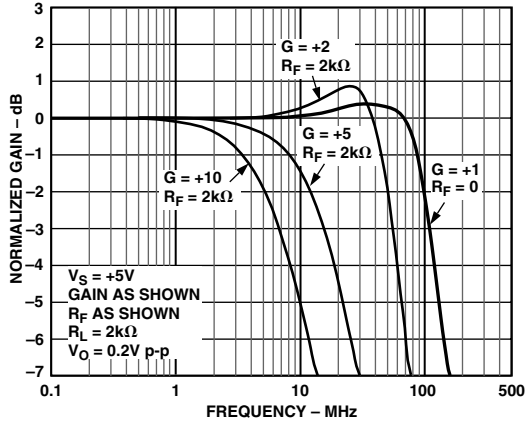
TPC 1. Normalized Gain vs. Frequency; V_S = +5 V
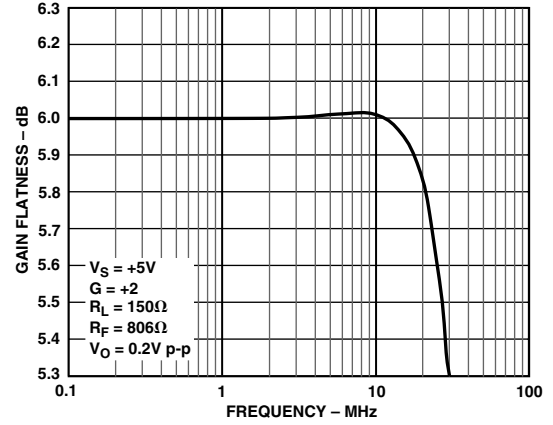
TPC 4. 0.1 dB Gain Flatness vs. Frequency; G = +2
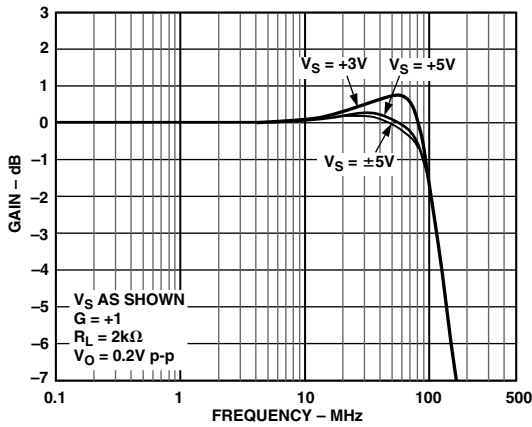
TPC 2. Gain vs. Frequency vs. Supply
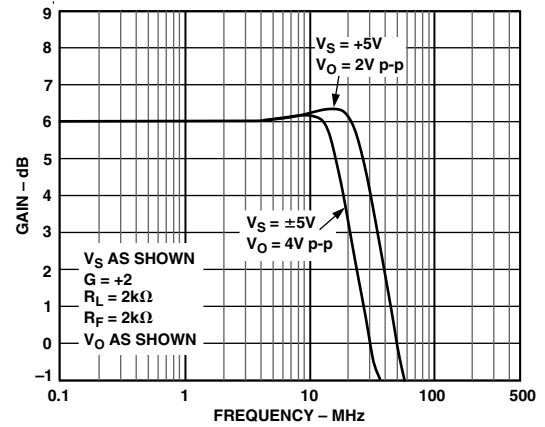
TPC 5. Large Signal Frequency Response; G = +2
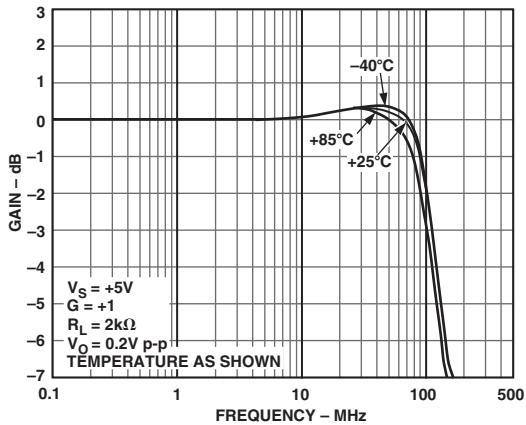
TPC 3. Gain vs. Frequency vs. Temperature
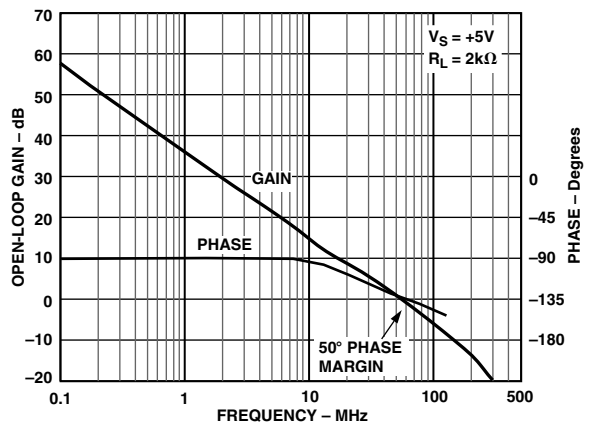
TPC 6. Open-Loop Gain and Phase vs. Frequency

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AD8091/AD8092
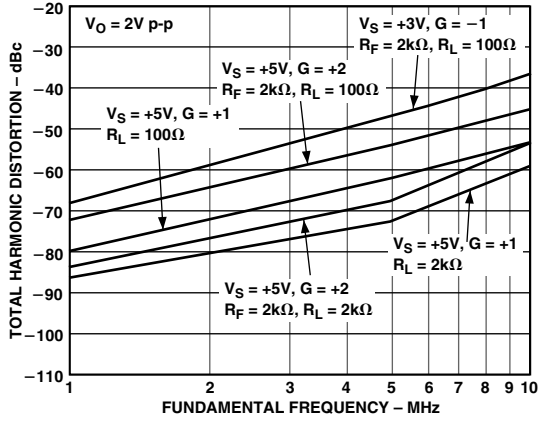
TPC 7. Total Harmonic Distortion
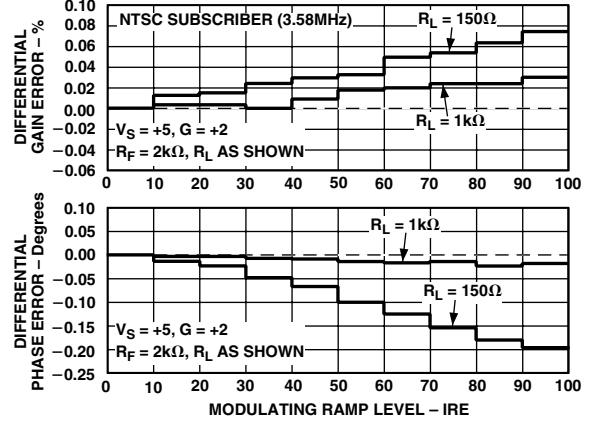
TPC 10. Differential Gain and Phase Errors
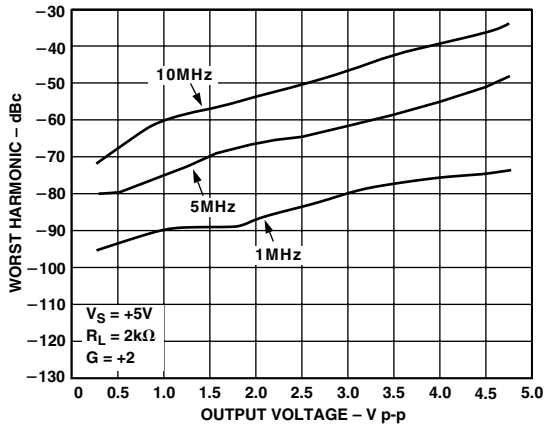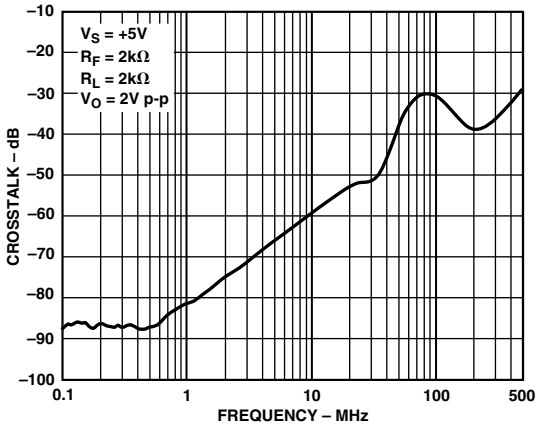

TPC 8. Worst Harmonic vs. Output Voltage
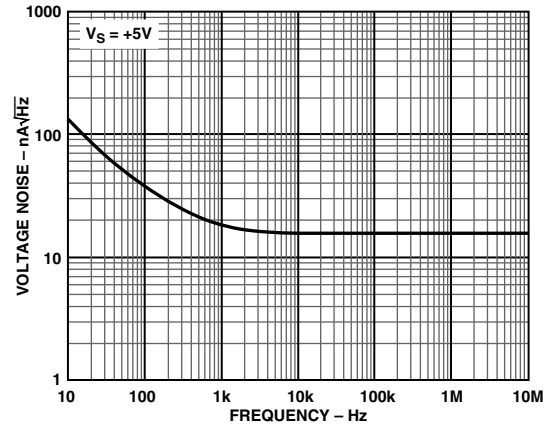
TPC 11. Input Voltage Noise vs. Frequency
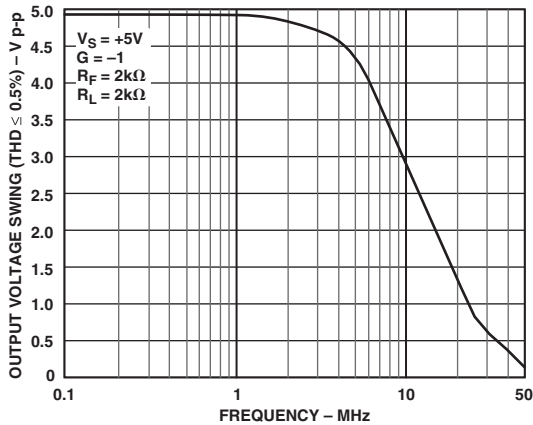
TPC 9. Low Distortion Rail-to-Rail Output Swing
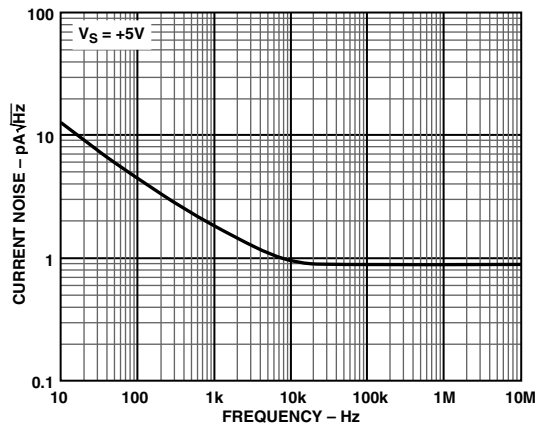
TPC 12. Input Current Noise vs. Frequency

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TPC 13. AD8092 Crosstalk (Output-to-Output) vs. Frequency
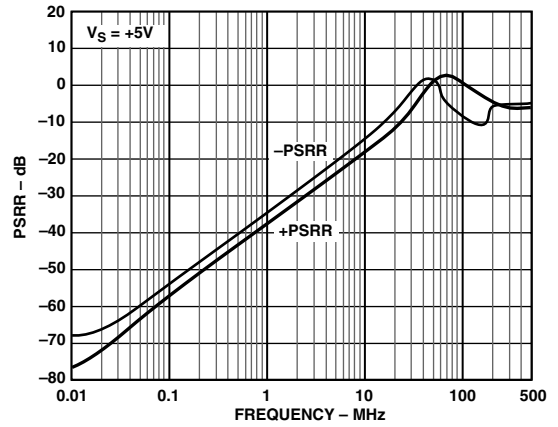
TPC 16. PSRR vs. Frequency
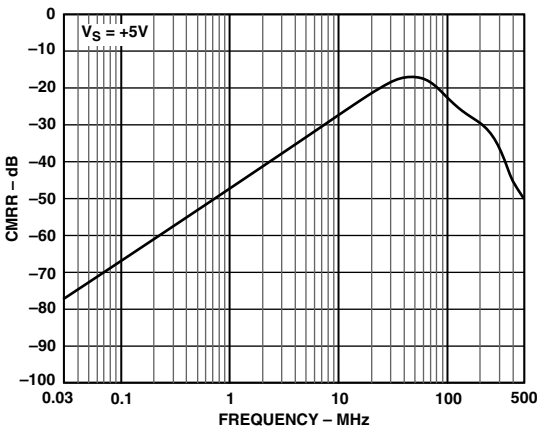
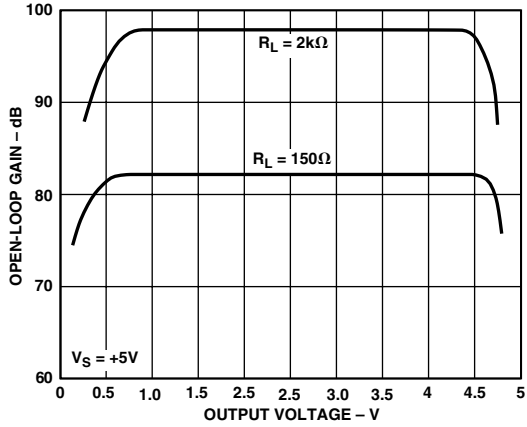TPC 14. CMRR vs. Frequency
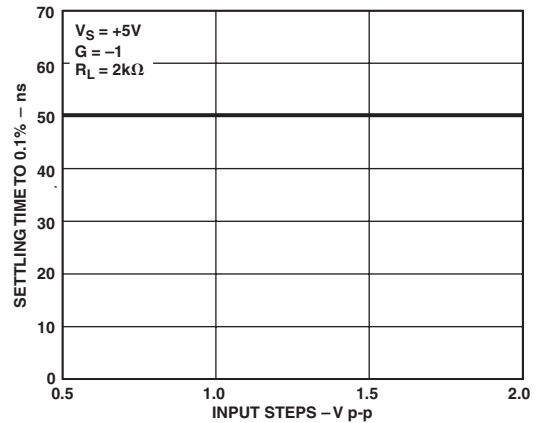
TPC 17. Settling Time vs. Input Step
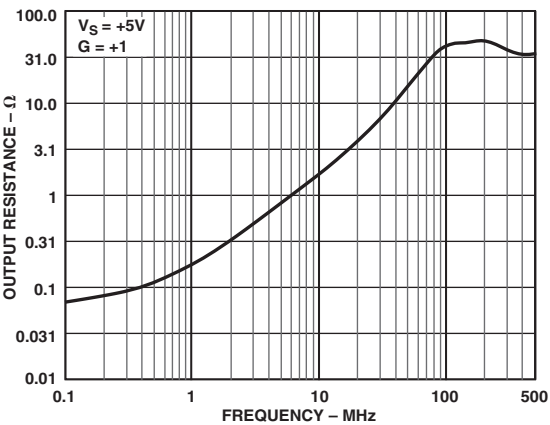
TPC 15. Closed-Loop Output Resistance vs. Frequency
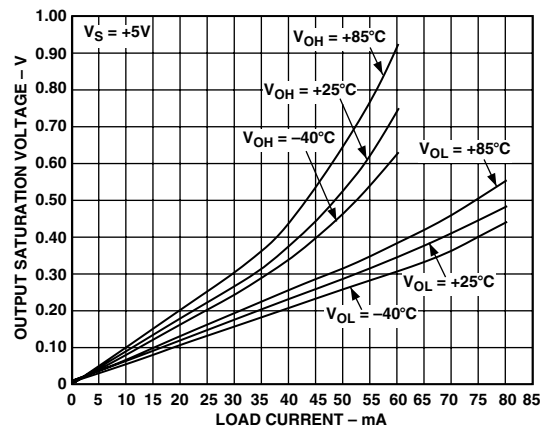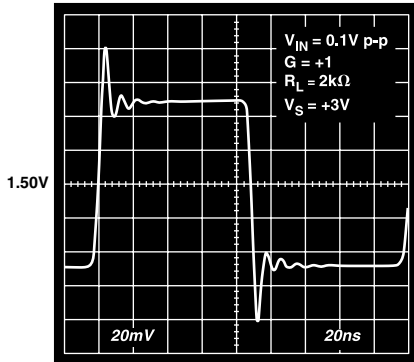

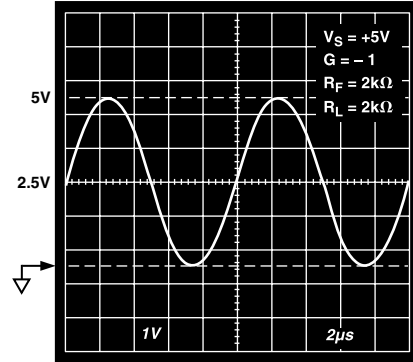TPC 18. Output Saturation Voltage vs. Load Current
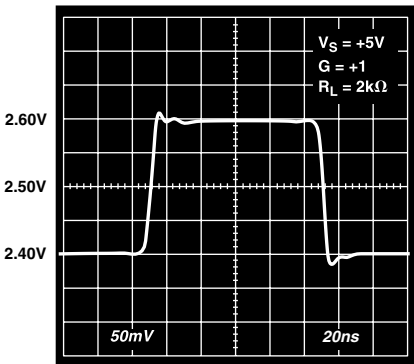
AD8091/AD8092

TPC 19. Open-Loop Gain vs. Output Voltage
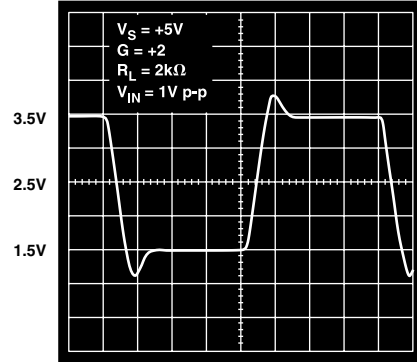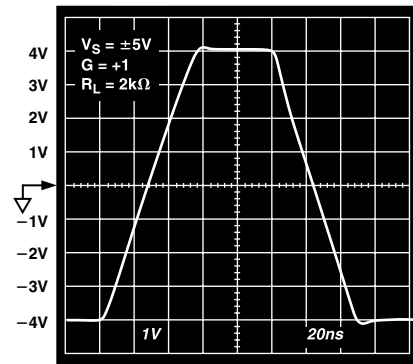

TPC 22. Large Signal Step Response; V_S = +5 V, G = +2

TPC 20. 100 mV Step Response; G = +1

TPC 23. Output Swing; G = –1, R_L = 2 kΩ

TPC 21. 200 mV Step Response; V_S = +5 V, G = +1

TPC 24. Large Signal Step Response; V_S = ±5 V, G = +1

REV. A

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Power Supply Bypassing

Power supply pins are actually inputs and care must be taken so that a noise-free stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering a majority of the noise.

Decoupling schemes are designed to minimize the bypassing imped-ance at all frequencies with a parallel combination of capacitors. 0.01 µF or 0.001 µF (X7R or NPO) chip capacitors are critical and should be as close as possible to the amplifier package. Larger chip capacitors, such as the 0.1 µF capacitor, can be shared among a few closely spaced active components in the same signal path. A 10 µF tantalum capacitor is less critical for high-frequency bypassing and, in most cases, only one per board is needed at the supply inputs.

Grounding

A ground plane layer is important in densely packed PC boards to spread the current minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high-speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high-frequency impedance of the path. High-speed currents in an inductive ground return will create an unwanted voltage noise.

The length of the high-frequency bypass capacitor leads are most critical. A parasitic inductance in the bypass grounding will work against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location. Because load currents flow from the supplies as well, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

Input Capacitance

Along with bypassing and ground, high-speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few pF of capacitance will reduce the input impedance at high frequencies, in turn increasing the amplifier's gain, causing peaking of the frequency response or even oscillations, if severe enough. It is recommended that the external passive components, which are connected to the input pins, be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

Input-to-Output Coupling

The input and output signal traces should not be parallel to mini-mize capacitive coupling between the inputs and output, avoiding any positive feedback.

DRIVING CAPACITIVE LOADS

A highly capacitive load will react with the output of the amplifiers, causing a loss in phase margin and subsequent peaking or even oscillation, as illustrated in Figures 2 and 3. There are two methods to effectively minimize its effect.

1. Put a small value resistor in series with the output to isolate the load capacitor from the amps' output stage.

2. Increase the phase margin with higher noise gains or by adding a pole with a parallel resistor and capacitor from –IN to the output.
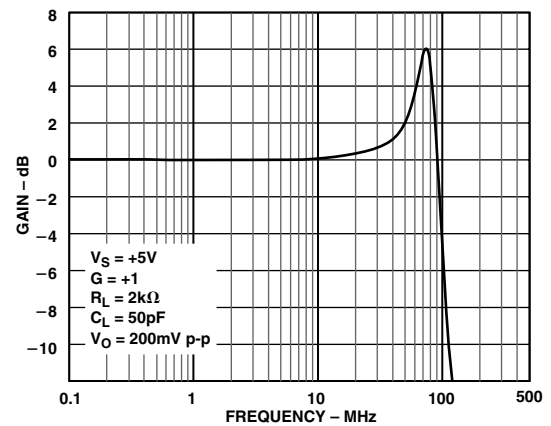

Figure 2. Closed-Loop Frequency Response: C_L = 50 pF

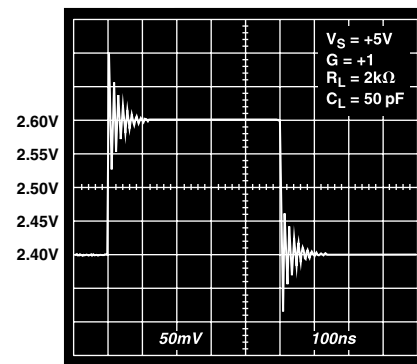

Figure 3. 200 mV Step Response: C_L = 50 pF

AD8091/AD8092

As the closed-loop gain is increased, the larger phase margin allows for large capacitor loads with less peaking. Adding a low value resistor in series with the load at lower gains has the same effect. Figure 4 shows the effect of a series resistor for various voltage gains. For large capacitive loads, the frequency response of the amplifier will be dominated by the series resistor and capacitive load.
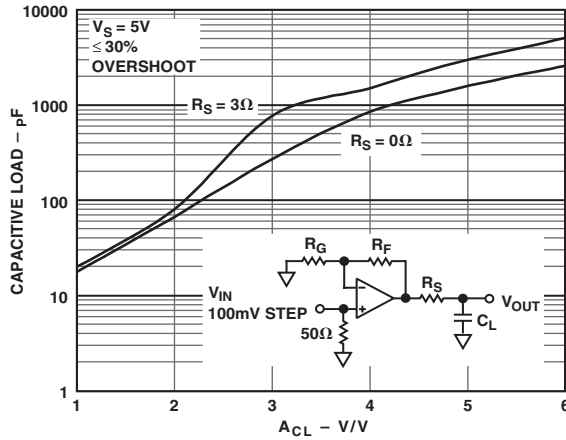

Figure 4. Capacitive Load Drive vs. Closed-Loop Gain

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 5, the AD8091/AD8092 recovers within 60 ns from negative overdrive and within 45 ns from positive overdrive.
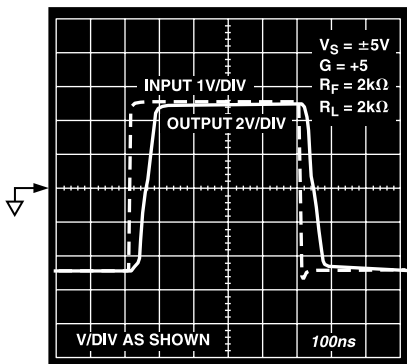

Figure 5. Overdrive Recovery

Active Filters

Active filters at higher frequencies require wider bandwidth op amps to work effectively. Excessive phase shift produced by lower frequency op amps can significantly impact active filter performance.

Figure 6 shows an example of a 2 MHz biquad bandwidth filter that uses three op amps. Such circuits are sometimes used in medical ultrasound systems to lower the noise bandwidth of the analog signal before A/D conversion. Please note that the unused amplifiers' inputs should be tied to ground.
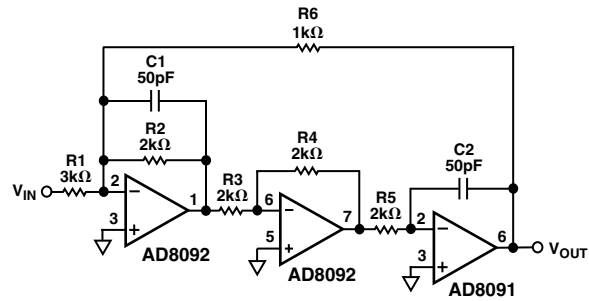

Figure 6. 2 MHz Biquad Band-Pass Filter

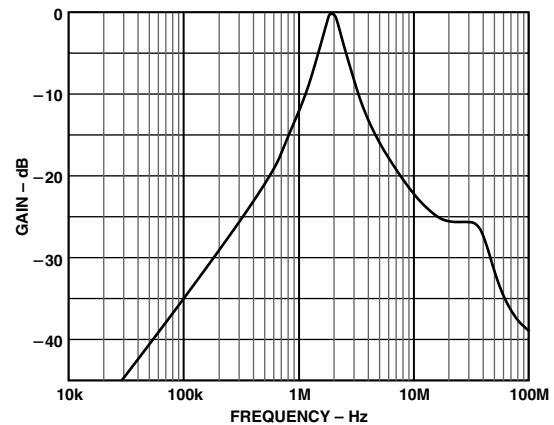The frequency response of the circuit is shown in Figure 7.

Figure 7. Frequency Response of 2 MHz Band-Pass Biquad Filter

Sync Stripper

Synchronizing pulses are sometimes carried on video signals so as not to require a separate channel to carry the synchronizing information. However, for some functions, such as A/D conversion, it is not desirable to have the sync pulses on the video signal. These

pulses will reduce the dynamic range of the video signal and do not provide any useful information for such a function.

A sync stripper will remove the synchronizing pulses from a video signal while passing all the useful video information. Figure 8 shows a practical single-supply circuit that uses only a single AD8091. It is capable of directly driving a reverse terminated video line.
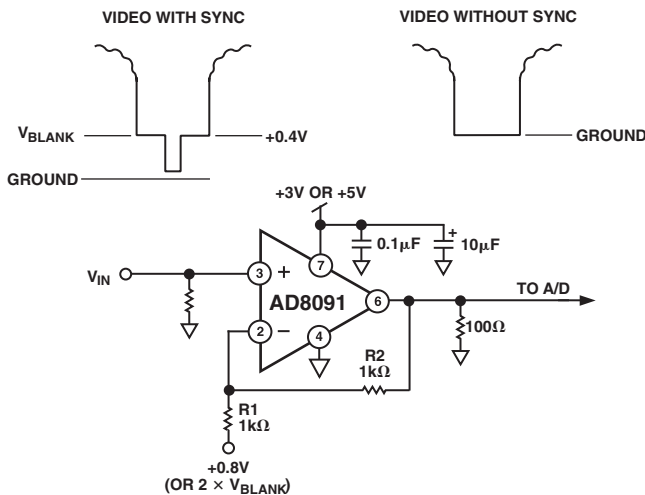

Figure 8. Sync Stripper

The video signal plus sync is applied to the noninverting input with the proper termination. The amplifier gain is set equal to 2 via the two 1 kΩ resistors in the feedback circuit. A bias voltage must be applied to R1 for the input signal to have the sync pulses stripped at the proper level.

The blanking level of the input video pulse is the desired place to remove the sync information. This level is multiplied by 2 by the amplifier. This level must be at ground at the output in order for the sync stripping action to take place. Since the gain of the amplifier from the input of R1 to the output is −1, a voltage equal to $2 \times V_{BLANK}$ must be applied to make the blanking level come out at ground.

Single-Supply Composite Video Line Driver
Many composite video signals have their blanking level at ground and have video information that is both positive and negative. Such signals require dual-supply amplifiers to pass them. However, by ac level shifting, a single-supply amplifier can be used to pass these signals. The following complications may arise from such techniques.

Signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capacity than their (bounded) peak-to-peak amplitude after they are ac-coupled. As a worst case, the dynamic signal swing will approach twice the peak-to-peak value. The two conditions that define the maximum dynamic swing requirements are a signal that is mostly low but goes high with a duty cycle that is a small fraction of a percent. The opposite condition defines the other extreme.

The worst case of composite video is not quite this demanding. One bounding condition is a signal that is mostly black for an entire frame but has a white (full amplitude) minimum width spike at least once in a frame.

The other extreme is a full white video signal. The blanking intervals and sync tips of such a signal will have negative-going excursions in compliance with the composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at the highest (white) level for a maximum of about 75% of the time.

As a result of the duty cycles between the two extremes presented above, a 1 V p-p composite video signal that is multiplied by a gain of 2 requires about 3.2 V p-p of dynamic voltage swing at the output for an op amp to pass a composite video signal of arbitrary varying duty cycle without distortion.

Some circuits use a sync tip clamp to hold the sync tips at a relatively constant level to lower the amount of dynamic signal swing required. However, these circuits can have artifacts like sync tip compression unless they are driven by a source with a very low output impedance. The AD8091/AD8092 have adequate signal swing when running on a single +5 V supply to handle an ac-coupled composite video signal.

The input to the circuit in Figure 9 is a standard composite (1 V p-p) video signal that has the blanking level at ground. The input network level shifts the video signal by means of ac-coupling. The noninverting input of the op amp is biased to half of the supply voltage.
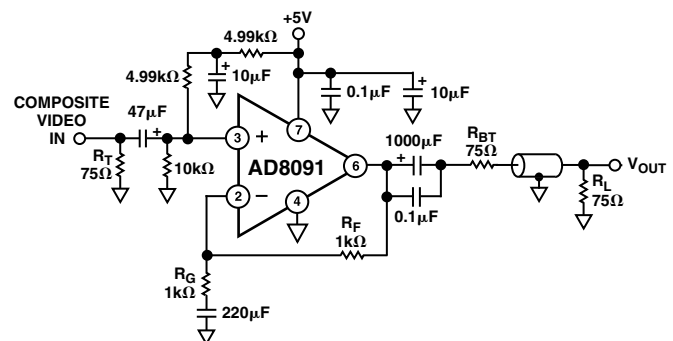

*Figure 9. Single-Supply Composite Video Line Driver*

The feedback circuit provides unity gain for the dc biasing of the input and provides a gain of 2 for any signals that are in the video bandwidth. The output is ac-coupled and terminated to drive the line.

The capacitor values were selected for providing minimum "tilt" or field time distortion of the video signal. These values would be required for video that is considered to be studio or broadcast quality. However, if a lower consumer grade of video, sometimes referred to as "consumer video," is all that is desired, the values and the cost of the capacitors can be reduced by as much as a factor of 5 with minimum visible degradation in the picture.
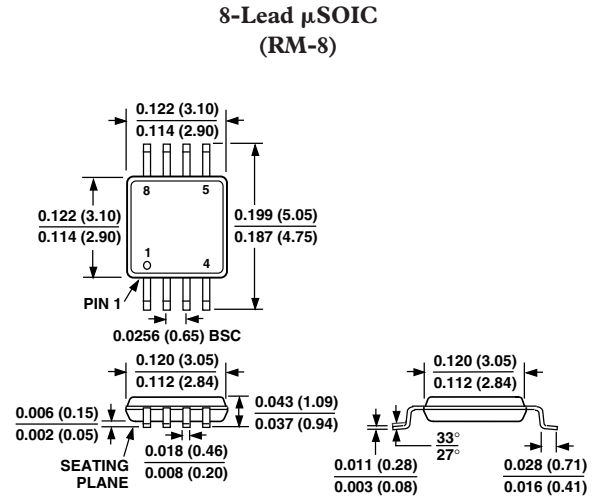
AD8091/AD8092

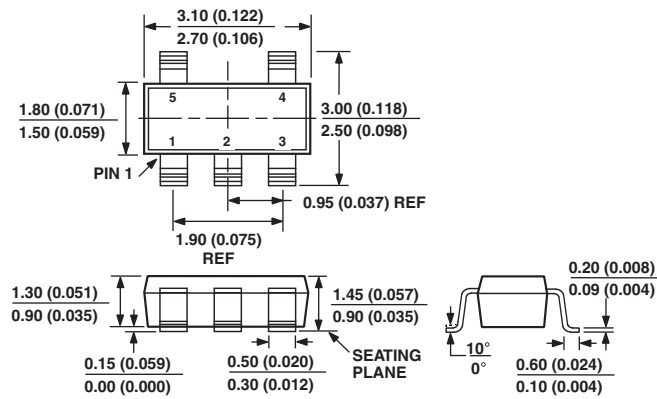**OUTLINE DIMENSIONS**

Dimensions shown in mm and (inches)
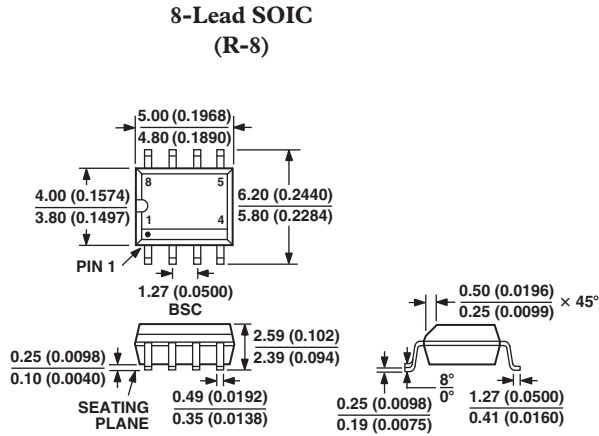
Dimensions shown in inches and (mm)

8-Lead SOIC
(R-8)

8-Lead μSOIC
(RM-8)

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Dimensions shown in mm and (inches)

5-Lead Plastic Surface Mount
(RT-5)

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

REV. A

Revision History