ANALOG DEVICES

Xstream™ 3.2 Gbps Quad Buffer Mux/Demux

AD8159

FEATURES

- Port level 2:1 mux/1:2 demux
- Each port consists of 4 lanes
- Each lane runs from dc to 3.2 Gbps, independent of the other lanes
- Compensates over 40 inches of FR4 at 3.2 Gbps through two levels of input equalization, or four levels of output pre-emphasis
- Accepts ac- or dc-coupled differential CML inputs
- Low deterministic jitter, typically 20 ps p-p
- Low random jitter, typically 1 ps rms
- BER < 10^{-16}
- On-chip termination
- Reversible inputs and outputs on one port
- Unicast or bicast on 1:2 demux function
- Port level loopback capability
- Single lane switching capability
- 3.3 V core supply
- Flexible I/O supply down to 2.5 V
- Low power, typically 1 W in basic configuration
- 100-pin TQFP_EP
- –40°C to +85°C operating temperature range

APPLICATIONS

- Low cost redundancy switch
- SONET OC48/SDH16 and lower data rates
- XAUI (10 Gigabit Ethernet) over backplane
- Gigabit Ethernet over backplane
- Fibre channel 1.06 Gbps and 2.125 Gbps over backplane
- Infiniband over backplane
- PCI-Express over backplane

FUNCTIONAL BLOCK DIAGRAM

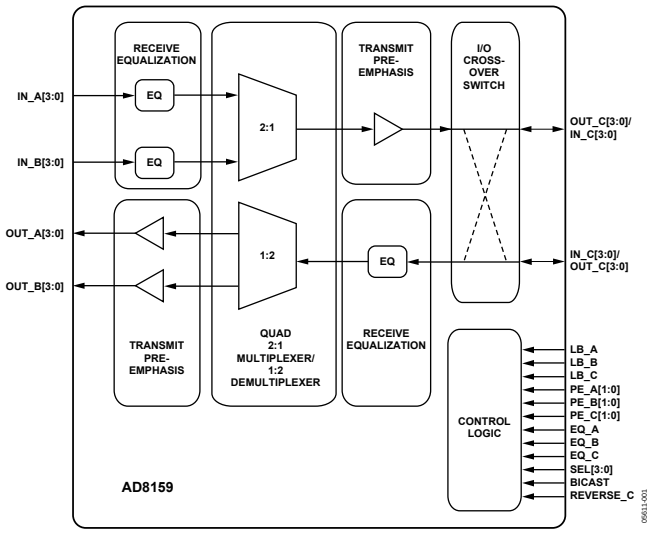

Figure 1.

GENERAL DESCRIPTION

The AD8159 is an asynchronous, protocol agnostic, quad-lane 2:1 switch with a total of 12 differential PECL/CML-compatible inputs and 12 differential CML outputs. The operation of this product is optimized for NRZ signaling with data rates up to 3.2 Gbps per lane. Each lane offers two levels of input equalization and four levels of output pre-emphasis.

The AD8159 consists of four multiplexers and four demultiplexers, one per lane. Each port is a 4-lane link, and each lane runs up to a 3.2 Gbps data rate independent of the other lanes. The lanes are switched independently using the four select pins, SEL[3:0]; each select pin controls one lane of the port. The AD8159 has low latency and very low lane-to-lane skew.

The main application of the AD8159 is to support redundancy on both the backplane side and the line interface side of a serial link. The device has unicast and bicast capability, so it is configurable to support either 1 + 1 or 1:1 redundancy.

The AD8159 supports reversing the output and input pins on one of its ports, which helps to connect two ASICs with opposite pinouts.

The AD8159 is also used for testing high speed serial links by duplicating incoming data and sending it to the destination port and to test equipment simultaneously.

Rev. A

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9/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = +3.3 V, V_{EE} = 0 V, R_L = 50 Ω, basic configuration,[1] data rate= 3.2 Gbps, input common-mode voltage = 2.7 V, differential input swing = 800 mV p-p, @ T_A = +25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate/Channel (NRZ)		DC		3.2	Gbps
Deterministic Jitter	Data rate = 3.2 Gbps; see Figure 21		20		ps p-p
Random Jitter	RMS; see Figure 24		1		ps
Propagation Delay	Input to output		600		ps
Lane-to-Lane Skew			100		ps
Switching Time			5		ns
Output Rise/Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential, $V_{ICM} = V_{CC} - 0.6$ V;[2] see Figure 22	200		2000	mV p-p
Input Voltage Range	Common mode, V_{ID} = 800 mV p-p;[3] see Figure 25	V_{EE} + 1.8		V_{CC} + 0.3	V
Input Bias Current			4		µA
Input Capacitance			2		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, PE = 0		800		mV p-p
Output Voltage Range	Single-ended absolute voltage level; see Figure 26	V_{CC} − 1.6		V_{CC} + 0.6	V
Output Current	Port A/B, PE_A/B = 0		16		mA
	Port C, PE_C = 0		20		mA
	Port A/B, PE_A/B = 3		28		mA
	Port C, PE_C = 3		32		mA
Output Capacitance			2		pF
TERMINATION CHARACTERISTICS					
Resistance	Differential	90	100	110	Ω
Temperature Coefficient			0.15		Ω/°C
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	3.0	3.3	3.6	V
Supply Current	Basic configuration[1], dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far end terminations				
I_{CC}			175		mA
$I_{I/O} = I_{TTO} + I_{TTOI} + I_{TTI} + I_{TTIO}$			144		mA
Supply Current	BICAST = 1, PE = 3 on all ports, dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far end terminations				
I_{CC}			255		mA
$I_{I/O} = I_{TTO} + I_{TTOI} + I_{TTI} + I_{TTIO}$			352		mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		−40		+85	°C
θ_{JA}	Still air		29		°C/W
θ_{JB}	Still air		16		°C/W
θ_{JC}	Still air		13		°C/W
LOGIC INPUT CHARACTERISTICS					
Input High (V_{IH})		2.4		V_{CC}	V
Input Low (V_{IL})		V_{EE}		0.8	V

[1] Bicast off, loopback off on all ports, pre-emphasis off on all ports, equalization set to minimum on all ports.
[2] V_{ICM} = input common-mode voltage.
[3] V_{ID} = input differential peak-to-peak voltage swing.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTIO}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
V_{TTOI}	V_{CC} + 0.6 V
Internal Power Dissipation	4.26 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

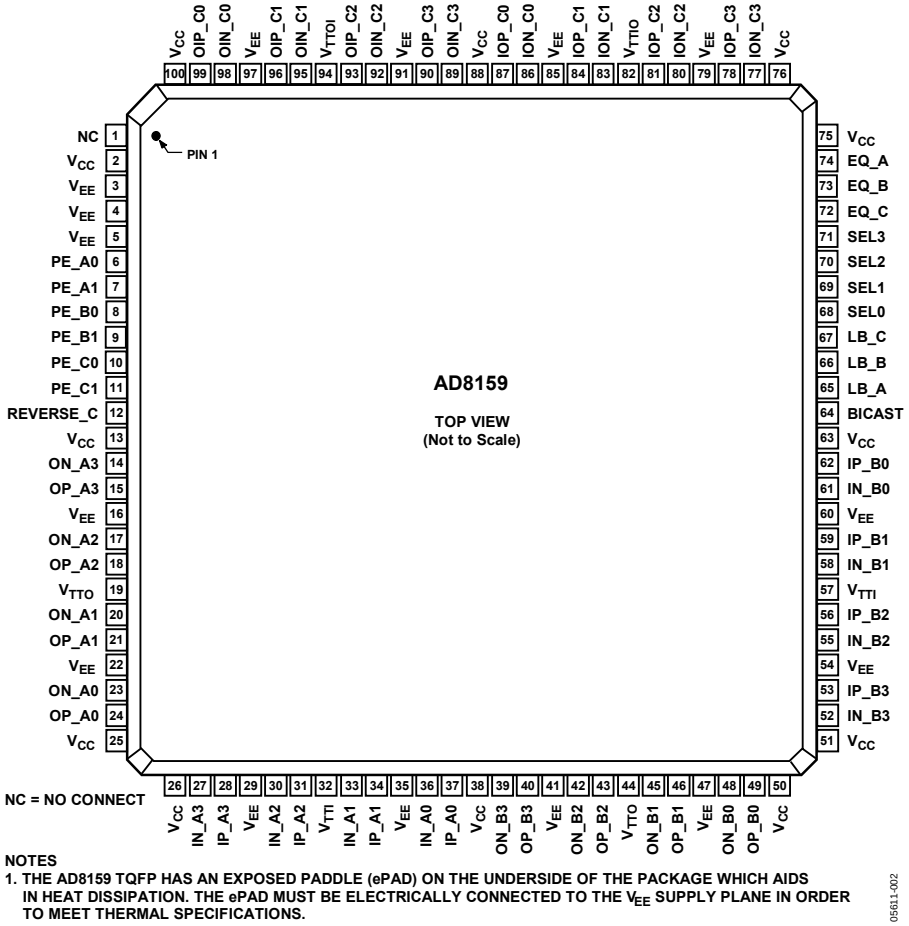


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	NC	N/A	No connect
2, 13, 25, 26, 38, 50, 51, 63, 75, 76, 88, 100	V_{CC}	Power	Positive supply
3 to 5, 16, 22, 29, 35, 41, 47, 54, 60, 79, 85, 91, 97	V_{EE}	Power	Negative supply
6	PE_A0	Control	Pre-emphasis control for Port A (LSB)
7	PE_A1	Control	Pre-emphasis control for Port A (MSB)
8	PE_B0	Control	Pre-emphasis control for Port B (LSB)
9	PE_B1	Control	Pre-emphasis control for Port B (MSB)
10	PE_C0	Control	Pre-emphasis control for Port C (LSB)
11	PE_C1	Control	Pre-emphasis control for Port C (MSB)
12	REVERSE_C	Control	Reverse inputs and outputs on Port C
14	ON_A3	I/O	High speed output complement
15	OP_A3	I/O	High speed output
17	ON_A2	I/O	High speed output complement
18	OP_A2	I/O	High speed output
19, 44	V_{TTO}	Power	Port A and Port B output termination supply
20	ON_A1	I/O	High speed output complement
21	OP_A1	I/O	High speed output
23	ON_A0	I/O	High speed output complement
24	OP_A0	I/O	High speed output
27	IN_A3	I/O	High speed input complement

Pin No.	Mnemonic	Type	Description
28	IP_A3	I/O	High speed input
30	IN_A2	I/O	High speed input complement
31	IP_A2	I/O	High speed input
32, 57	V_{TTI}	Power	Port A and Port B input termination supply
33	IN_A1	I/O	High speed input complement
34	IP_A1	I/O	High speed input
36	IN_A0	I/O	High speed input complement
37	IP_A0	I/O	High speed input
39	ON_B3	I/O	High speed output complement
40	OP_B3	I/O	High speed output
42	ON_B2	I/O	High speed output complement
43	OP_B2	I/O	High speed output
45	ON_B1	I/O	High speed output complement
46	OP_B1	I/O	High speed output
48	ON_B0	I/O	High speed output complement
49	OP_B0	I/O	High speed output
52	IN_B3	I/O	High speed input complement
53	IP_B3	I/O	High speed input
55	IN_B2	I/O	High speed input complement
56	IP_B2	I/O	High speed input
58	IN_B1	I/O	High speed input complement
59	IP_B1	I/O	High speed input
61	IN_B0	I/O	High speed input complement
62	IP_B0	I/O	High speed input
64	BICAST	Control	Bicast enable
65	LB_A	Control	Loopback enable for Port A
66	LB_B	Control	Loopback enable for Port B
67	LB_C	Control	Loopback enable for Port C
68	SEL0	Control	$\overline{A}$/B select for Lane 0
69	SEL1	Control	$\overline{A}$/B select for Lane 1
70	SEL2	Control	$\overline{A}$/B select for Lane 2
71	SEL3	Control	$\overline{A}$/B select for Lane 3
72	EQ_C	Control	Equalization control for Port C
73	EQ_B	Control	Equalization control for Port B
74	EQ_A	Control	Equalization control for Port A
77	ION_C3	I/O	High speed input/output complement
78	IOP_C3	I/O	High speed input/output
80	ION_C2	I/O	High speed input/output complement
81	IOP_C2	I/O	High speed input/output
82	V_{TTIO}	Power	Port C input/output termination supply
83	ION_C1	I/O	High speed input/output complement
84	IOP_C1	I/O	High speed input/output
86	ION_C0	I/O	High speed input/output complement
87	IOP_C0	I/O	High speed input/output
89	OIN_C3	I/O	High speed output/input complement
90	OIP_C3	I/O	High speed output/input
92	OIN_C2	I/O	High speed output/input complement
93	OIP_C2	I/O	High speed output/input
94	V_{TTOI}	Power	Port C output/input termination supply
95	OIN_C1	I/O	High speed output/input complement
96	OIP_C1	I/O	High speed output/input
98	OIN_C0	I/O	High speed output/input complement
99	OIP_C0	I/O	High speed output/input

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +3.3 V, V_{EE} = 0 V, R_L = 50 Ω, basic configuration, data rate = 3.2 Gbps, input common-mode voltage = 2.7 V, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted.

Note: All graphs were generated using the setup shown in Figure 32, unless otherwise specified.

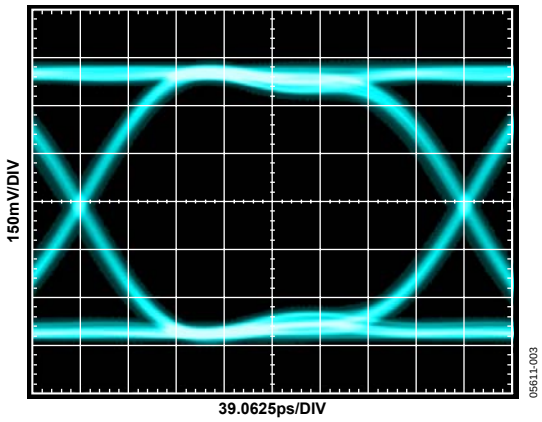


Figure 3. Output Port A Eye Diagram 3.2 Gbps Input Port A or Input Port C

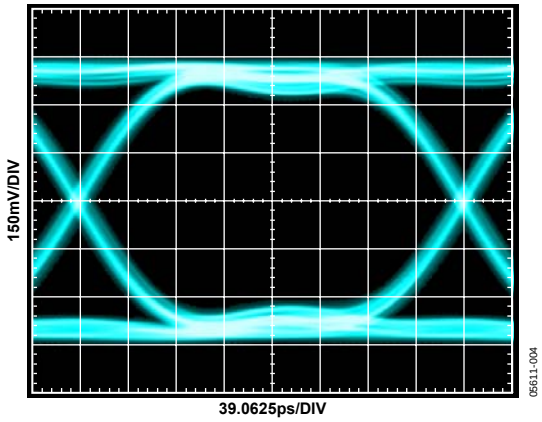


Figure 4. Output Port B Eye Diagram Input Port B or Input Port C

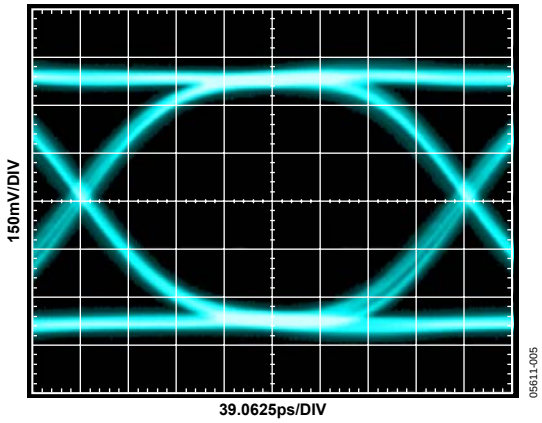


Figure 5. Output Port C Eye Diagram 3.2 Gbps Input Port A or Input Port B

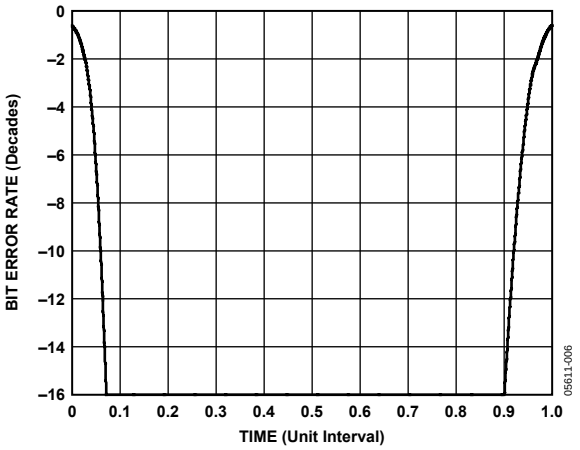


Figure 6. Output Port A Bathtub Curve 3.2 Gbps

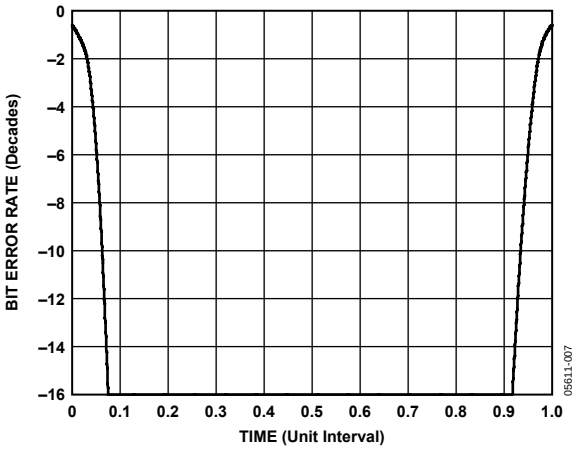


Figure 7. Output Port B Bathtub Curve 3.2 Gbps

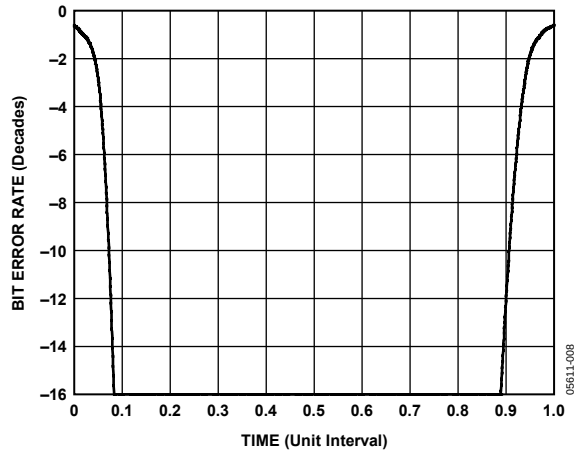


Figure 8. Output Port C Bathtub Curve 3.2 Gbps

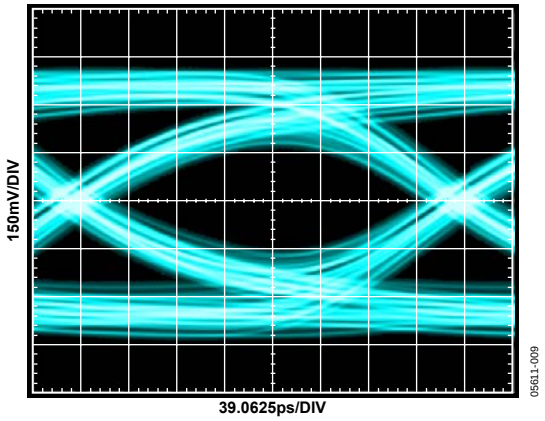


Figure 9. Eye Diagram over Backplane
(18" FR4 + 2 GbX Connectors), PE = 0

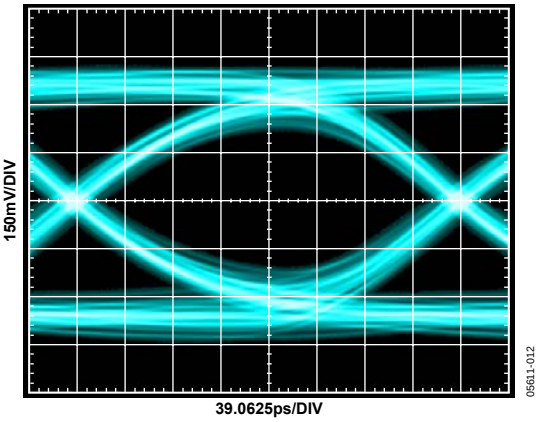


Figure 12. Eye Diagram over Backplane
(18" FR4 + 2 GbX Connectors), PE = 1

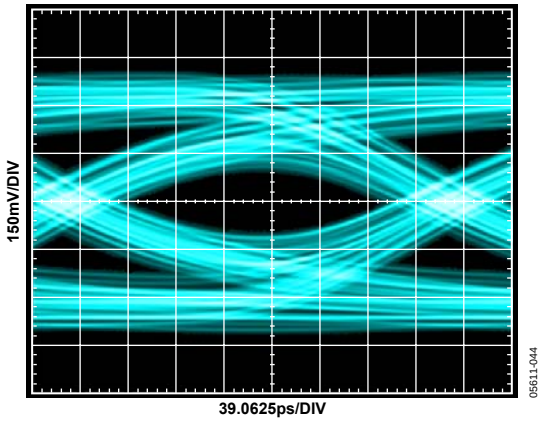


Figure 10. Eye Diagram over Backplane
(30" FR4 + 2 GbX Connectors), PE = 0

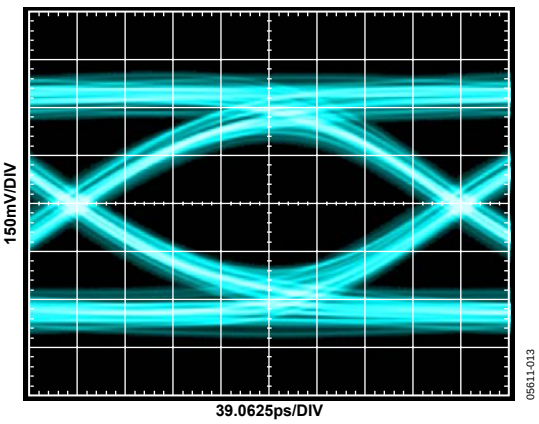


Figure 13. Eye Diagram over Backplane
(30" FR4 + 2 GbX Connectors), PE = 2

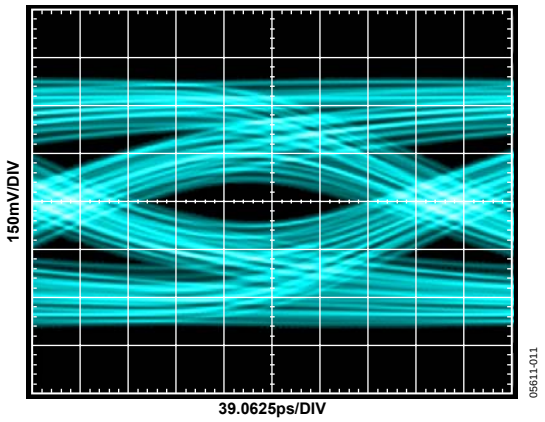


Figure 11. Eye Diagram over Backplane
(36" FR4 + 2 GbX Connectors), PE = 0

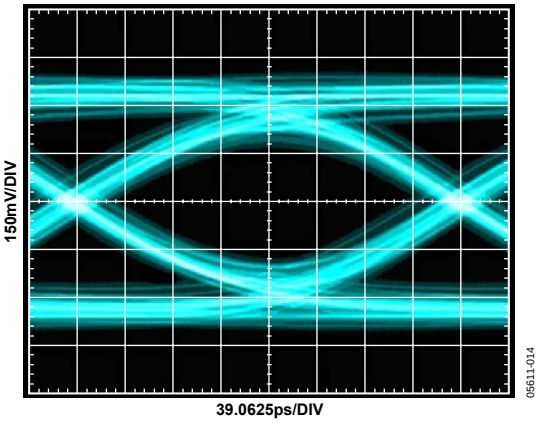


Figure 14. Eye Diagram over Backplane
(36" FR4 + 2 GbX Connectors), PE = 3

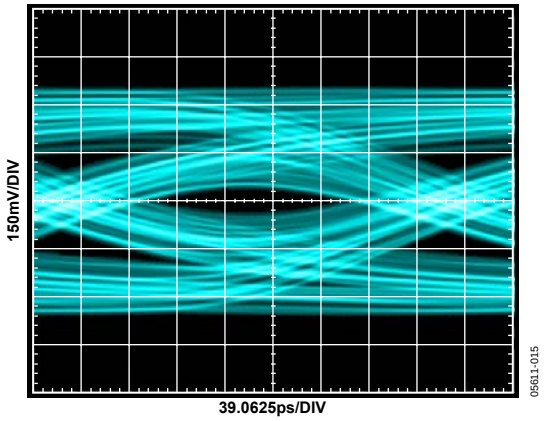


Figure 15. Eye Diagram over Backplane
(42" FR4 + 2 GbX Connectors), PE = 0

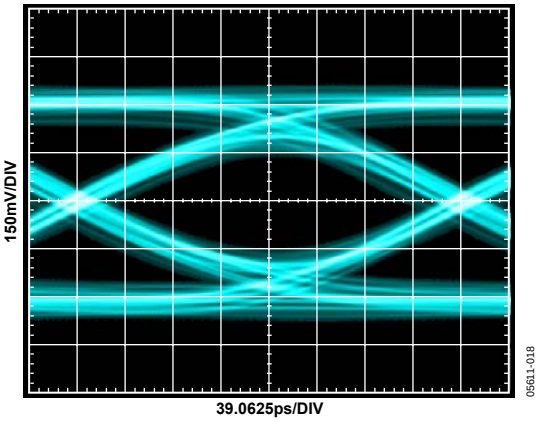


Figure 18. Eye Diagram over Backplane
(42" FR4 + 2 GbX Connectors), PE = 3

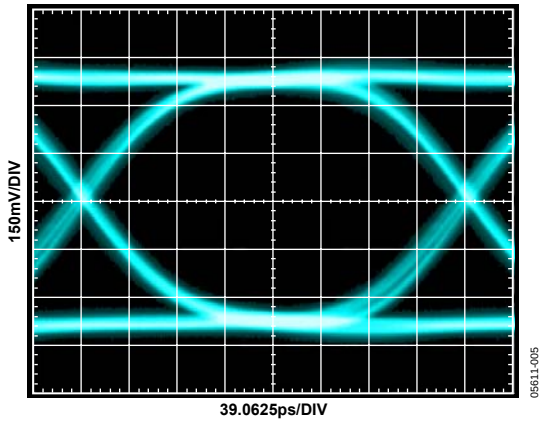


Figure 16. Reference Eye Diagram for Figure 19

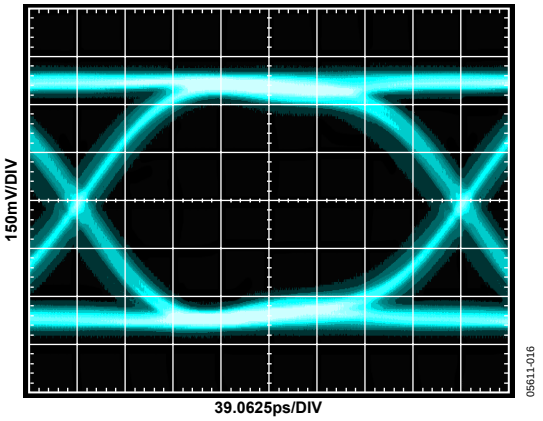


Figure 19. Eye Diagram with Equalization
(10" FR4), EQ = 0
Note: See Figure 34 for Test Circuit Used

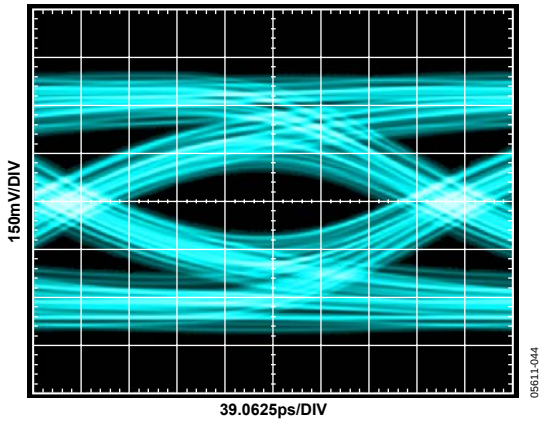


Figure 17. Reference Eye Diagram for Figure 20

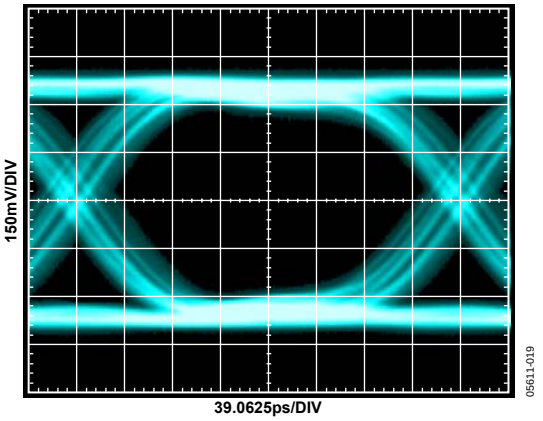


Figure 20. Eye Diagram with Equalization
(34" FR4 + 2 GbX Connectors), EQ = 1
Note: See Figure 34 for Test Circuit Used

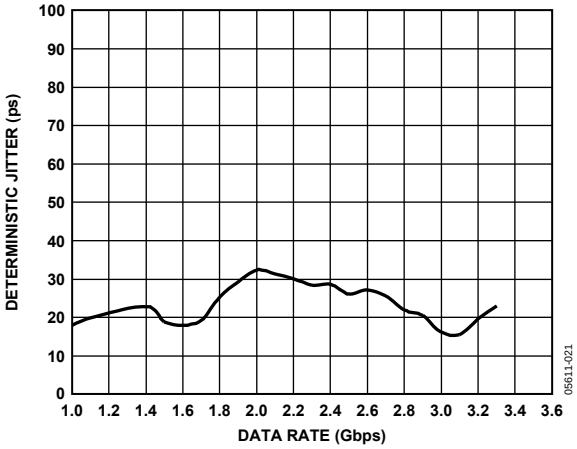


Figure 21. Deterministic Jitter vs. Data Rate

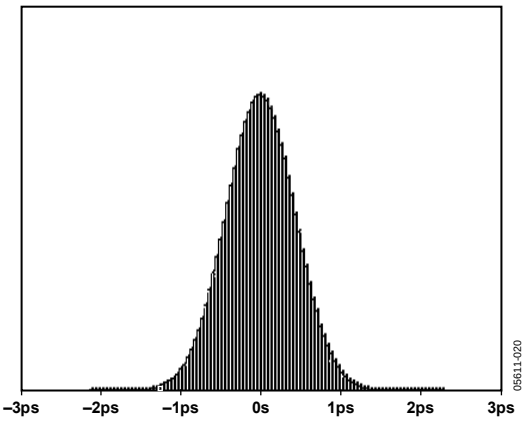


Figure 24. Random Jitter Histogram
Note: See Figure 35 for Test Circuit Used

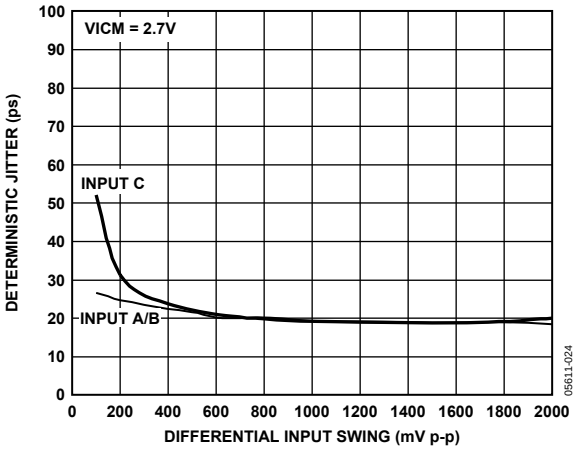


Figure 22. Deterministic Jitter vs. Differential Input Swing

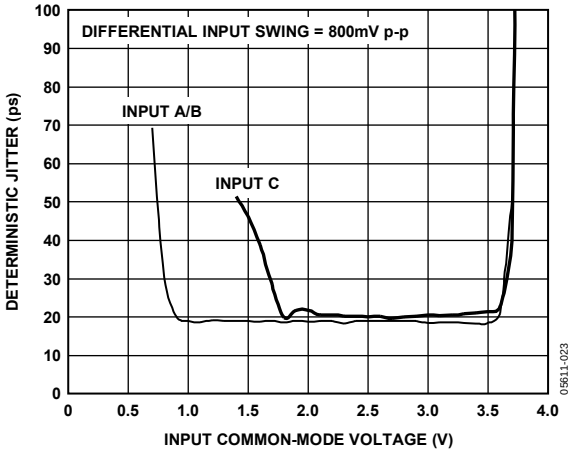


Figure 25. Deterministic Jitter vs. Input Common-Mode Voltage

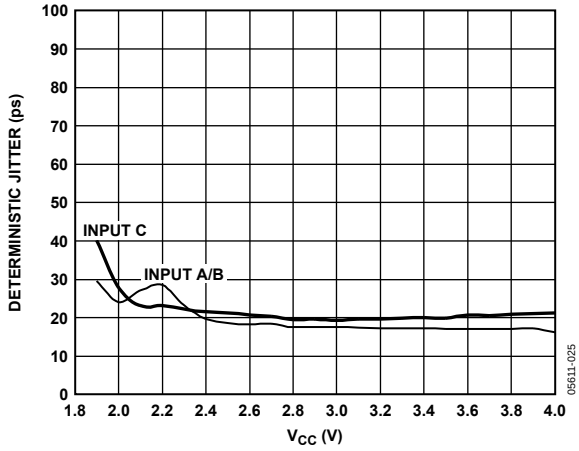


Figure 23. Deterministic Jitter vs. Core Supply Voltage

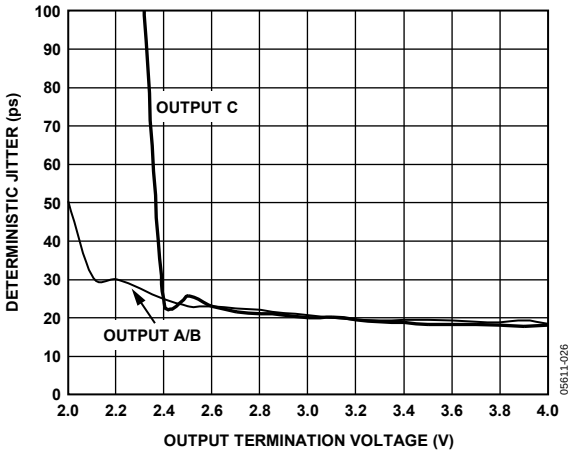


Figure 26. Deterministic Jitter vs. Output Termination Voltage

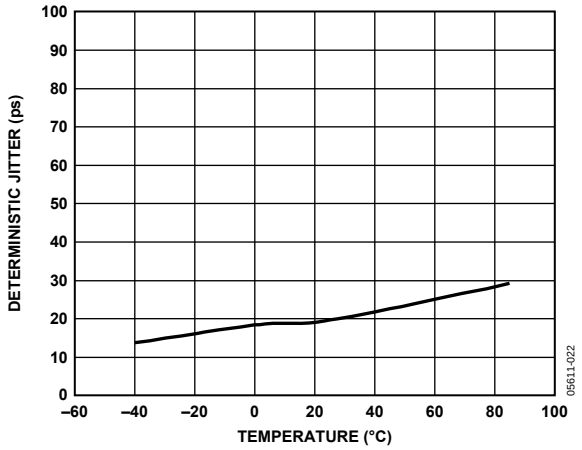


Figure 27. Deterministic Jitter vs. Temperature

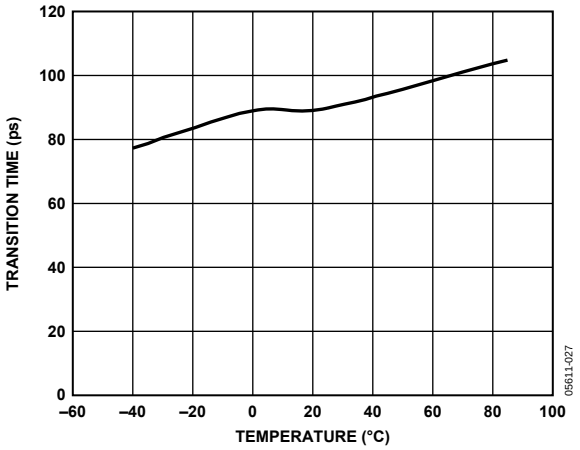


Figure 28. Transition Time vs. Temperature
Note: See Figure 33 for Test Circuit Used

EVALUATION BOARD SIMPLIFIED BLOCK DIAGRAMS

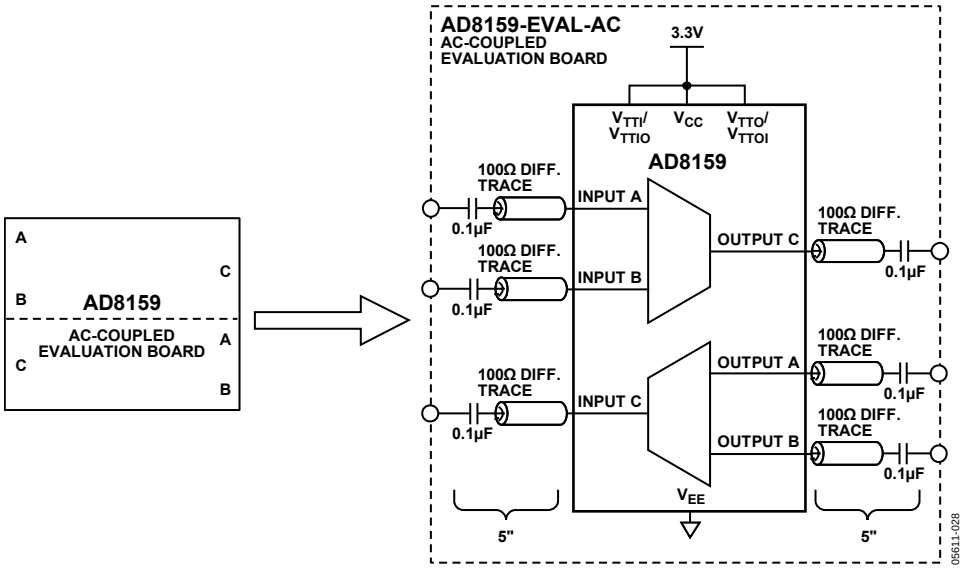


Figure 29. AC-Coupled Evaluation Board Simplified Block Diagram

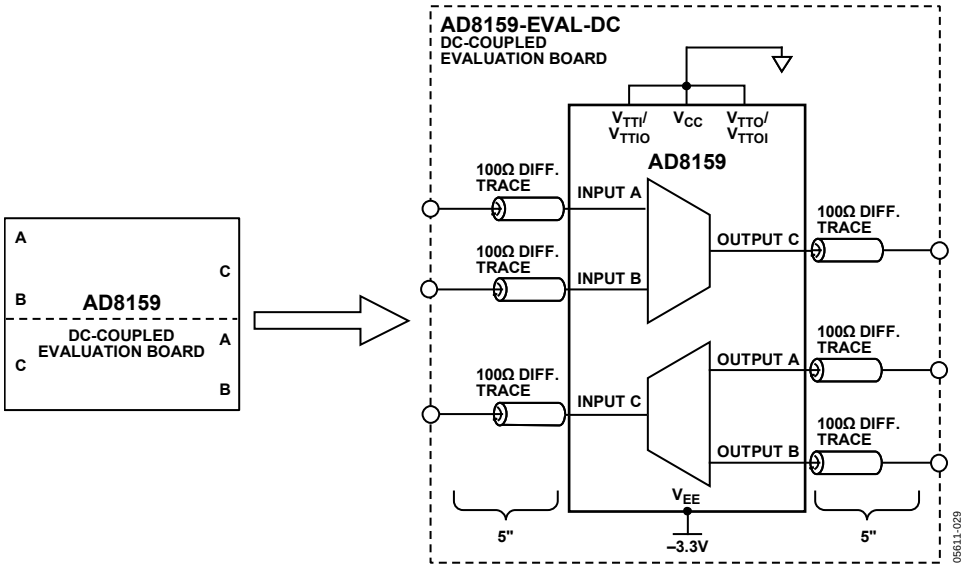


Figure 30. DC-Coupled Evaluation Board Simplified Block Diagram

TEST CIRCUITS

All graphs were generated using the setup shown in Figure 32, unless otherwise specified.

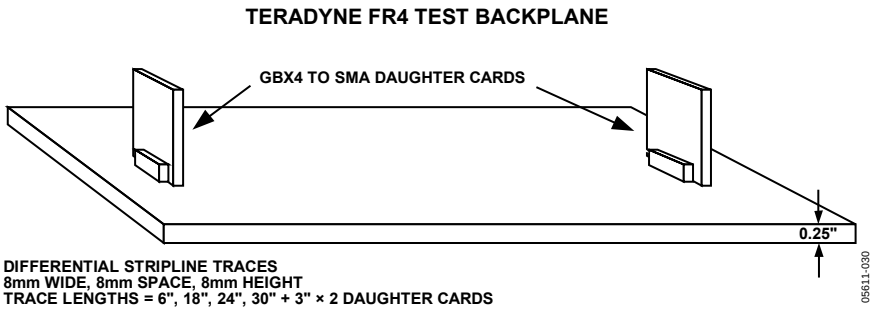


Figure 31. Test Backplane

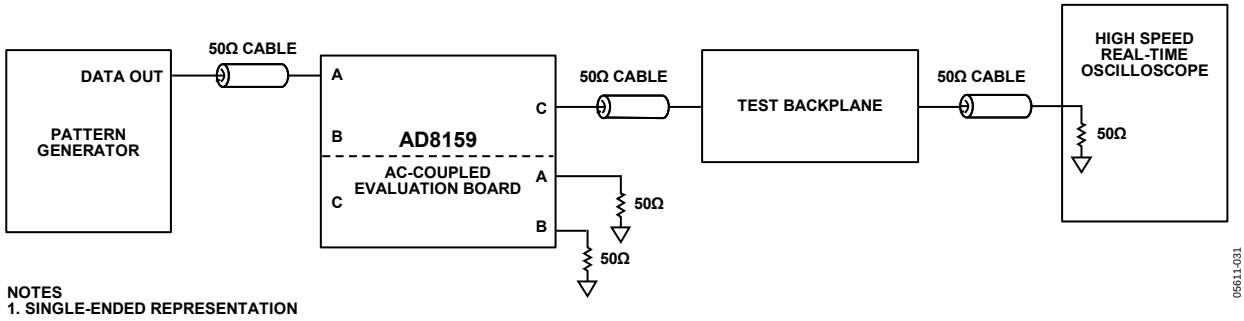


Figure 32. AC-Coupled Test Circuit

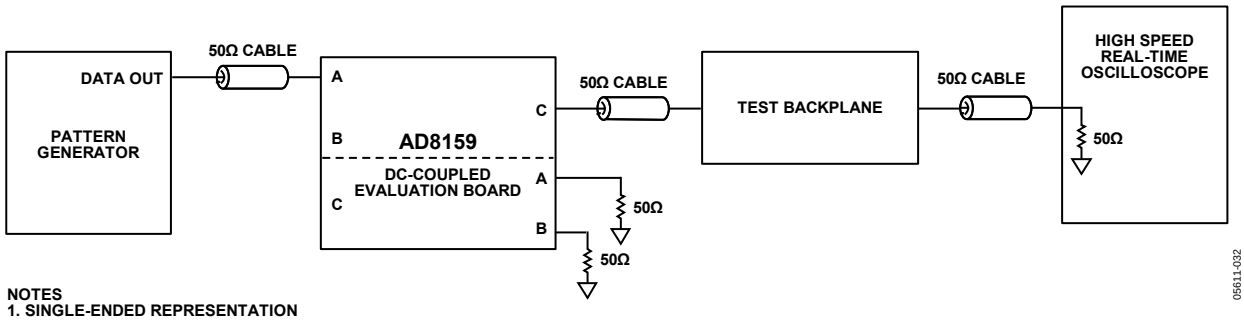


Figure 33. DC-Coupled Test Circuit
Note: Test Circuit Used for Figure 28

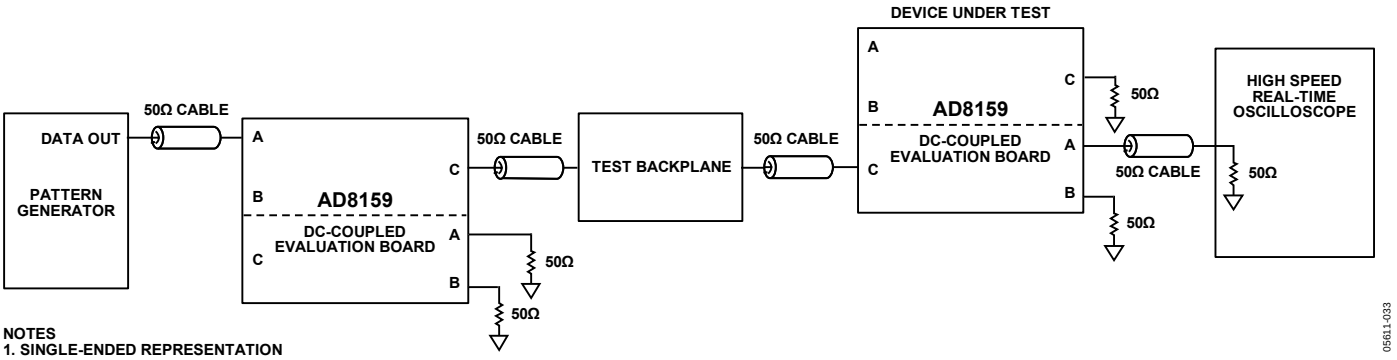


Figure 34. Equalization Test Circuit
Note: Test Circuit Used for Figure 19 and Figure 20

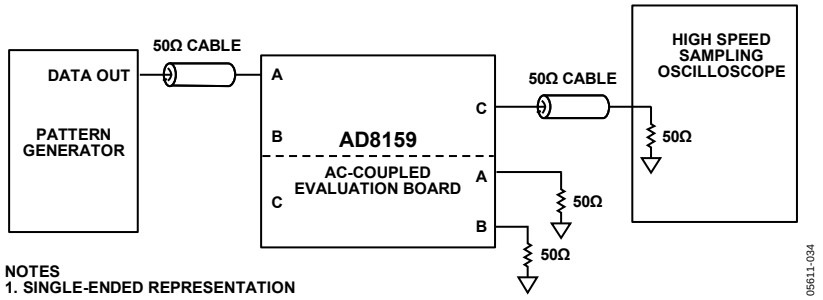


Figure 35. Random Jitter Test Circuit
Note: Test Circuit Used for Figure 24

THEORY OF OPERATION

The AD8159 relays received data on the demultiplexer Input Port C to Output Port A and/or Output Port B, depending on the mode selected by the BICAST control pin. On the multiplexer side, the AD8159 relays received data on either Input Port A or Input Port B to Output Port C, based on the SEL[3:0] pin states.

The AD8159 is configured by toggling control pins. On the demultiplexer side, when the device is configured in the unicast mode, it sends the received data on Input Port C to Output Port A or Output Port B. When the device is configured in the bicast mode, received data on Input Port C is sent to both Output Port A and Output Port B.

On the multiplexer side, only received data on Input Port A or Input Port B is sent to Output Port C, depending on the state of the SEL[3:0] pins. Table 4 summarizes port selection and configuration when loopback is disabled (LB_A = LB_B = LB_C = 0).

When the device is in unicast mode, the output lanes on either Port A or Port B are in an *idle* state. In the *idle* state, the output tail current is set to 0, and the P and N sides of the lane are pulled up to the output termination voltage through the on-chip termination resistors.

Table 4. Port Selection and Configuration Table

SEL	BICAST	OUT_A	OUT_B	OUT_C
0	0	IN_C	Idle	IN_A
0	1	IN_C	IN_C	IN_A
1	0	Idle	IN_C	IN_B
1	1	IN_C	IN_C	IN_B

INPUT EQUALIZATION (EQ) AND OUTPUT PRE-EMPHASIS (PE)

In backplane applications, the AD8159 needs to compensate for signal degradation over potentially long traces. The device supports two levels of input equalization, configured on a per-port basis. **Table 6** to **Table 8** summarize the high-frequency gain (EQ) for each control setting as well as the typical length of backplane trace that can be compensated for each setting.

The AD8159 also has four levels of output pre-emphasis, configured for each port. The pre-emphasis circuitry adds a controlled amount of overshoot to the output waveform to compensate for the loss in a backplane trace.

Table 9 to Table 11 summarize the high-frequency gain, amount of overshoot, and the typical backplane channel length (including two connectors) that can be compensated using each setting. A typical backplane is made of FR4 material with 8 mil wide trace and 8 mil spacing loosely coupled differential traces. Each backplane channel consists of two connectors. The total length of the channel includes three inches of traces on each card.

Table 5. Port C I/O Selection

Port C Pin List on 100-Lead TQFP	Port C when REVERSE_C = 0		Port C when REVERSE_C = 1	
	Pin Name	Input/Output	Pin Name	Input/Output
77	ION_C3 = INN_C3	Input pin	ION_C3 = OUTN_C3	Output pin
78	IOP_C3 = INP_C3	Input pin	IOP_C3 = OUTP_C3	Output pin
80	ION_C2 = INN_C2	Input pin	ION_C2 = OUTN_C2	Output pin
81	IOP_C2 = INP_C2	Input pin	IOP_C2 = OUTP_C2	Output pin
83	ION_C1 = INN_C1	Input pin	ION_C1 = OUTN_C1	Output pin
84	IOP_C1 = INP_C1	Input pin	IOP_C1 = OUTP_C1	Output pin
86	ION_C0 = INN_C0	Input pin	ION_C0 = OUTN_C0	Output pin
87	IOP_C0 = INP_C0	Input pin	IOP_C0 = OUTP_C0	Output pin
89	OIN_C3 = OUTN_C3	Output pin	OIN_C3 = INN_C3	Input pin
90	OIP_C3 = OUTP_C3	Output pin	OIP_C3 = INP_C3	Input pin
92	OIN_C2 = OUTN_C2	Output pin	OIN_C2 = INN_C2	Input pin
93	OIP_C2 = OUTP_C2	Output pin	OIP_C2 = INP_C2	Input pin
95	OIN_C1 = OUTN_C1	Output pin	OIN_C1 = INN_C1	Input pin
96	OIP_C1 = OUTP_C1	Output pin	OIP_C1 = INP_C1	Input pin
98	OIN_C0 = OUTN_C0	Output pin	OIN_C0 = INN_C0	Input pin
99	OIP_C0 = OUTP_C0	Output pin	OIP_C0 = INP_C0	Input pin

Table 6. IN_C Port Input Equalization Settings

EQ_C	EQ	Typical Backplane Length
0	6 dB	0 to 20 inches
1	12 dB	20 to 40+ inches

Table 7. IN_A Port Input Equalization Settings

EQ_A	EQ	Typical Backplane Length
0	6 dB	0 to 20 inches
1	12 dB	20 to 40+ inches

Table 8. IN_B Port Input Equalization Settings

EQ_B	EQ	Typical Backplane Length
0	6 dB	0 to 20 inches
1	12 dB	20 to 40+ inches

Table 9. OUT_C Port Output Pre-Emphasis Settings

PE_C[1]	PE_C[0]	PE	Overshoot	Typical Backplane Length
0	0	0 dB	0%	0 to 10 inches
0	1	1.9 dB	15%	10 to 20 inches
1	0	3.5 dB	35%	20 to 30 inches
1	1	4.9 dB	60%	30 to 40+ inches

Table 10. OUT_A Port Output Pre-Emphasis Settings

PE_A[1]	PE_A[0]	PE	Overshoot	Typical Backplane Length
0	0	0 dB	0%	0 to 10 inches
0	1	1.9 dB	15%	10 to 20 inches
1	0	3.5 dB	35%	20 to 30 inches
1	1	4.9 dB	60%	30 to 40+ inches

Table 11. OUT_B Port Output Pre-Emphasis Settings

PE_B[1]	PE_B[0]	PE	Overshoot	Typical Backplane Length
0	0	0 dB	0%	0 to 10 inches
0	1	1.9 dB	15%	10 to 20 inches
1	0	3.5 dB	35%	20 to 30 inches
1	1	4.9 dB	60%	30 to 40+ inches

LOOPBACK

The AD8159 also supports port level loopback, illustrated in Figure 36. The loopback control pins override the lane select (SEL[3:0]) and bicast control (BICAST) pins. Table 12 summarizes the different loopback configurations.

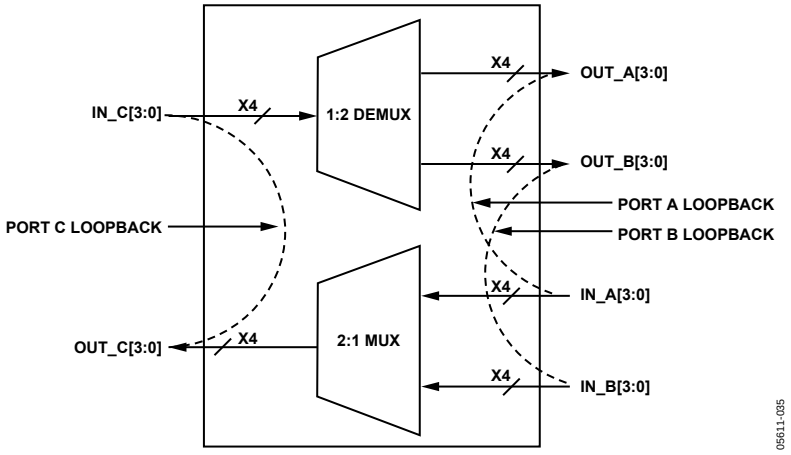


Figure 36. Port-Based Loopback Capability

Table 12. Loopback, Bicast, and Port Select Settings[1]

LB_A	LB_B	LB_C	SEL	BICAST	OUT_A	OUT_B	OUT_C
0	0	0	0	0	IN_C	Idle	IN_A
0	0	0	0	1	IN_C	IN_C	IN_A
0	0	0	1	0	Idle	IN_C	IN_B
0	0	0	1	1	IN_C	IN_C	IN_B
0	0	1	0	0	IN_C	Idle	IN_C
0	0	1	X	1	IN_C	IN_C	IN_C
0	0	1	1	0	Idle	IN_C	IN_C
0	1	0	0	X	IN_C	IN_B	IN_A
0	1	0	1	0	Idle	IN_B	IN_B
0	1	0	1	1	IN_C	IN_B	IN_B
0	1	1	0	X	IN_C	IN_B	IN_C
0	1	1	1	0	Idle	IN_B	IN_C
0	1	1	X	1	IN_C	IN_B	IN_C
1	0	0	0	0	IN_A	Idle	IN_A
1	0	0	0	1	IN_A	IN_C	IN_A
1	0	0	1	X	IN_A	IN_C	IN_B
1	0	1	0	0	IN_A	Idle	IN_C
1	0	1	X	1	IN_A	IN_C	IN_C
1	0	1	1	X	IN_A	IN_C	IN_C
1	1	0	0	X	IN_A	IN_B	IN_A
1	1	0	1	X	IN_A	IN_B	IN_B
1	1	1	X	X	IN_A	IN_B	IN_C

[1] Switching is done on a lane-by-lane basis, but input equalization, output pre-emphasis, and loopback are set for each port.

PORT C REVERSE (CROSSOVER) CAPABILITY

Port C has a reversible I/O capability. The sense (input vs. output) of the Port C pins can be swapped by toggling the REVERSE_C control pin. This feature has been added to facilitate the connection to different ASICs that may have the opposite pinouts.

Figure 37 illustrates the reversible I/O function of Port C, and Table 5 describes this function in a selection table that corresponds to a TQFP-100 package. Please note that the reverse capability is supported only on Port C.

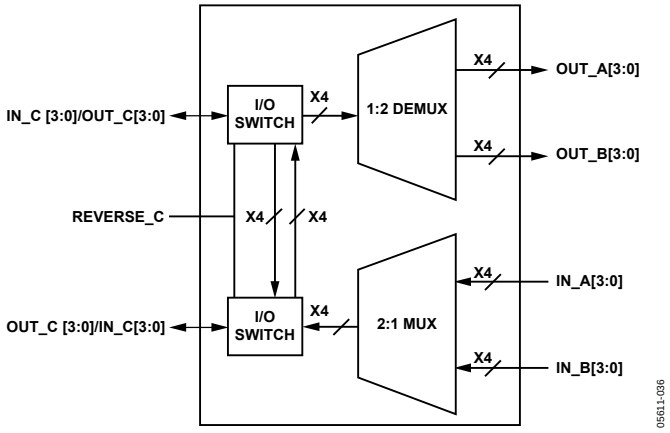


Figure 37. Port C Reverse I/O Capability

APPLICATIONS

The main application of the AD8159 is to support redundancy on both the backplane side and the line interface side of a serial link. Each port consists of four lanes to support standards such as XAUI. Figure 38 illustrates redundancy in an XAUI backplane system. Each line card is connected to two switch fabrics (primary and redundant). The device can be configured to support either 1 + 1 or 1:1 redundancy.

Another application for the AD8159 is test equipment for evaluating high speed serial I/Os running at data rates at or lower than 3.2 Gbps. Figure 40 illustrates a possible application of the AD8159 in a simple XAUI link tester.

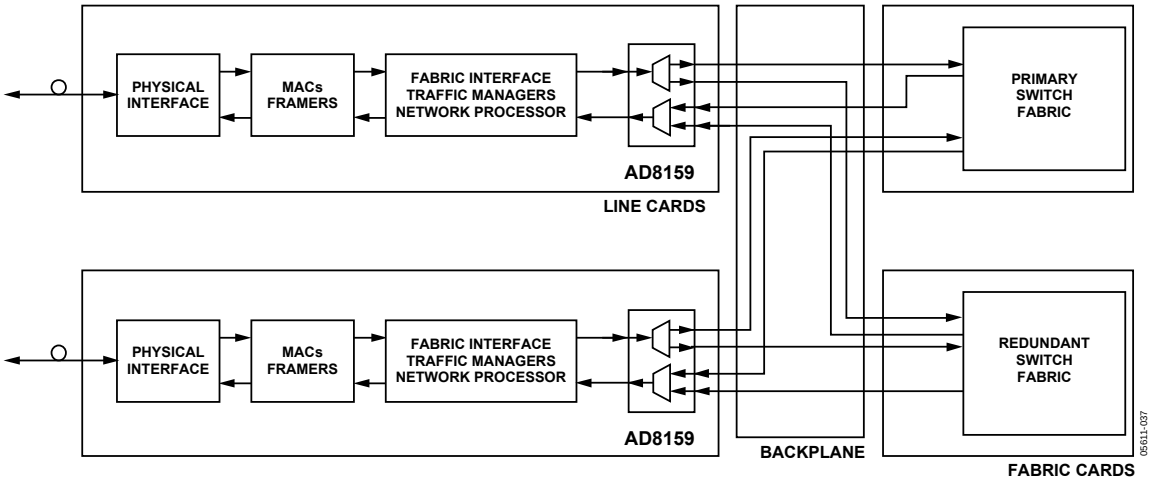


Figure 38. Using the AD8159 for Switch Redundancy

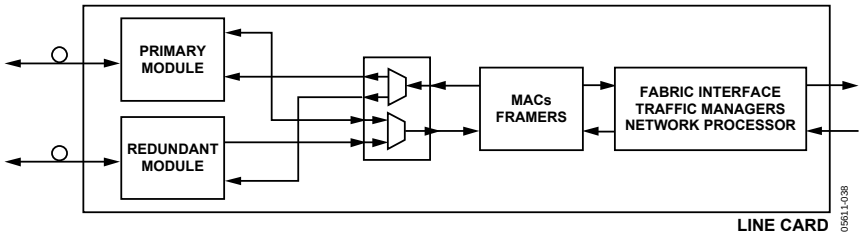


Figure 39. Using the AD8159 for Line Interface Redundancy

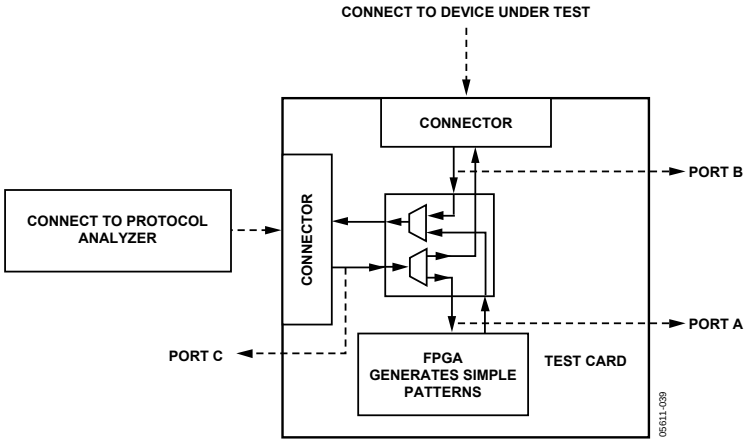


Figure 40. Using the AD8159 in Test Equipment

INTERFACING TO THE AD8159

TERMINATION STRUCTURES

To determine the best strategy for connecting to the high speed pins of the AD8159, the user must first be familiar with the on-chip termination structures. The AD8159 contains two types of these structures (see Figure 41 and Figure 42): one type for input and bidirectional ports and one type for output ports.

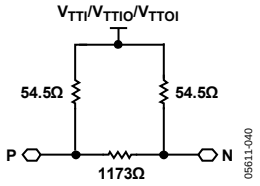


Figure 41. Termination Structure: Input and Bidirectional Ports

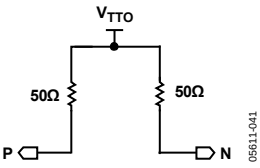


Figure 42. Output Ports

For input and bidirectional ports, the termination structure consists of two 54.5 Ω resistors connected to a termination supply and an 1173 Ω resistor connected across the differential inputs, the latter being a result of the finite differential input impedance of the equalizer.

For output ports, there are two 50 Ω resistors connected to the termination supply. Note that the differential input resistance for both structures is the same, 100 Ω.

INPUT COMPLIANCE

The range of allowable input voltages is determined by the fundamental limitations of the active input circuitry. This range of signals is normally a function of the common-mode level of the input signal, the signal swing, and the supply voltage. For a given input signal swing, there is a range of common-mode voltages that keeps the high and low voltage excursions within acceptable limits. Similarly, for a given common-mode input voltage there is a maximum acceptable input signal swing. There is also a minimum signal swing that the active input circuitry can resolve reliably.

Figure 22 and Figure 25 summarize the input voltage ranges for all ports. Note that the input range is different when comparing bidirectional ports to strictly input ports. This is a consequence of the additional circuitry required to support the bidirectional feature on Port C.

AC Coupling

One way to simplify the input circuit and make it compatible with a wide variety of driving devices is to use ac coupling. This has the effect of isolating the dc common-mode levels of the driver and the AD8159 input circuitry. AC coupling requires a capacitor in series with each single-ended input signal, as shown in Figure 43. This should be done in a manner that does not interfere with the high speed signal integrity of the PCB.

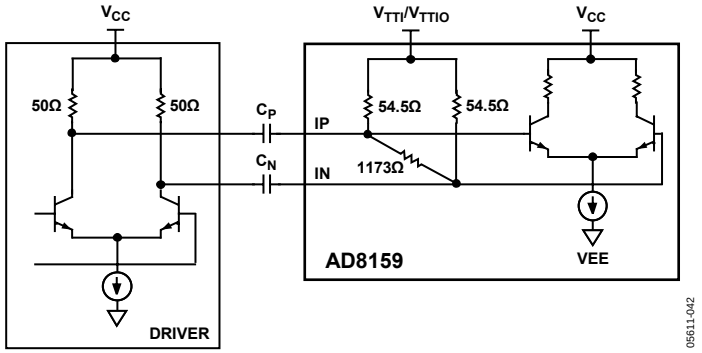


Figure 43. AC-Coupling Input Signal of AD8159

When ac coupling is used, the common-mode level at the input of the device is equal to V_{TTI}. The single-ended input signal swings above and below V_{TTI} equally. The user can then use Figure 22 and Figure 25 to determine the acceptable range of common-mode levels and signal swing levels that satisfy the input range of the AD8159.

If dc coupling is required, determining the input common-mode level is less straightforward because the configuration of the driver must be also be considered. In most cases, the user would set V_{TTI} on the AD8159 to the same level as the driver output termination voltage, V_{TTOD}. This prevents a continuous dc current from flowing between the two supply nets. As a practical matter, both devices can be terminated to the same physical supply net.

Consider the following example: A driver is dc-coupled to the input of the AD8159. The AD8159 input termination voltage (V_{TTI}) and the driver output termination voltage (V_{TTOD}) are both set to the same level; that is, $V_{TTI} = V_{TTOD} = 3.3$ V. If an 800 mV differential p-p swing is desired, the total output current of the driver is 16 mA. At balance, the output current is divided evenly between the two sides of the differential signal path, 8 mA to each side. This 8 mA of current flows through the parallel combination of the 54.5 Ω input termination resistor on the AD8159 and the 50 Ω output termination resistor on the driver, resulting in a common-mode level of

$$V_{TTI} - 8\text{ mA} \times (50\ \Omega \parallel 54.5\ \Omega) = V_{TTI} - 209\text{ mV}$$

The user can then use Figure 25 to determine the allowable range of values for V_{TTI} that meets the input compliance range based on an 800 mV p-p differential swing.

OUTPUT COMPLIANCE

Not surprisingly, there is also a range of voltages that satisfies the requirements of the output devices. This range is specified as the minimum and maximum voltage (with respect to V_{CC}) allowed at an output pin.

DC Coupling

First, consider the dc-coupled case (see Figure 44). A lane on Output Port A or Output Port B on the AD8159 is dc-coupled to a receiving device. In this example, the output termination voltage (V_{TTO}) on the AD8159 is set to the same level as the input termination voltage (V_{TTIR}) on the receiving device, and this level sets the high value (V_{HI}) of the single-ended output voltage. With pre-emphasis low (PE = 0), the maximum single-ended current is 16 mA[1], which flows through the parallel combination of the 50 Ω on-chip resistor and the 50 Ω far end termination. Therefore, the low value (V_{LO}) of the output voltage is equal to

$$V_{TTO} - 16\text{ mA} \times (50\ \Omega \parallel 50\ \Omega) = V_{TTO} - 400\text{ mV}$$

Because the minimum allowed voltage at the output is $V_{CC} - 1.6$ V, the lowest acceptable value for V_{TTO} is

$$V_{CC} - 1.6\text{ V} + 0.4\text{ V} = V_{CC} - 1.2\text{ V}$$

Increasing pre-emphasis to its highest level (PE = 3) results in a maximum, single-ended current of 28 mA.[2] In this case

$$V_{LO} = V_{TTO} - 28\text{ mA} \times (50\ \Omega \parallel 50\ \Omega) = V_{TTO} - 700\text{ mV}$$

As a result, the lowest acceptable value for V_{TTO} is

$$V_{CC} - 1.6\text{ V} + 0.7\text{ V} = V_{CC} - 0.9\text{ V}$$

It is expected that the minimum V_{TTO} is 300 mV higher than the case when PE = 0, because increasing the pre-emphasis level results in a 300 mV lower voltage excursion at the output.

[1] The output current for Port C when PE_C = 0 is slightly higher, 20 mA. The extra 4 mA of current (compared to Port A/Port B) is needed to support the bidirectional feature.
[2] The output current for Port C when PE_C = 3 is 32 mA, for the same reason as stated in Endnote 1.

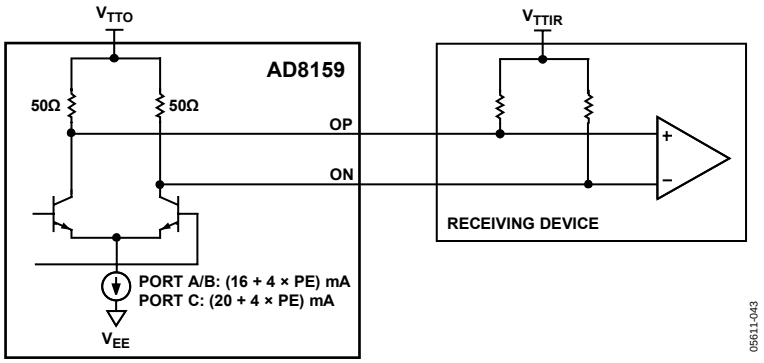


Figure 44. DC-Coupling Output Signal from AD8159

AC Coupling

In general, more V_{TTO} supply headroom is required with ac-coupled outputs. When the outputs are ac-coupled, the average single-ended current does not see the far end 50 Ω termination because the capacitor acts as a dc block. For example, with PE = 0, the single-ended output current alternates from 0 mA to 16 mA, or 8 mA on average. This 8 mA current flows entirely through the on-chip 50 Ω termination resistor due to the dc block.

The single-ended output voltage has an average value of

$$V_{TTO} - 8\text{ mA} \times 50\ \Omega = V_{TTO} - 400\text{ mV}$$

For appropriate data patterns,[1] the capacitor acts as a short and the voltage swing is 400 mV p-p, identical to the dc-coupled case. The low output voltage is, therefore,

$$V_{TTO} - 400\text{ mV} - 200\text{ mV} = V_{TTO} - 600\text{ mV}$$

[1]AC coupling requires that the signal pattern have no long term dc component. Codes such as 8b/10b, for example, ensure that the data pattern is benign in an ac-coupled link.

The lowest acceptable value for V_{TTO} is

$$V_{CC} - 1.6\text{ V} + 0.6\text{ V} = V_{CC} - 1.0\text{ V}$$

The same exercise can be repeated for other pre-emphasis settings.

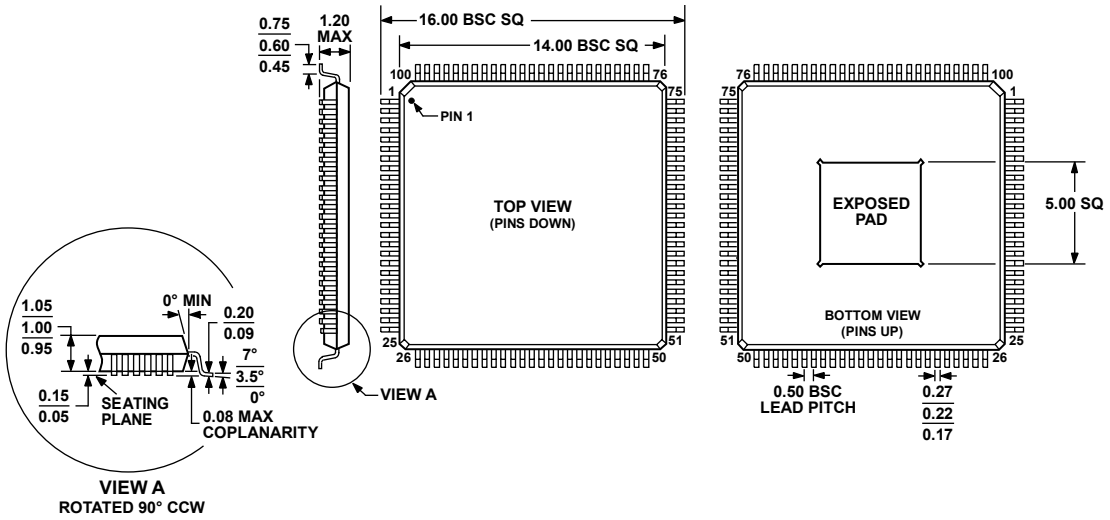
Output Compliance Table

To simplify the task of interfacing to the AD8159 output, Table 13 is useful as a quick-reference. It provides the minimum and maximum values for output termination voltage for both ac and dc coupling. The values in the table are valid for any pre-emphasis setting.

Table 13. Output Compliance

	AC-Coupled		DC-Coupled	
	Minimum (V)	**Maximum (V)**	**Minimum (V)**	**Maximum (V)**
V_{TTO}	V_{CC} – 0.5	V_{CC} + 0.6	V_{CC} – 0.9	V_{CC} + 0.6
V_{TTOI}	V_{CC} – 0.4	V_{CC} + 0.6	V_{CC} – 0.8	V_{CC} + 0.6

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

NOTES
1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE AD8159 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO V_{EE}. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A V_{EE} PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

040506-A

Figure 45. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8159ASVZ[1]	−40°C to +85°C	100-Lead TQFP_EP	SV-100-4
AD8159-EVAL-DC	−40°C to +85°C	DC-Coupled Evaluation Board	
AD8159-EVAL-AC	−40°C to +85°C	AC-Coupled Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

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D05611-0-4/06(A)