

### FEATURES

- Low offset voltage: 13  $\mu$ V maximum**
- Input offset drift: 0.03  $\mu$ V/ $^{\circ}$ C**
- Single-supply operation: 2.7 V to 5.5 V**
- High gain, CMRR, and PSRR**
- Low input bias current: 25 pA**
- Low supply current: 180  $\mu$ A**

### APPLICATIONS

- Mobile communications**
- Portable instrumentation**
- Battery-powered devices**
- Sensor interfaces**
- Temperature measurement**
- Electronic scales**

### GENERAL DESCRIPTION

The AD8538 is a very high precision amplifier featuring extremely low offset voltage, low input bias current, and low power consumption. The supply current is less than 180  $\mu$ A at 5.0 V. Operation is fully specified from 2.7 V to 5.0 V single supply ( $\pm 1.35$  V to  $\pm 2.5$  V dual supply).

The AD8538 operates using very low power making this amplifier ideal for battery-powered devices and portable equipment.

The AD8538 is specified over the extended industrial temperature range ( $-40^{\circ}$ C to  $+125^{\circ}$ C). The AD8538 amplifier is available in 5-lead TSOT-23, and 8-lead, narrow body SOIC packages.

### PIN CONFIGURATION DIAGRAMS

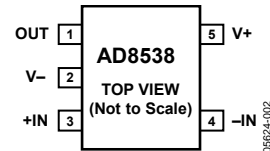


Figure 1. 5-Lead TSOT-23 (UJ-5)

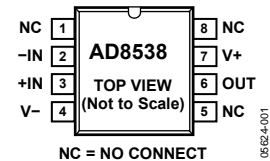


Figure 2. 8-Lead SOIC\_N (R-8)

#### Rev. 0

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**REVISION HISTORY**

10/05—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

@ $V_S = 5.0\text{ V}$ ,  $V_{CM} = 2.5\text{ V}$ ,  $V_O = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	13	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	25	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	$\text{nA}$
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		150	$\text{pA}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; $V_{CM} = 0.2\text{ V to } 4.8\text{ V}$	115	150		$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 0.1\text{ V to } 4.9\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	135		$\text{dB}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	135	0.1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.99	4.998		$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.98			$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	4.970		$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.94			$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.9	5	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2.8	7	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		17	20	$\text{mV}$
Short-Circuit Limit	$I_{SC}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	30	$\text{mV}$
				$\pm 25$		$\text{mA}$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$I_O = 0$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	125		$\text{dB}$
				150	180	$\mu\text{A}$
				190	215	$\mu\text{A}$
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		$\text{V}/\mu\text{s}$
Settling Time 0.01%	$t_s$	$G = \pm 1$ , $2\text{ V step}$ , $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		10		$\mu\text{s}$
Overload Recovery Time				0.05		$\text{ms}$
Gain Bandwidth Product	GBP			600		$\text{kHz}$
Phase Margin	$\phi_o$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$

# AD8538

@  $V_S = 2.7\text{ V}$ ,  $V_{CM} = 1.35\text{ V}$ ,  $V_O = 1.35\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	13	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	25	$\mu\text{A}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	$\text{nA}$
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	$\text{pA}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		150	$\text{pA}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 0.1\text{ V to } 1.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	140	2.7	$\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	135		$\text{dB}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.68	2.698		$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.68			$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.67	2.68		$\text{V}$
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.66			$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.7	5	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2.4	5	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		14	20	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to $V_+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	25	$\text{mV}$
Short-Circuit Limit	$I_{SC}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		$\pm 8$		$\text{mA}$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$I_O = 0$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	125		$\text{dB}$
				150	180	$\mu\text{A}$
				190	215	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		$\text{V}/\mu\text{s}$
Settling Time 0.01%	$t_s$	$G = \pm 1$ , $1\text{ V step}$ , $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		5		$\mu\text{s}$
Overload Recovery Time				0.05		$\text{ms}$
Gain Bandwidth Product	GBP			600		$\text{kHz}$
Phase Margin	$\angle O$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		65		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
Supply Voltage	+6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Observe derating curve
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at  $25^\circ\text{C}$ , unless otherwise noted.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Characteristics**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Lead TSOT-23 (UJ-5)	207	61	$^\circ\text{C}/\text{W}$
8-Lead SOIC_N (R-8)	158	43	$^\circ\text{C}/\text{W}$

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SY} = 5\text{ V}$  or  $\pm 2.5\text{ V}$ , unless otherwise noted.

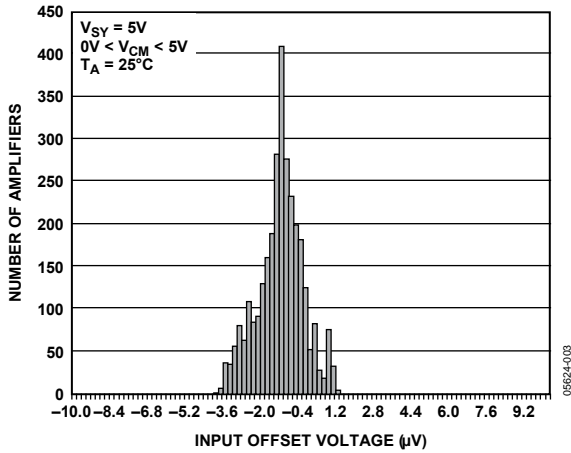


Figure 3. Input Offset Voltage Distribution

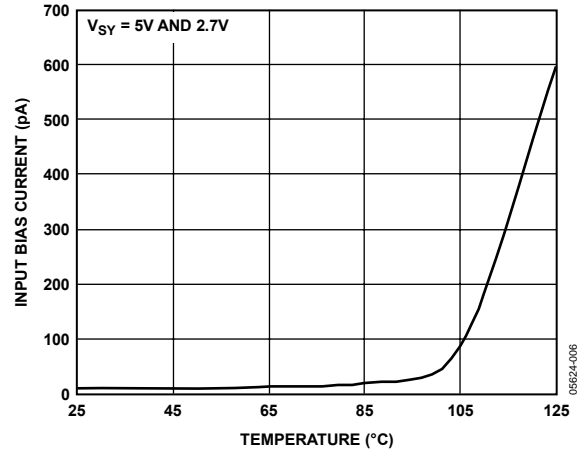


Figure 6. Input Bias Current vs. Temperature

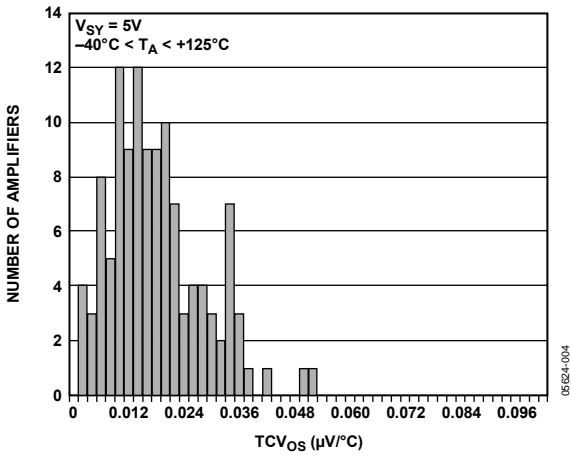


Figure 4. Input Offset Voltage Drift Distribution

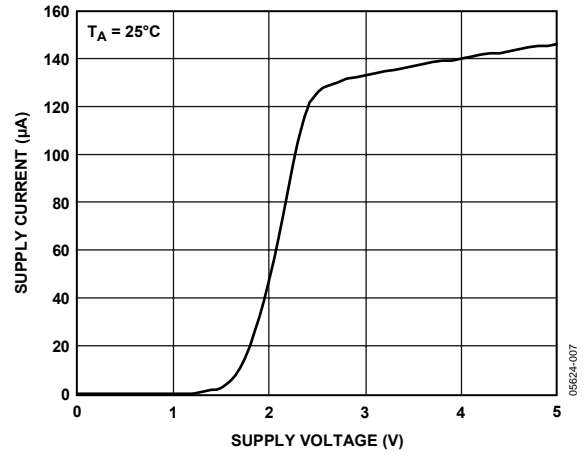


Figure 7. Supply Current vs. Supply Voltage

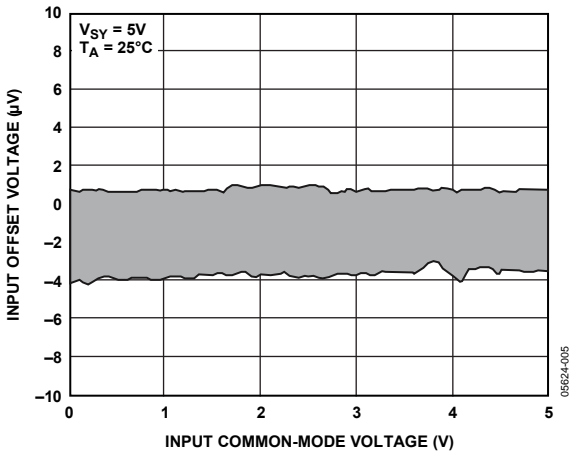


Figure 5. Input Offset Voltage vs. Input Common-Mode Voltage

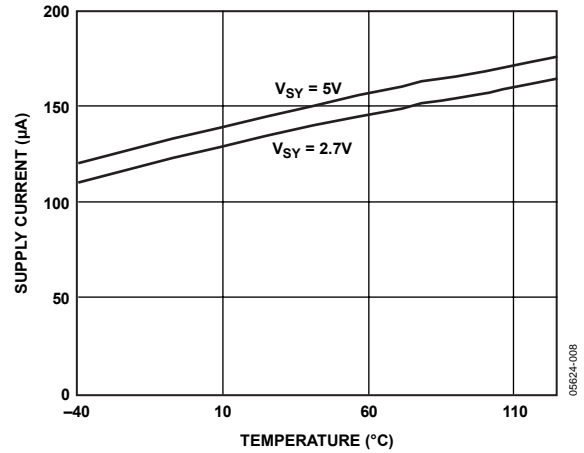


Figure 8. Supply Current vs. Temperature

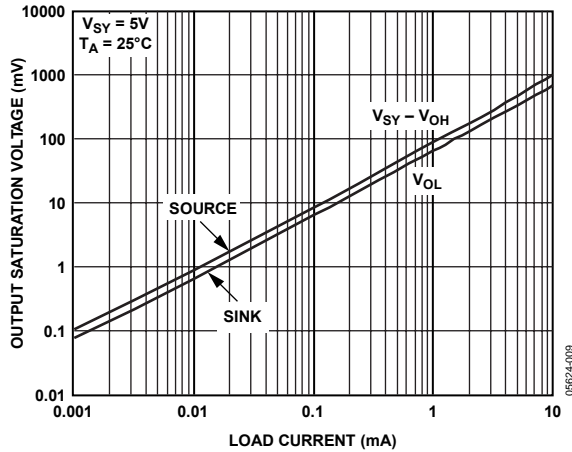


Figure 9. Output Saturation Voltage vs. Load Current

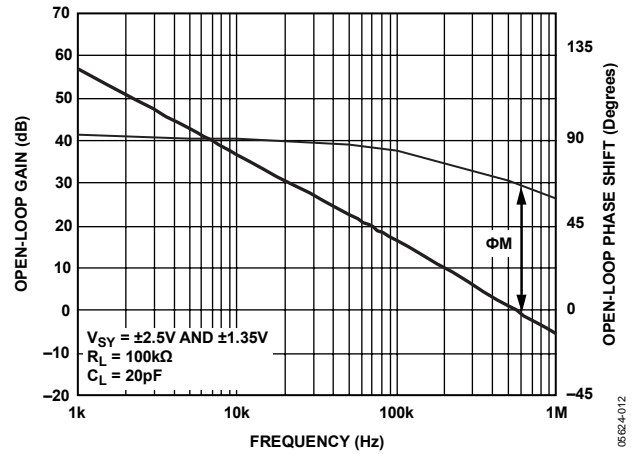


Figure 12. Open-Loop Gain and Phase vs. Frequency

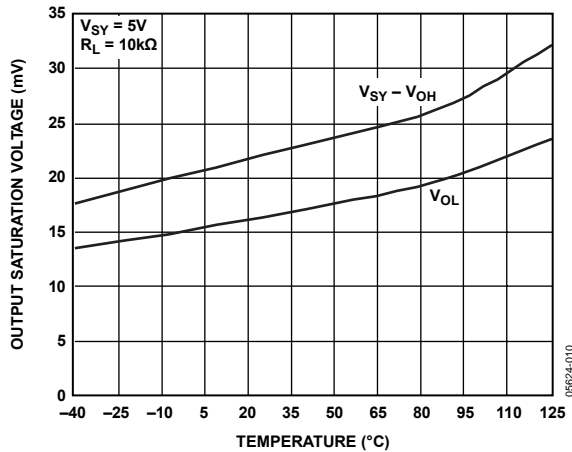


Figure 10. Output Saturation Voltage vs. Temperature

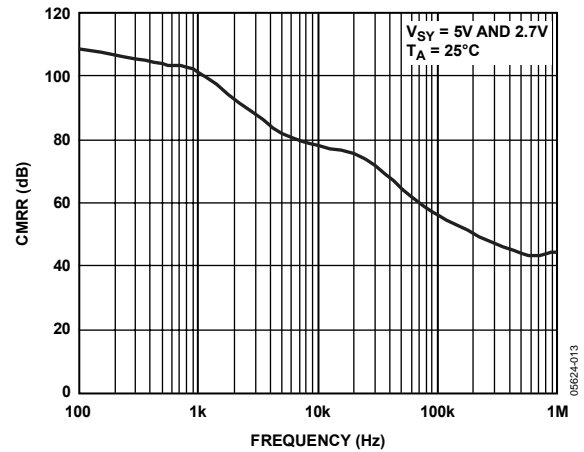


Figure 13. CMRR vs. Frequency

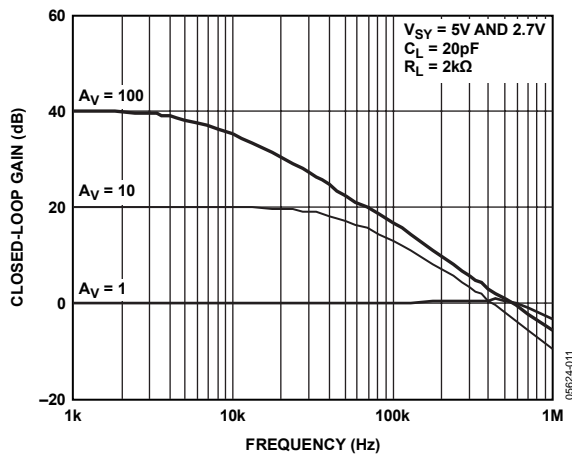


Figure 11. Closed-Loop Gain vs. Frequency

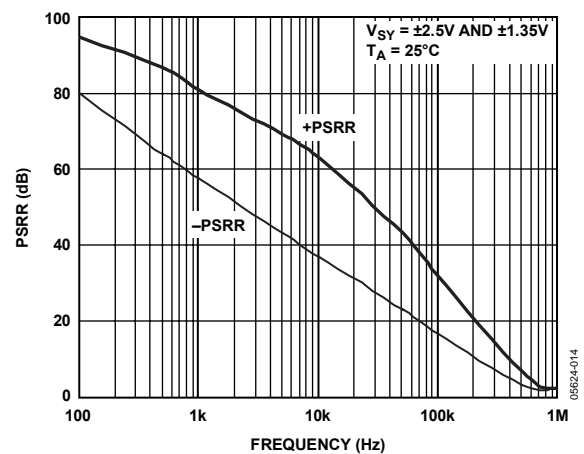


Figure 14. PSRR vs. Frequency

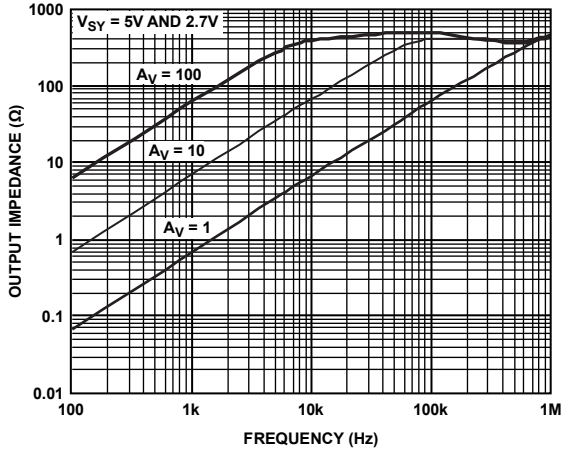


Figure 15. Closed-Loop Output Impedance vs. Frequency

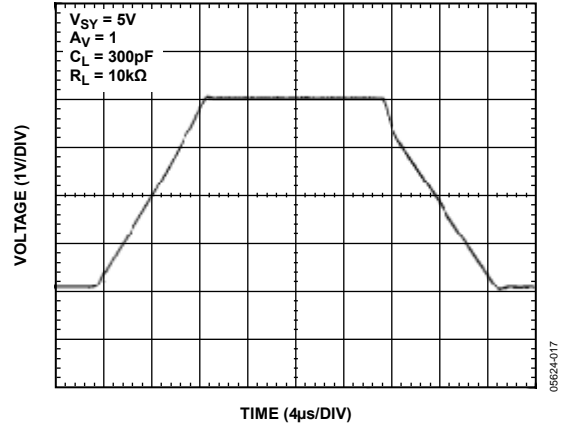


Figure 18. Large Signal Transient Response

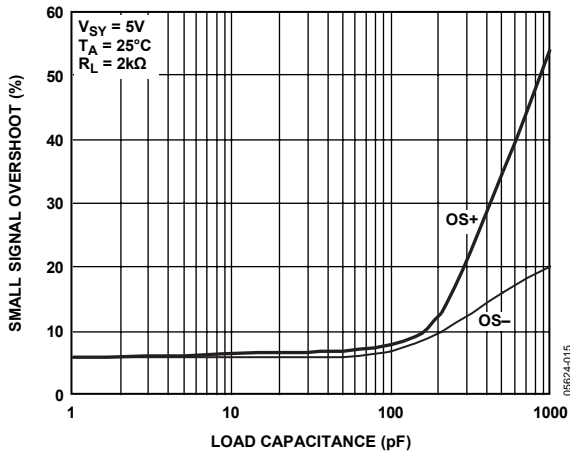


Figure 16. Small Signal Overshoot vs. Load Capacitance

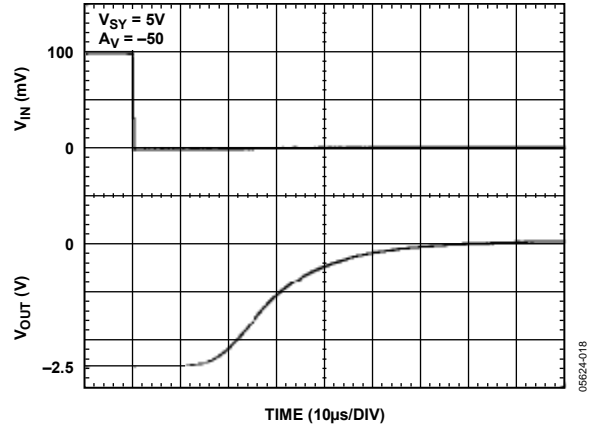


Figure 19. Positive Overload Recovery

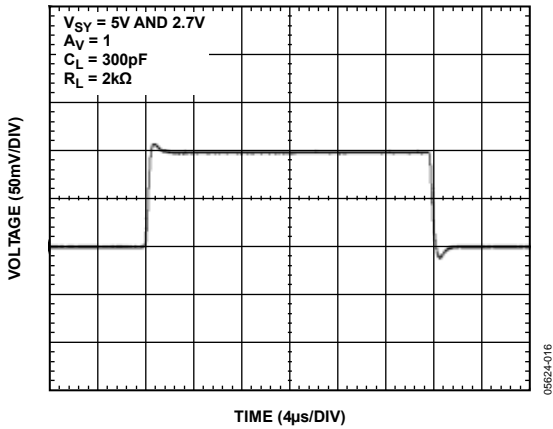


Figure 17. Small Signal Transient Response

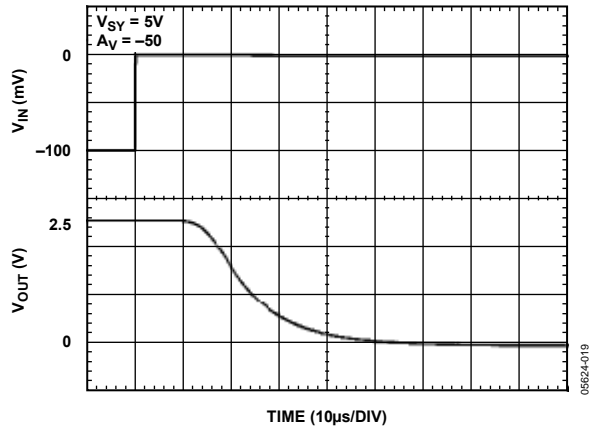


Figure 20. Negative Overload Recovery



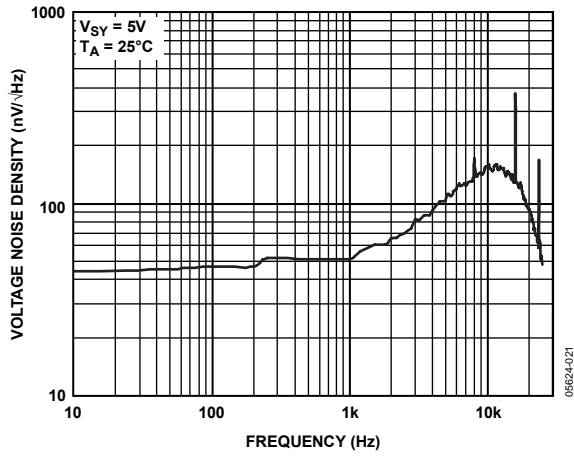


Figure 21. Voltage Noise Density

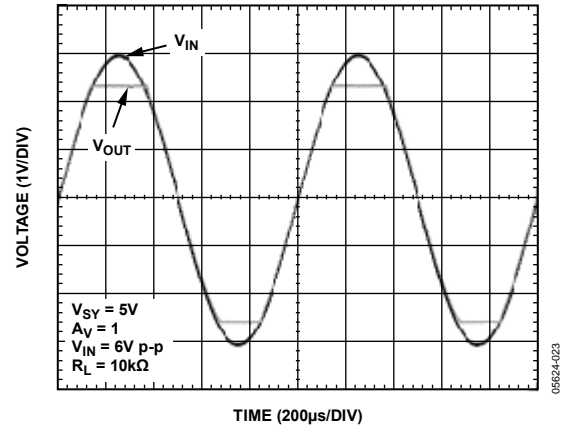


Figure 23. No Phase Reversal

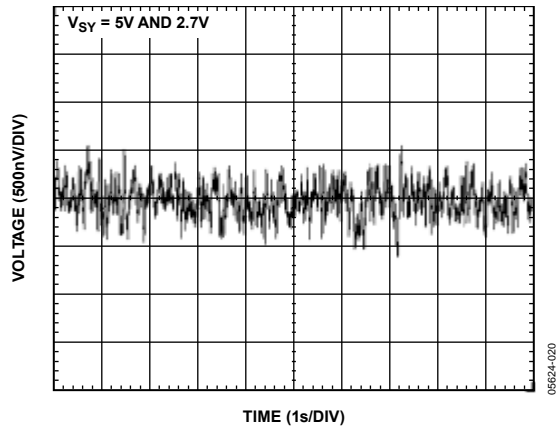


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

$V_s = 2.7\text{ V}$  or  $\pm 1.35\text{ V}$ .

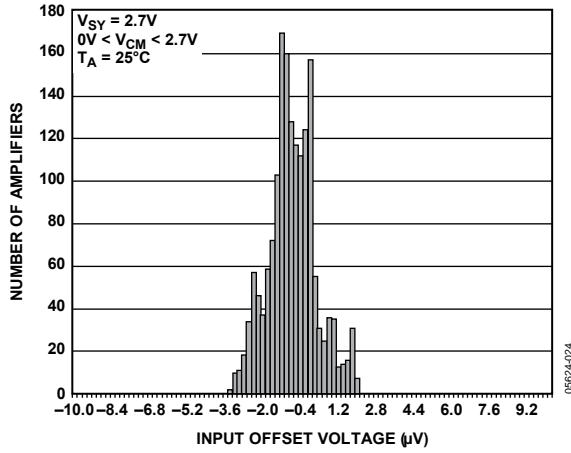


Figure 24. Input Offset Voltage Distribution

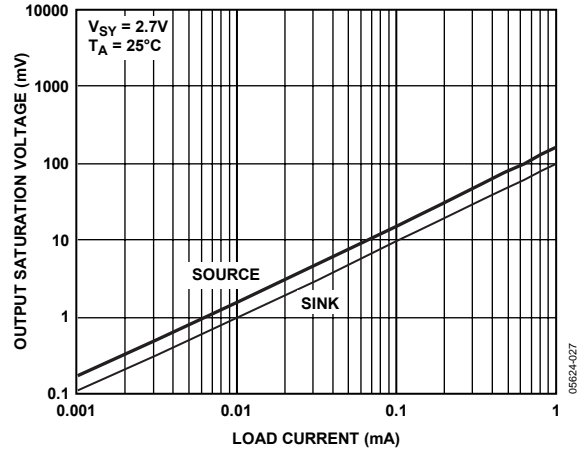


Figure 27. Output Saturation Voltage vs. Load Current

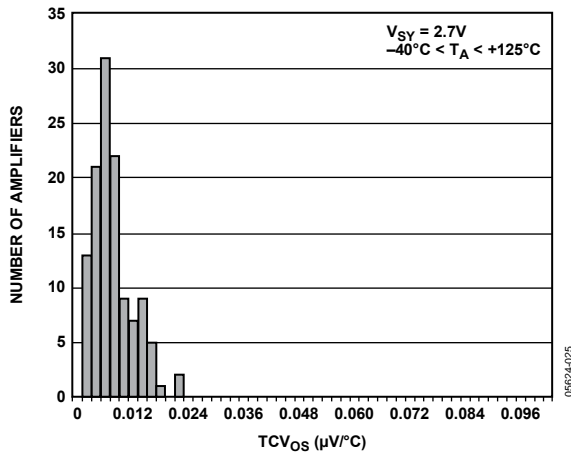


Figure 25. Input Offset Voltage Drift Distribution

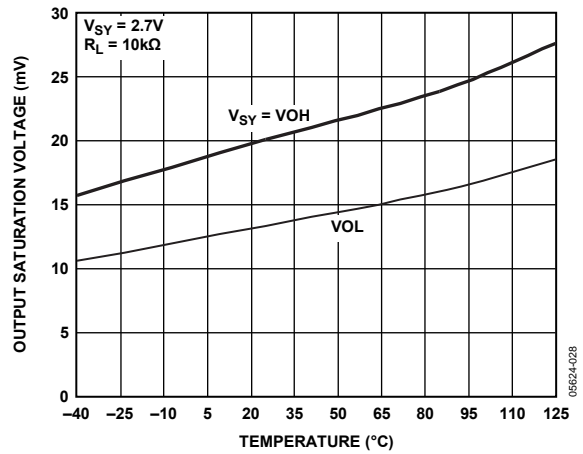


Figure 28. Output Saturation Voltage vs. Temperature

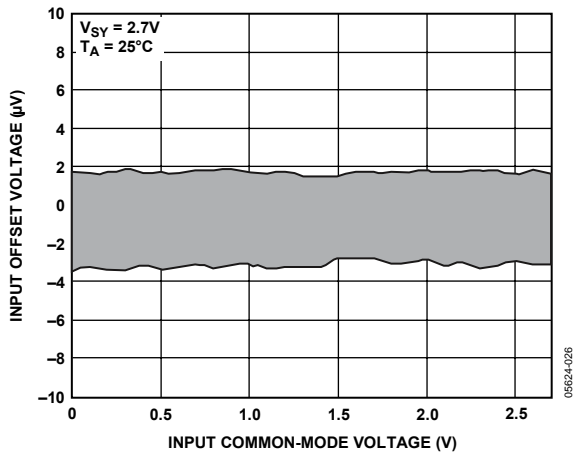


Figure 26. Input Offset Voltage vs. Input Common-Mode Voltage

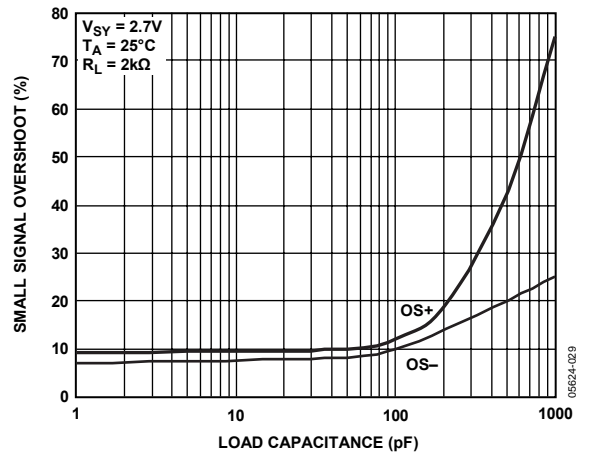


Figure 29. Small Signal Overshoot vs. Load Capacitance

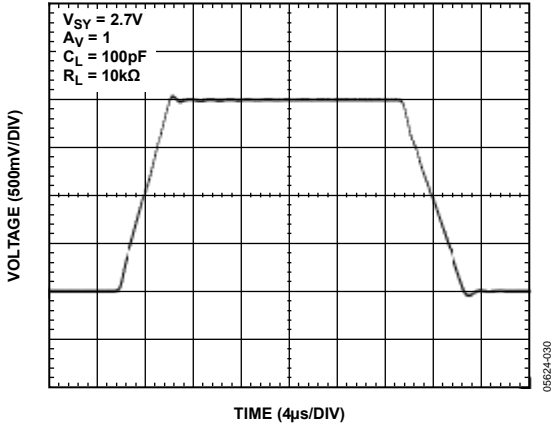


Figure 30. Large Signal Transient Response

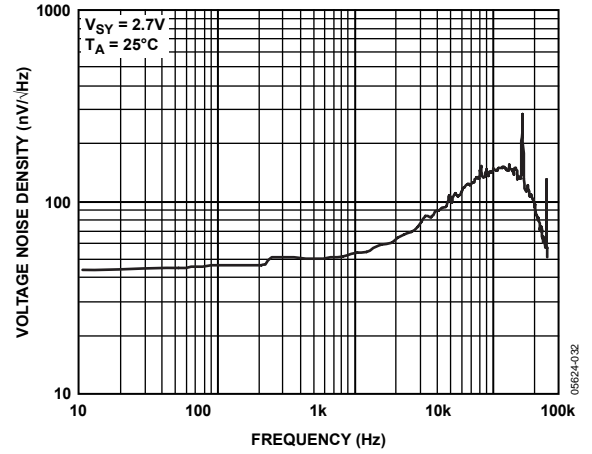


Figure 31. Voltage Noise Density

## OUTLINE DIMENSIONS

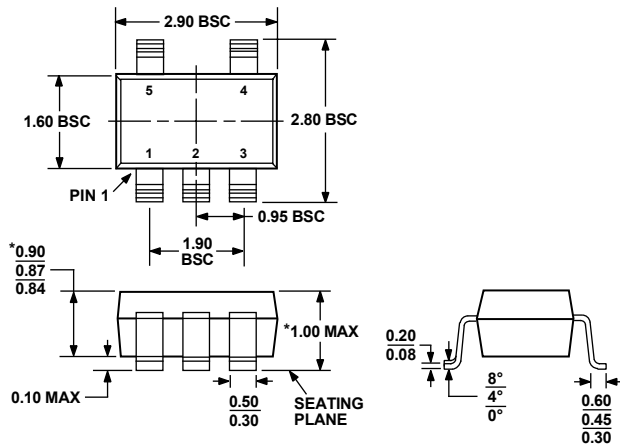


Figure 32. 5-Lead Thin Small Outline Transistor Package [TSOT\_23] (UJ-5)  
Dimensions shown in millimeters

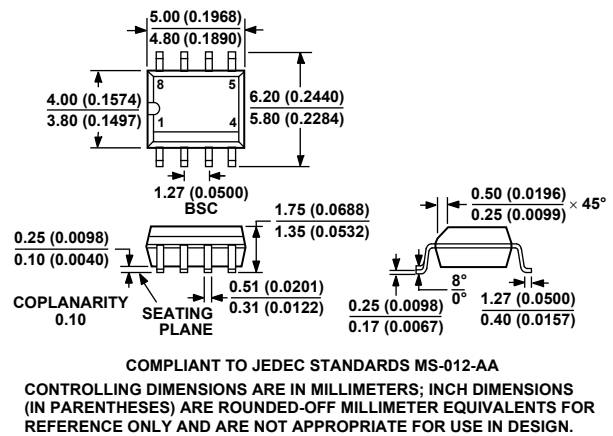


Figure 33. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)  
Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8538AUJZ-R2 <sup>1</sup>	-40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538AUJZ-REEL <sup>1</sup>	-40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538AUJZ-REEL7 <sup>1</sup>	-40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538ARZ <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8538ARZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8538ARZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	

<sup>1</sup> Z = Pb-free part.