

FEATURES

Lower power at high voltage: 180 μ A typical

Low offset voltage: 100 μ V

Voltage noise

21 nV/ $\sqrt{\text{Hz}}$ at 10 kHz

23 nV/ $\sqrt{\text{Hz}}$ at 1 kHz

Low input bias current: 300 fA

Single-supply operation: 5 V to 16 V

Dual-supply operation: ± 2.5 V to ± 8 V

Output drive: 10 mA

Unity gain stable

APPLICATIONS

Medical equipment

Physiological measurement

Precision references

Buffer/level shifting

Portable operated systems

High density power budget systems

Multipole filters

Sensors

Photodiode amplification

ADC drivers

GENERAL DESCRIPTION

The AD8667 is a dual, rail-to-rail output, single-supply/dual-supply amplifier that uses Analog Devices, Inc. patented DigiTrim[®] trimming technique to achieve low offset voltage, 300 μ V over the common-mode range. The AD8667 features an extended operating range with supply voltages up to 16 V for low power operation with an I_{SV} of $<325 \mu\text{A}$ per amplifier over temperature. The device is designed for low noise at higher voltages: 21 nV/ $\sqrt{\text{Hz}}$ at 10 kHz and 23 nV/ $\sqrt{\text{Hz}}$ at 1 kHz. It also features a low input bias current of 300 fA and a 10 mA output drive.

The combination of low supply currents, low offsets, very low input bias currents, and wide supply range makes the AD8667

PIN CONFIGURATION



Figure 1. 8-Lead MSOP, 8-Lead SOIC

ideal for a wide variety of low power applications. Systems utilizing dc-to-low frequency measurements or high impedance sensors, such as photodiodes, benefit from the low input bias current, low noise, low offset, and low drive current. The wide operating voltage range matches today's high performance ADCs and DACs. Medical monitoring equipment can take advantage of the low voltage noise, high input impedance, low voltage, and low current noise.

The AD8667 is specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	5
Applications.....	1	Thermal Resistance	5
Pin Configuration.....	1	ESD Caution.....	5
General Description	1	Typical Performance Characteristics	6
Revision History	2	Outline Dimensions	13
Specifications.....	3	Ordering Guide	13
Electrical Characteristics	3		

REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 2.5\text{ V}$			100	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			350	μV
		$V_{CM} = 0\text{ V to }3.5\text{ V}$		70	300	μV
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		100	450	μV
		$V_{CM} = 0.2\text{ V to }3.5\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$		100	450	μV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.3		pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			20	pA
					150	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2		pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			15	pA
					50	pA
Input Voltage Range	IVR	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	0		3.5	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	0.2		3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }3.5\text{ V}$	80	90		dB
		$V_{CM} = 0.2\text{ V to }3.5\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$	80	90		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega, V_O = 0.5\text{ V to }4.5\text{ V}$	106	115		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.3	5	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$	4.65	4.8		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.6	4.7		V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$		150	200	mV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		200	250	mV
Short-Circuit Current	I_{SC}			± 6		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 100\text{ kHz}, A_V = 1$		120		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to }16\text{ V}$	95	105		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		180	275	μA
					325	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.2		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.1%, 0 V to 2 V step, $A_V = 10$		12		μs
Gain Bandwidth Product	GBP			600		kHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		3		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 10\text{ kHz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		23		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

AD8667

$V_S = 16\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 8\text{ V}$		40	300	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			350	μV
		$V_{CM} = 0\text{ V to }14.5\text{ V}$		70	300	μV
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			450	μV
		$V_{CM} = 0.2\text{ V to }14.5\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$			450	μV
Input Bias Current	I_B			0.3		pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			30	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			250	pA
Input Offset Current	I_{OS}			0.2		pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			25	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			150	pA
Input Voltage Range	IVR	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	0		14.5	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	0.2		14.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }14.5\text{ V}$	90	100		dB
		$V_{CM} = 0.2\text{ V to }14.5\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$	90	100		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega, V_O = 0.5\text{ V to }15.5\text{ V}$	112	124		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.2	5	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$	15.8	15.9		V
Output Voltage Low	V_{OL}	$I_L = 10\text{ mA}$	14.8	15.1		V
		$I_L = 10\text{ mA}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$	14.65	14.8		V
		$I_L = 1\text{ mA}$		80	100	mV
Short-Circuit Current	I_{SC}	$I_L = 10\text{ mA}$		600	720	mV
		$I_L = 10\text{ mA}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$		800	900	mV
				± 50		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 100\text{ kHz}, A_V = 1$		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to }16\text{ V}, -40^\circ\text{C} < T_A < +125^\circ\text{C}$	95	105		dB
Supply Current/Amplifier	I_{SY}			230	285	μA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			325	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		0.3		$\text{V}/\mu\text{s}$
Settling Time	t_S	To 0.1%, 0 V to 2 V step		12		μs
Gain Bandwidth Product	GBP			600		kHz
Phase Margin	Φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		3		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		23		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	-0.1 V to V_s
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-60°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	145	45	°C/W
8-Lead SOIC	125	43	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Specifications at $V_{SY} = \pm 8\text{ V}$, unless otherwise noted.

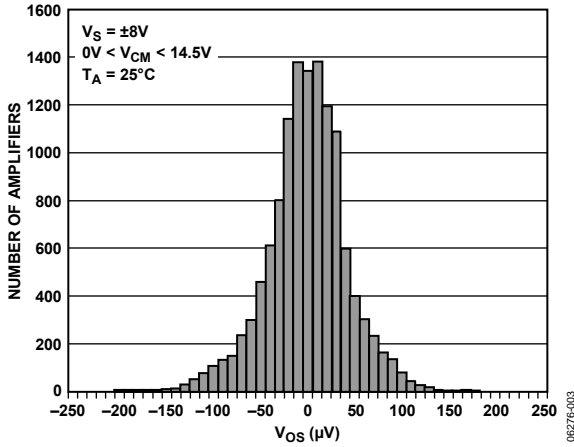


Figure 2. Input Offset Voltage Distribution

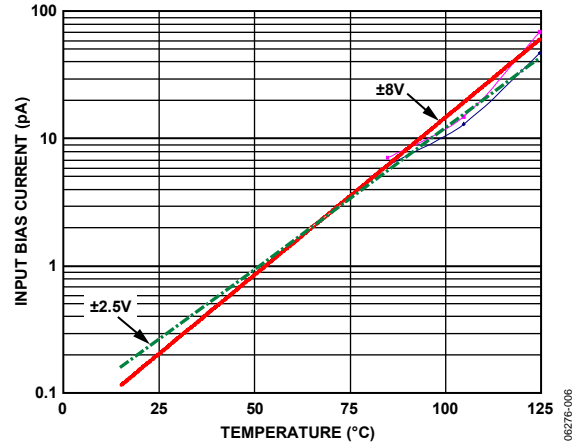


Figure 5. Input Bias Current vs. Temperature

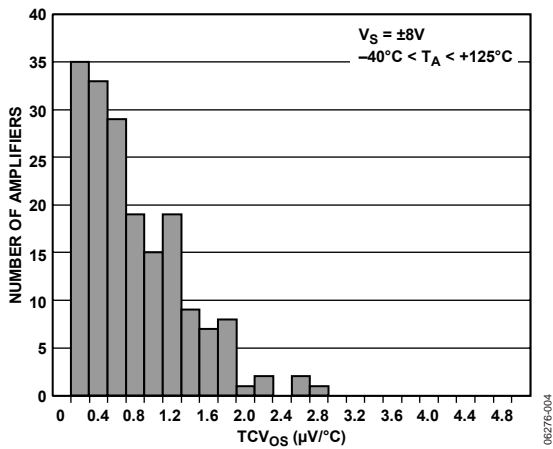


Figure 3. Input Offset Voltage Drift Distribution

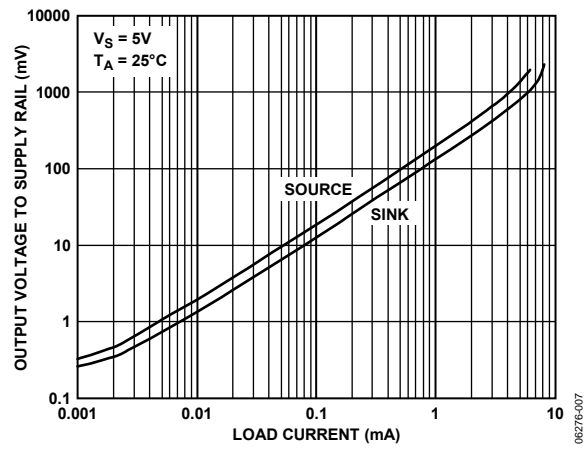


Figure 6. Output Swing Saturation Voltage vs. Load Current

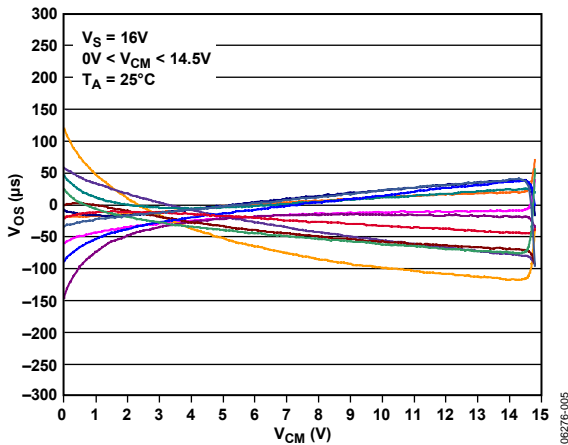


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

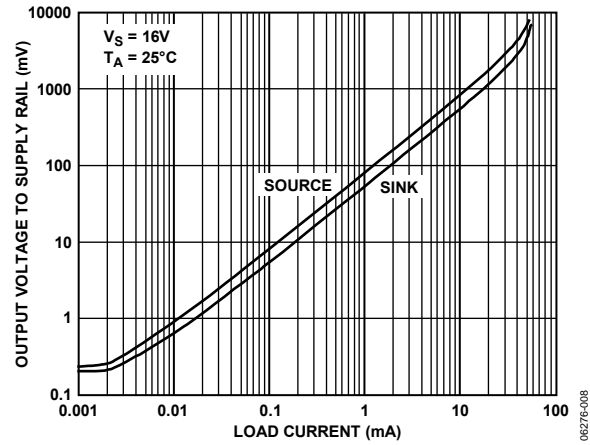


Figure 7. Output Swing Saturation Voltage vs. Load Current

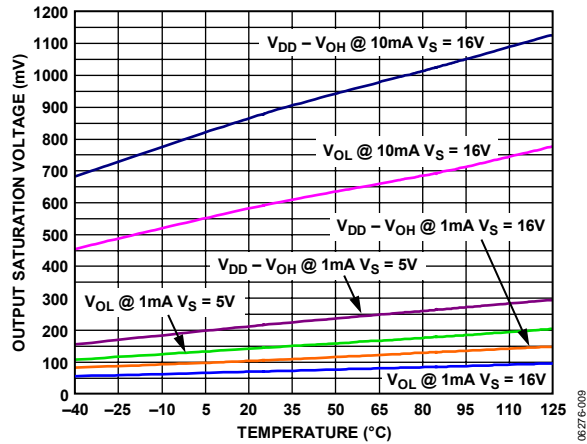


Figure 8. Output Saturation Voltage vs. Temperature

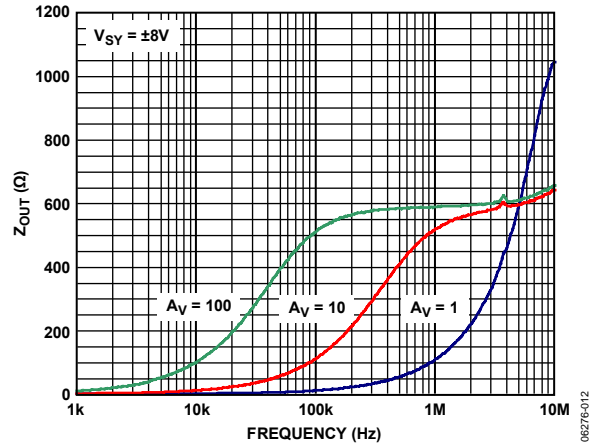


Figure 11. Closed-Loop Output Impedance vs. Frequency

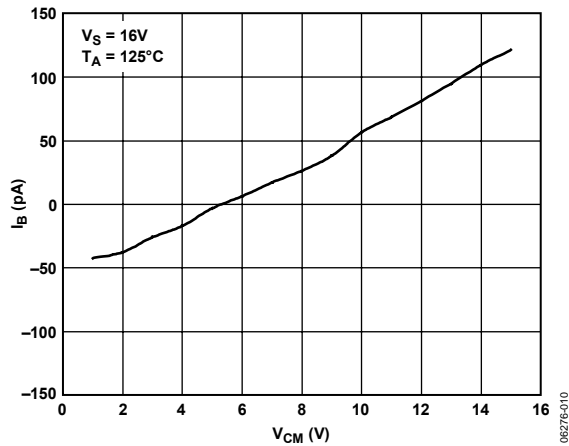


Figure 9. Input Bias Current vs. Common Mode Voltage at 125°C

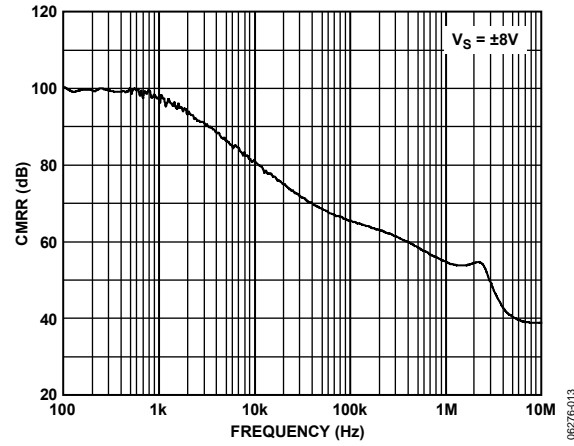


Figure 12. CMRR vs. Frequency

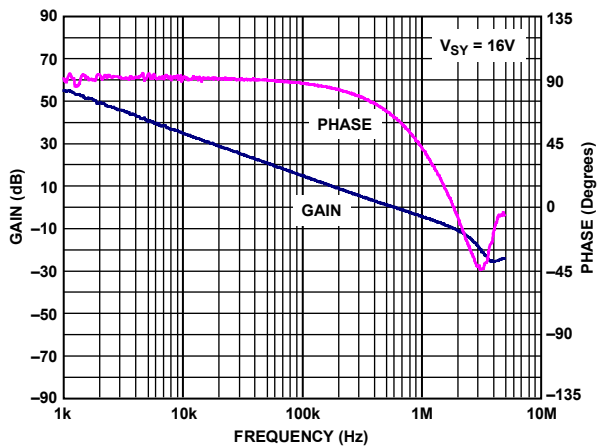


Figure 10. Open-Loop Gain and Phase Shift vs. Frequency

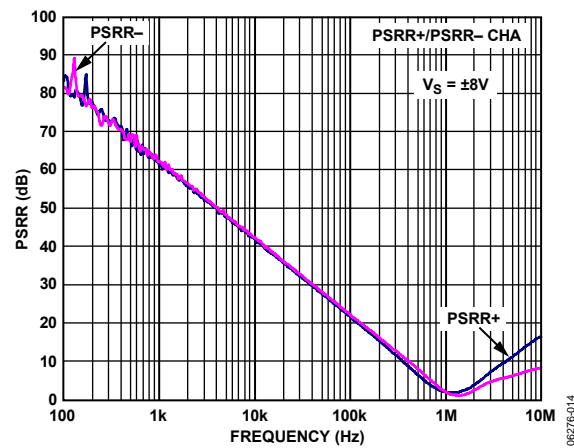


Figure 13. PSRR vs. Frequency

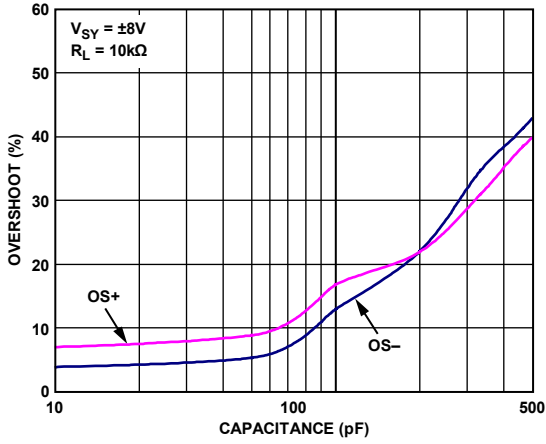


Figure 14. Small Signal Overshoot vs. Load Capacitance

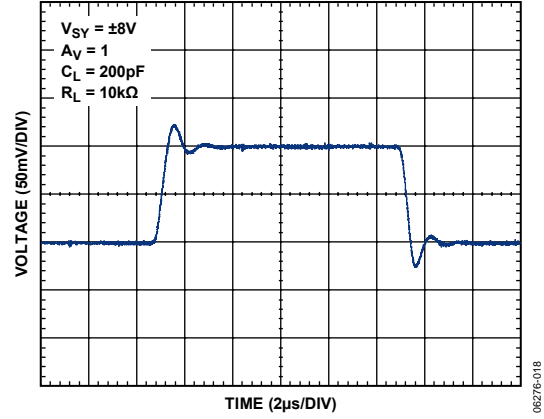


Figure 17. Small Signal Transient Response

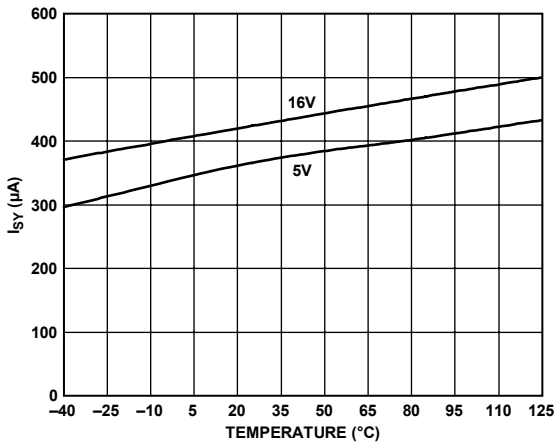


Figure 15. Supply Current vs. Temperature

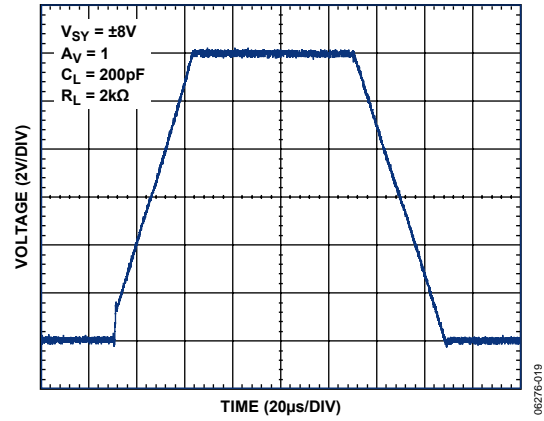


Figure 18. Large Signal Transient Response

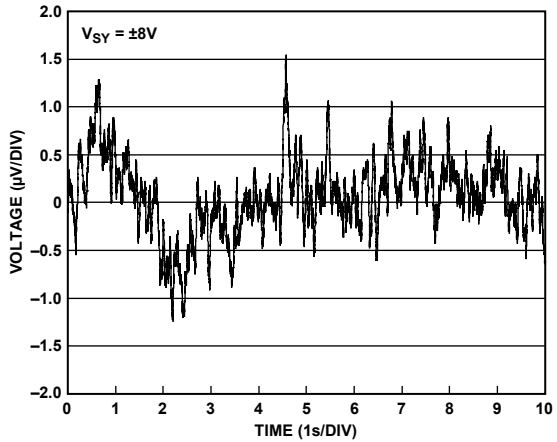


Figure 16. 0.1 Hz to 10 Hz Input Voltage Noise

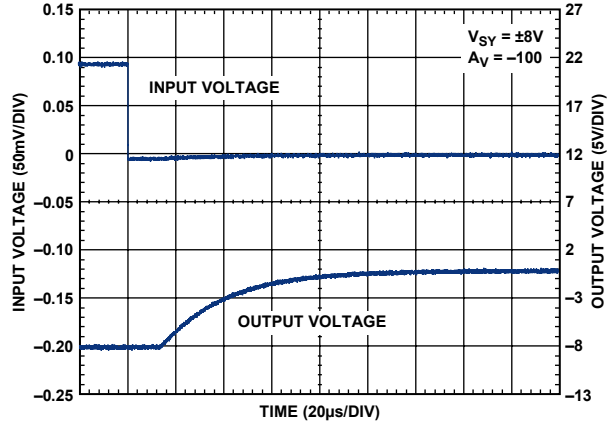


Figure 19. Positive Overload Recovery

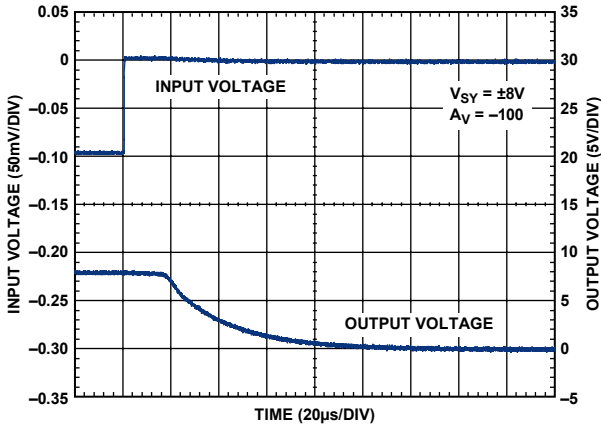


Figure 20. Negative Overload Recovery

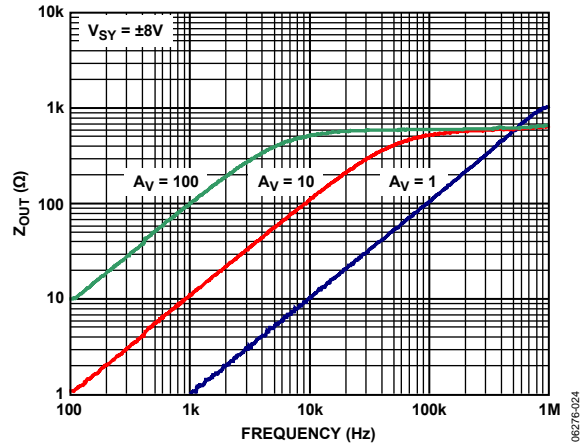


Figure 23. Closed-Loop Output Impedance vs. Frequency

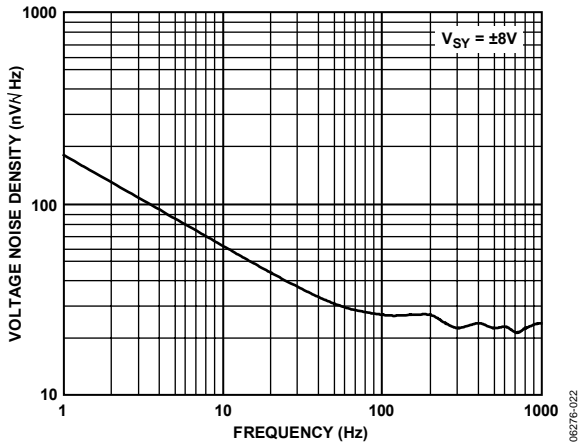


Figure 21. Voltage Noise Density vs. Frequency

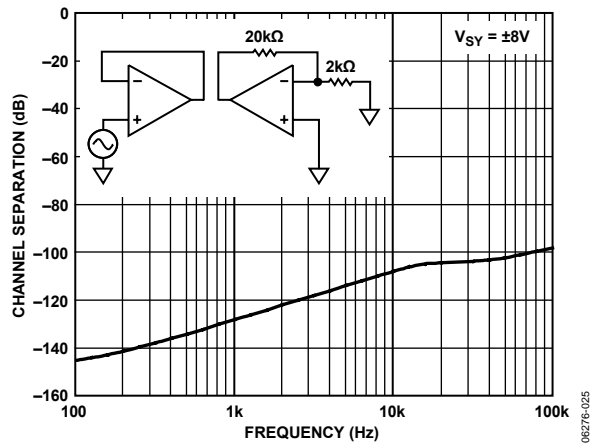


Figure 24. Channel Separation vs. Frequency

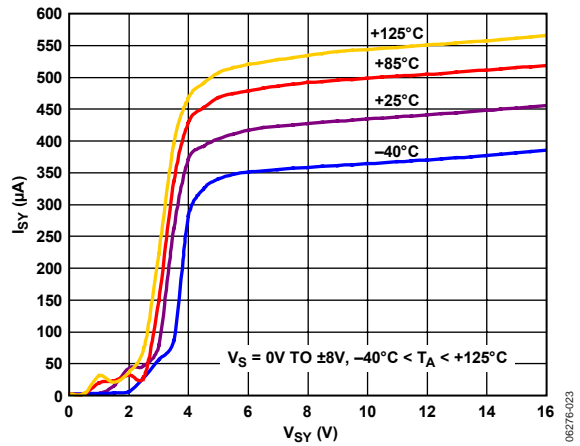


Figure 22. Supply Current vs. Supply Voltage

Specifications at $V_{SY} = \pm 2.5$ V, unless otherwise noted.

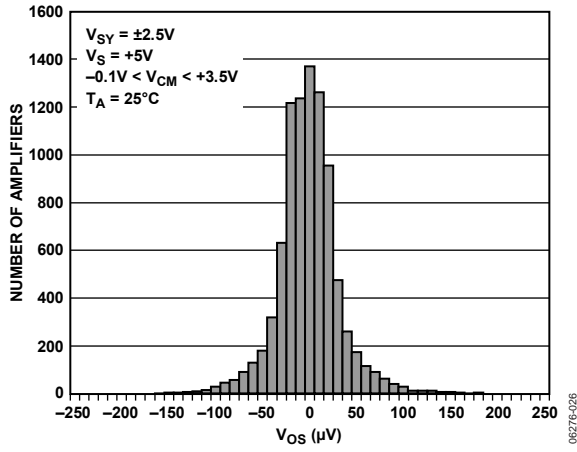


Figure 25. Input Offset Voltage Distribution

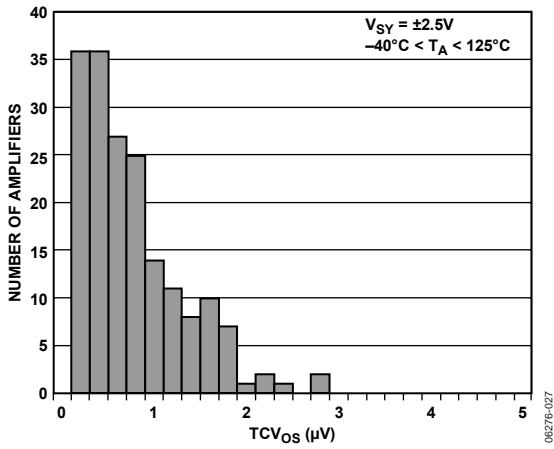


Figure 26. Input Offset Voltage Drift Distribution

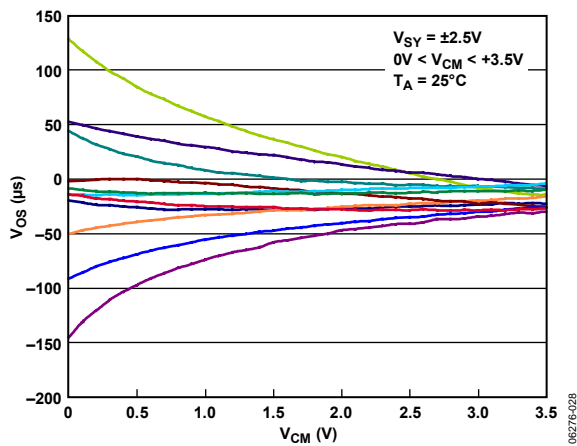


Figure 27. Input Offset Voltage vs. Common-Mode Voltage

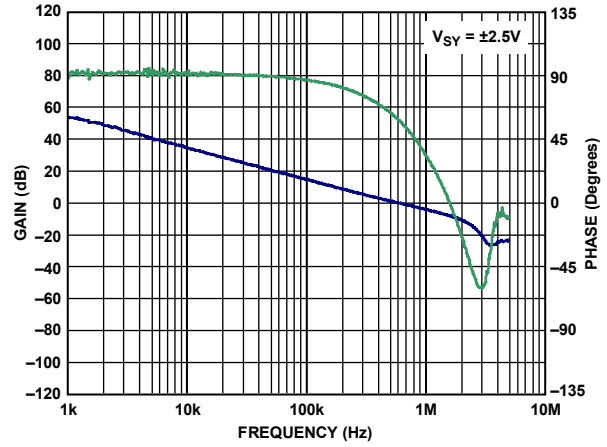


Figure 28. Open-Loop Gain and Phase Shift vs. Frequency

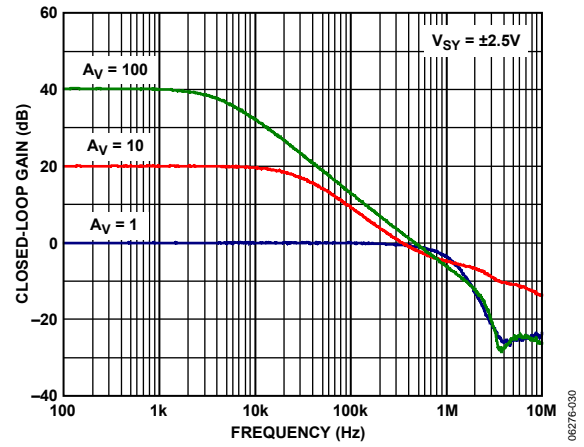


Figure 29. Closed-Loop Gain vs. Frequency

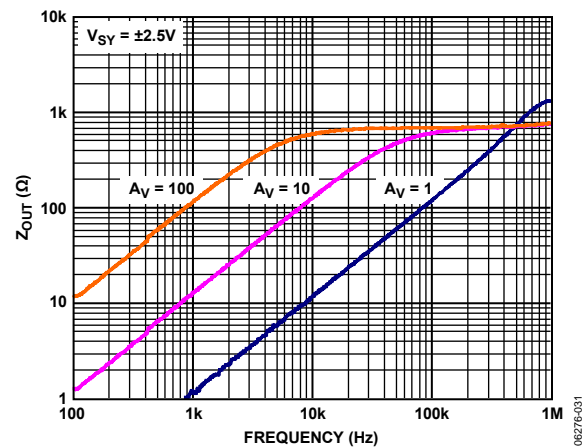


Figure 30. Closed-Loop Output Impedance vs. Frequency

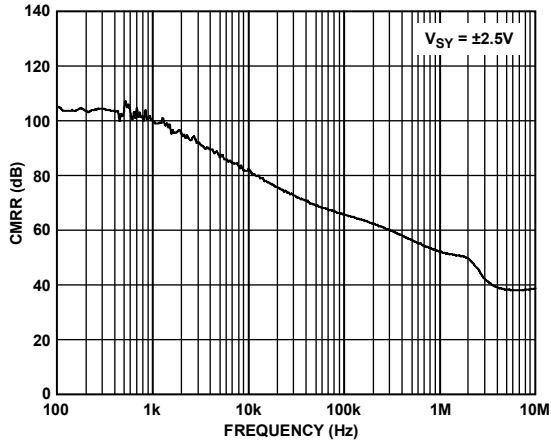


Figure 31. CMRR vs. Frequency

06276-032

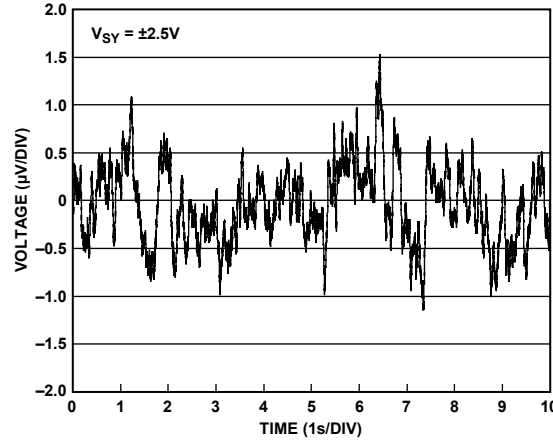


Figure 34. 0.1 Hz to 10 Hz Input Voltage Noise

06276-035

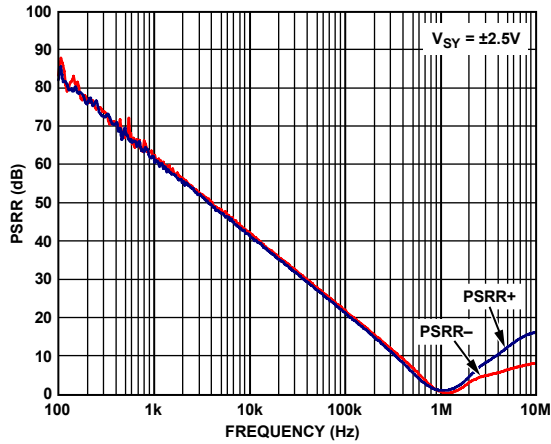


Figure 32. PSRR vs. Frequency

06276-033

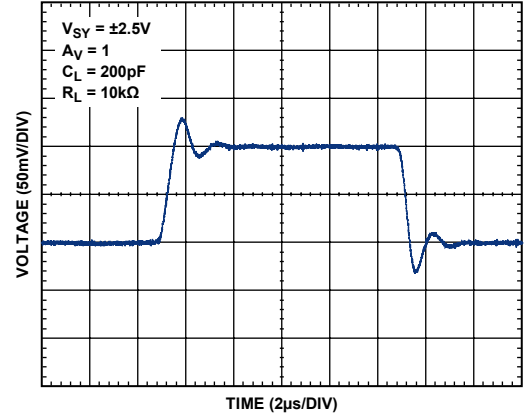


Figure 35. Small Signal Transient Response

06276-036

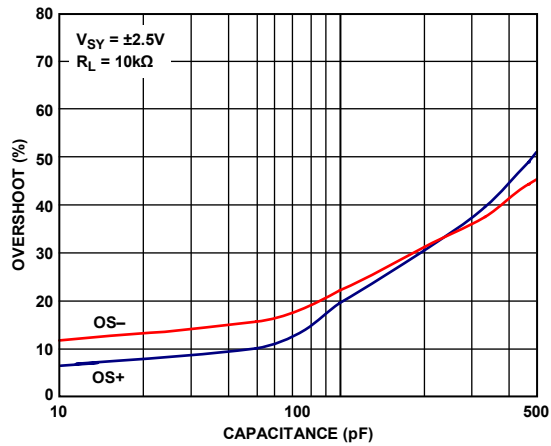


Figure 33. Small Signal Overshoot vs. Load Capacitance

06276-034

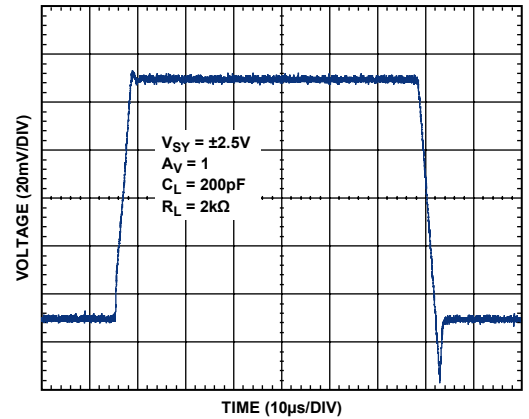


Figure 36. Large Signal Transient Response

06276-037

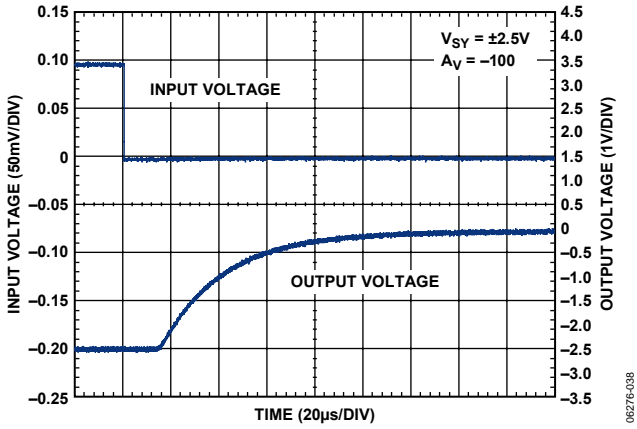


Figure 37. Positive Overload Recovery

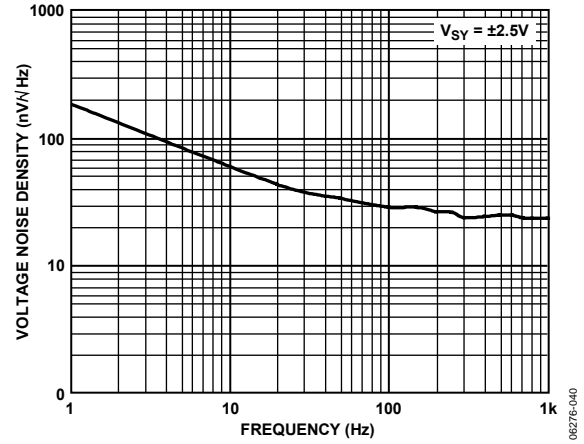


Figure 39. Voltage Noise Density vs. Frequency

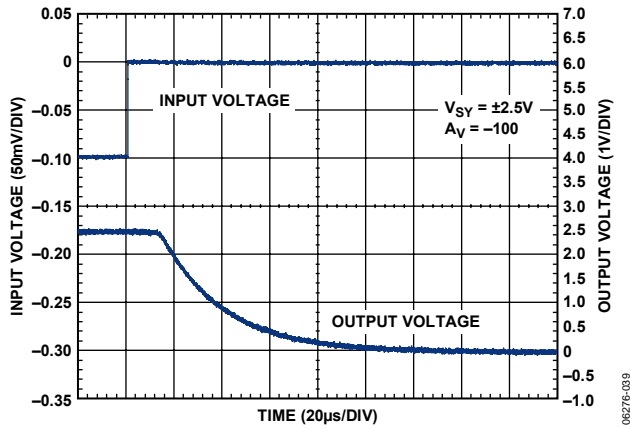


Figure 38. Negative Overload Recovery

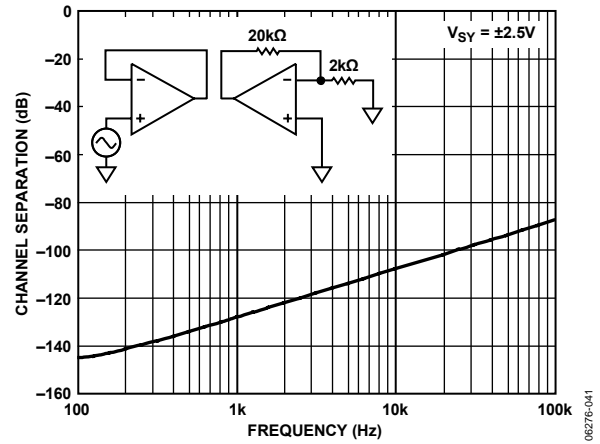
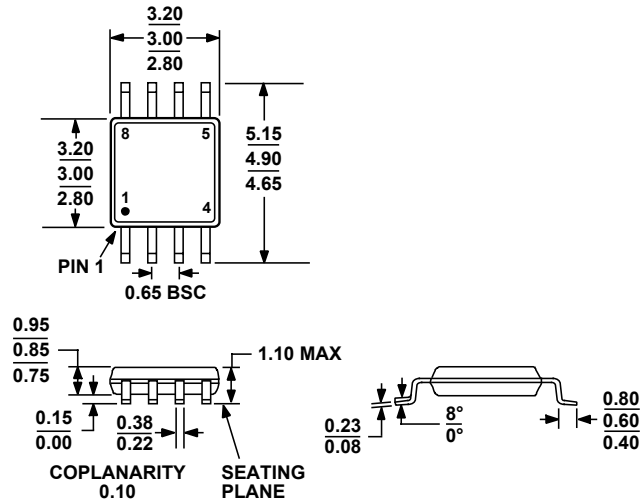


Figure 40. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

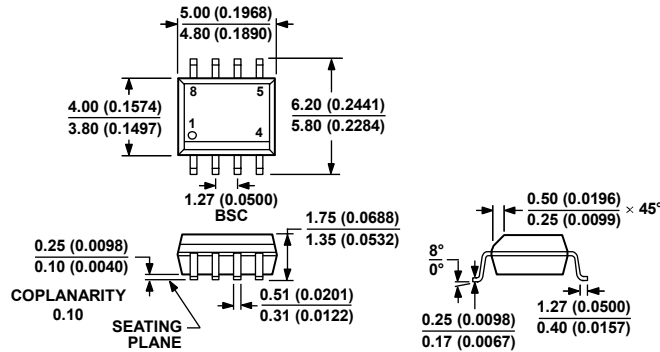


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 41. 8-Lead Mini Small Outline Package [MSOP]

(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 42. 8-Lead Standard Small Outline Package [SOIC_N]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8667ARMZ-R2 ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A1E
AD8667ARMZ-REEL ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A1E
AD8667ARZ ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8667ARZ-REEL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8667ARZ-REEL7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

¹ Z = RoHS Compliant Part.

AD8667

NOTES

NOTES

AD8667

NOTES