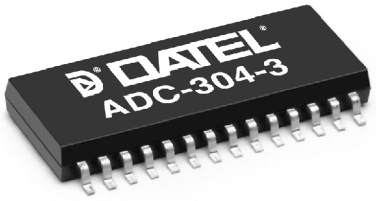
ADC-304

8-Bit, 20MHz, Low-Power Flash A/D Converters

FEATURES

- **8-bit resolution**
- **20MHz conversion rate**
- **±1/2LSB maximum nonlinearity**
- **8MHz input bandwidth**
- **Low power consumption, 375mW**
- **TTL compatible**
- **Single or dual supply operation**



GENERAL DESCRIPTION

Datel's ADC-304 is an 8-bit, 20MHz analog-to-digital flash converter. The ADC-304 offers many performance features not obtainable from other flash A/D's.

Key reatures include a low power dissipation of 375mW and TTL-compatible outputs. A wide analog input bandwidth of 8MHz (–3dB) allows operation without the need of a sample-hold. Also, single +5V supply operation is obtainable with an input range of +3 to +5V, eliminating the need for an additional power supply. A 0 to –2V input range is available with ±5V supply operation.

Another novel feature of the ADC-304 is its user-selectable output coding. The MINV and LINV pins allow selection of binary, complementary binary, and if external offset circuitry is used for bipolar inputs, offset binary, two's complement and complementary two's complement coding.

The ADC-304 is supplied in a 28-pin plastic DIP or a 28-pin plastic SOP package. Operating temperature range is –20 to +75°C. Storage temperature range is –55 to +150°C.

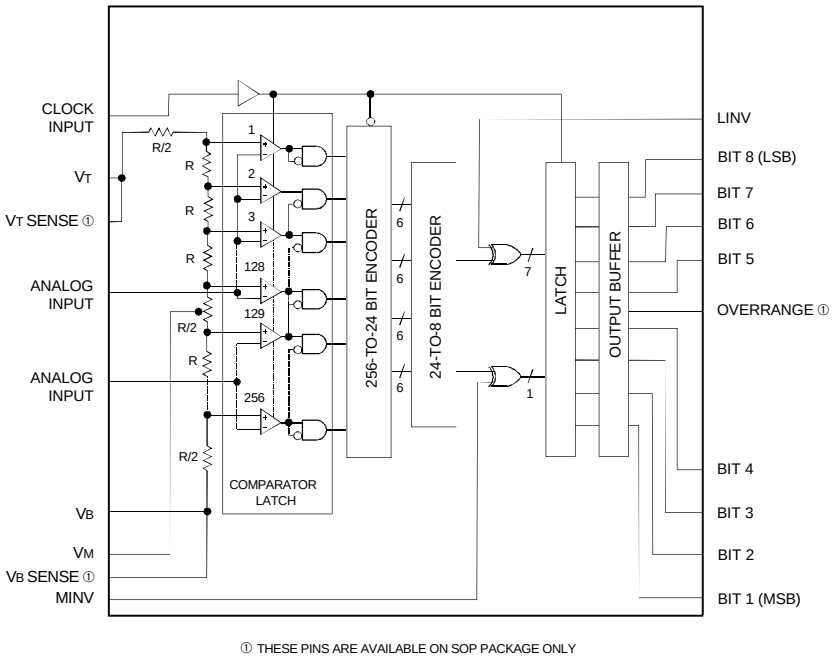


Figure 1. ADC-304 Functional Block Diagram

INPUT/OUTPUT CONNECTIONS PLASTIC DIP PACKAGE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	MINV
2	BIT 2	27	V_M
3	BIT 3	26	V_B
4	BIT 4	25	ANALOG GND
5	DIGITAL GND	24	NO CONNECT
6	+5V POWER	23	ANALOG INPUT
7	–5.2V POWER	22	NO CONNECT
8	–5.2V POWER	21	ANALOG INPUT
9	–5.2V POWER	20	NO CONNECT
10	+5V POWER	19	ANALOG GND
11	DIGITAL GND	18	V_T
12	LINV	17	CLOCK INPUT
13	BIT 5	16	BIT 8 (LSB)
14	BIT 6	15	BIT 7

INPUT/OUTPUT CONNECTIONS PLASTIC SOP PACKAGE

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG INPUT	28	ANALOG INPUT
2	V_B SENSE	27	V_T SENSE
3	ANALOG GND	26	ANALOG GND
4	V_B	25	V_T
5	V_M	24	CLOCK INPUT
6	NO CONNECT	23	BIT 8 (LSB)
7	MINV	22	BIT 7
8	BIT 1 (MSB)	21	BIT 6
9	BIT 2	20	BIT 5
10	BIT 3	19	LINV
11	BIT 4	18	DIGITAL GND
12	DIGITAL GND	17	+5V POWER
13	+5V POWER	16	OVERRANGE
14	–5.2V POWER	15	–5.2V POWER

ABSOLUTE MAXIMUM RATINGS

PARAMETERS		LIMITS	UNITS
Supply Voltages	$+V_S$ to GND	0 to +6	Volts
	$-V_S$ to GND	0 to –6	Volts
Input Voltage (Analog)	Vin (dual power supply)	$-V_S$ to (ANA GND + 0.3)	Volts
Input Voltage (Reference)	V_T, V_B, V_M (dual power supply)	$-V_S$ to (ANA GND + 0.3)	Volts
	$\lvert V_T - V_B \rvert$	2.5	Volts
Input Current	I_M	–3.0 to +3.0	mA
Input Voltage (Digital)	Digital Inputs	–0.5 to $+V_S$	Volts

FUNCTIONAL SPECIFICATIONS

Unless otherwise noted, the following specifications apply to the ADC-304 when used either with a single or dual power source. The test conditions are:

For single power supply operation:
$+V_S$ = +5V, DIG GND = 0V
$-V_S$ = 0V, V_T = +5V
V_B = +3V, T_A = +25°C
ANA GND = +5V, f_S = 20MHz

For dual power supply operation:
$+V_S$ = +5V, DIG GND = 0V
$-V_S$ = –5.2V, V_T = 0V,
V_B = –2V, T_A = +25°C
ANA GND = 0V, f_S = 20MHz

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Range	V_B		V_T	Volts
Input Capacitance	—	30	35	pF
Input Bias Current	15	50	100	µA
Offset Voltage				
V_T	–8	–13	–19	mV
V_B	0	+5	+11	mV
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Input Currents				
Logic "1"	—	–100	–150	µA
Logic "0"	–0.1	–0.32	–0.5	mA
PERFORMANCE				
Conversion Rate ①	20	—	—	MHz
Integral Nonlinearity	—	—	±1/2	LSB
Differential Nonlinearity	—	—	±1/2	LSB
Differential Gain Error ②	—	—	1.5	%
Differential Phase Error ②	—	—	0.5	degrees
Aperture Delay Ta	5	7	9	ns
Aperture Uncertainty	—	30	—	ps
Signal-to-Noise and Distortion				
(V_{in} = full scale, f_S = 20MHz)				
f_{in} = 1MHz		47		dB
f_{in} = 5MHz		43		dB
f_{in} = 10MHz		35		dB
Clock Pulse Width				
Tpw1	35	—	—	ns
Tpw0	10	—	—	ns
Reference Pin Current	11	15	18	mA
Reference Resistance (V_T to V_B)	—	130	—	Ohms
Reference Input (dual supply)				
V_T	–0.1	0	+0.1	Volts
V_B	–1.8	–2.0	–2.2	Volts

Footnotes:

① f_{in} = 1kHz, ramp

② NTSC 40 IRE-modulated ramp, f_S = 14.3MHz

DIGITAL OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution and Output Coding	8 Straight binary Complementary binary Two's complement Complementary two's complement			bits
Logic Levels				
Logic "1"	+2.7	+3.4	—	Volts
Logic "0"	—	—	+0.5	Volts
Logic Loading "1"	—	–500	—	µA
Logic Loading "0"	—	—	+3	mA
Output Data Delay				
TDLH	15	20	30	ns
TDHL	22	26	35	ns
POWER REQUIREMENTS				
Single Power Supply				
Supply Voltage = $+V_S$	+4.75	+5.0	+5.25	Volts
Supply Voltage = $-V_S$	—	0	—	Volts
Supply Current = $+I_S$	+56	+71	+91	mA
Power Dissipation	280	355	455	mW
Dual Power Supply				
Supply Voltage = $+V_S$	+4.75	+5.0	+5.25	Volts
Supply Voltage = $-V_S$	–4.75	–5.2	–5.5	Volts
Supply Current = $+I_S$	+7	+10	+14	mA
Supply Current = $-I_S$	–50	–62	–78	mA
Power Dissipation	295	375	476	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature	–20	—	+75	°C
Storage Temperature	–55	—	+150	°C

TECHNICAL NOTES

1. The two DIGITAL GND pins (pins 5 and 11 on the DIP, pins 12 and 18 on the SOP) are not connected to each other internally and neither are the two +5V POWER pins (6 and 10 on the DIP, 13 and 17 on the SOP). All four pins must be externally connected to the appropriate pcb patterns. Also, the DIGITAL GND and ANALOG GND pins are not connected to each other internally.

2. Layout of the analog and digital sections should be separated to reduce interference from noise. To further guard against unwanted noise, it is recommended to bypass, as close as possible, the voltage supply pins to their respective ground pins with 1µF tantalum and 0.01µF ceramic disk capacitors in parallel.

3. The input capacitance of the analog input is much smaller than that of a typical flash A/D converter. It is necessary to use an amplifier with sufficient bandwidth and driving power. The analog input pins are separated internally, so they should be connected together externally. If the ADC-304 is driven with a low output impedance amplifier, parasitic oscillations may occur.

   These parasitic oscillations can be prevented by introducing a small resistance of 2 to 10Ω between the amplifier output and the ADC-304's A/D input. This resistance must have a very low value of series inductance at high frequencies.

   Note that each of the analog input pins is divided in this manner with these resistances. Connect the driving amplifier as close as possible to the A/D input of the ADC-304.

4. The voltage between V_T and V_B is equivalent to the dynamic range of the analog input. Bypass V_B to ANALOG GND USING a 1µF and a 0.01µF capacitor in parallel. To balance the characteristics of the ADC-304 at high frequencies, bypass V_M with a 0.01µF capacitor to ANALOG GND.

   Also, V_M can be used as a trimming pin for more precise linearity compensation. A stable voltage source with a potential equal to V_B and a 1kΩ potentiometer can be connected to V_M as shown in Figure 2 for this purpose.

5. Separate the clock input, CLOCK, from other leads as much as possible, observing proper EMI and RFI wiring techniques. This reduces the inductive pick-up of this lead from interfering with the "clean" operation of the ADC-304.

6. The analog input signal is sampled on the positive-going edge of CLOCK. Corresponding digital data appears at the output on the negative-going edge of the CLOCK pulse after a brief delay of 31ns maximum (TDLH, TDHL). Refer to the Timing Diagram (Figure 3) for more information.

7. Connect all free pins to ANALOG GND to reduce unwanted noise.

   The analog input range is equal to a 2V spread. The voltage on V_T-V_B will equal 2V. The connection of V_T and ANALOG GND is 2V higher than V_B. Whether using a single or dual power supply, the analog input will range from the value of V_T to V_B. If V_T equals +5V, then V_B will equal +3V and the analog input range will be from +3 to +5V.

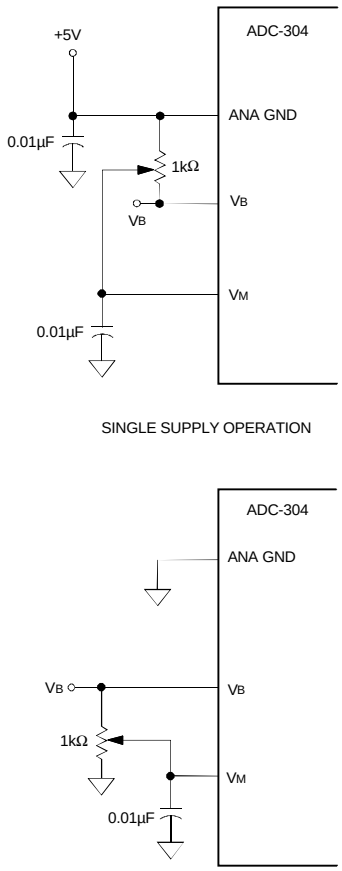


Figure 2.
Improving Linearity Compensation

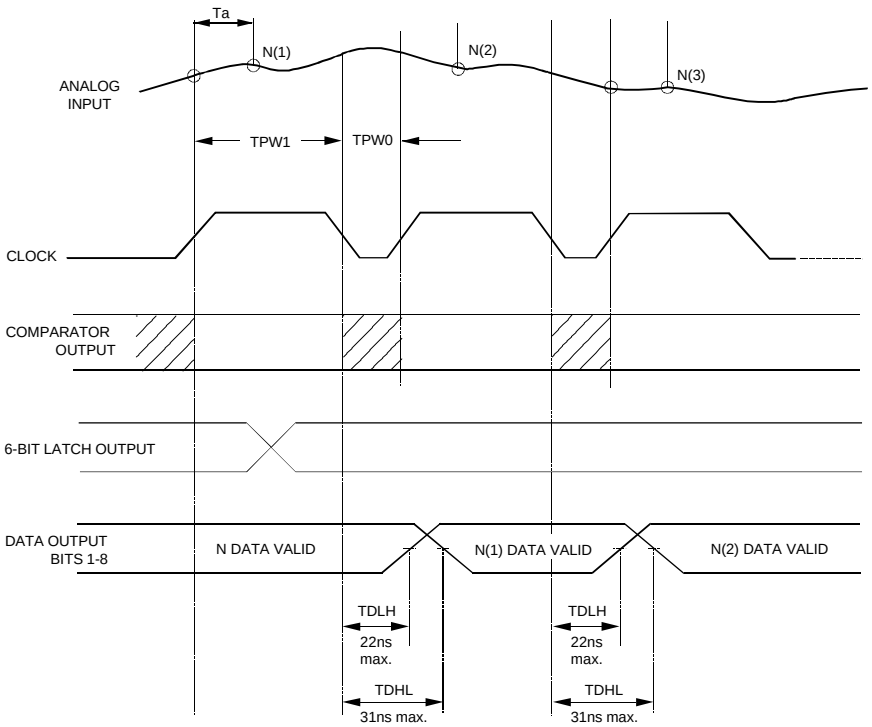


Figure 3. ADC-304 Timing Diagram

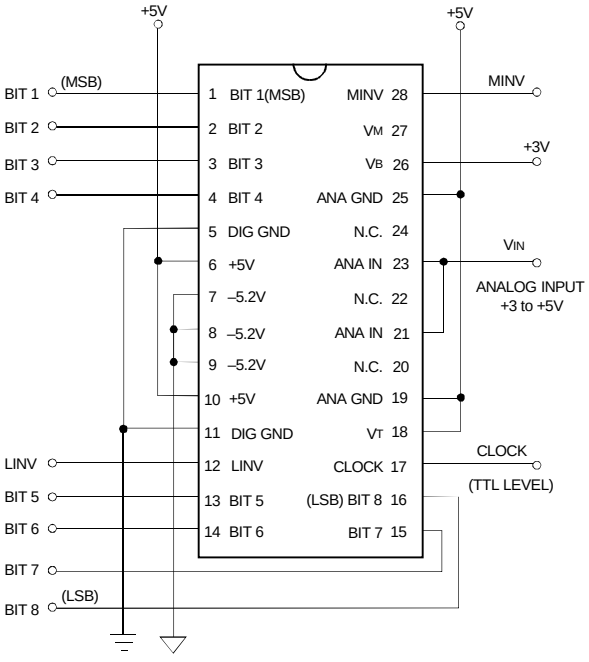
Table 1. Output Coding for +5V Power Supply Operation (+3 to +5V Signal Input)

		Straight Binary	Complementary Two's Complement	Two's Complement	Complementary Binary
Unipolar	**MINV**	**0**	**0**	**1**	**1**
Scale	**LINV**	**0**	**1**	**0**	**1**
+FS – 1SLB	+4.9922V	11111111	10000000	01111111	00000000
+7/8FS	+4.7500V	11011111	10100000	01011111	00100000
+3/4FS	+4.5000V	10111111	11000000	00111111	01000000
+1/2FS	+4.0000V	01111111	00000000	11111111	10000000
+1/4FS	+3.5000V	00111111	01000000	10111111	11000000
+1/8FS	+3.2500V	00011111	01100000	10011111	11100000
+1LSB	+3.0078V	00000001	01111110	10000001	11111110
Zero	+3.0000V	00000000	01111111	10000000	11111111

Table 2. Output Coding for ±5V Power Supply Operation (0 to –2V Signal Input)

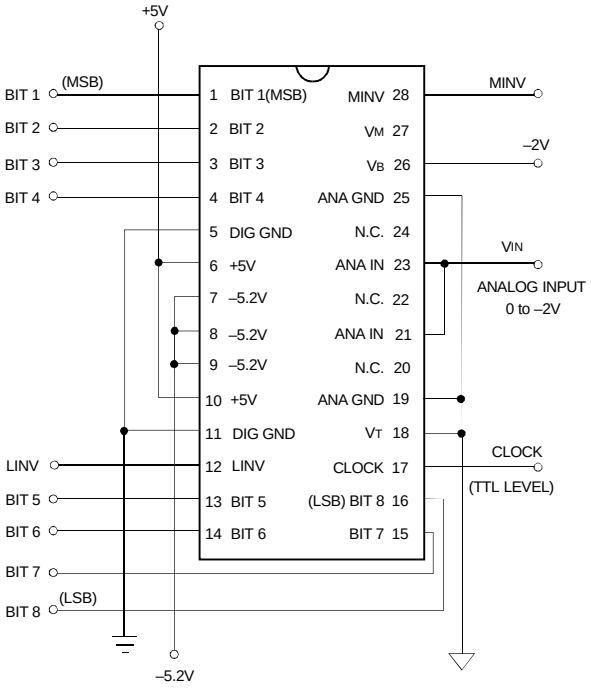
		Straight Binary	Complementary Two's Complement	Two's Complement	Complementary Binary
Unipolar	**MINV**	**0**	**0**	**1**	**1**
Scale	**LINV**	**0**	**1**	**0**	**1**
Zero	0.0000V	11111111	10000000	01111111	00000000
–1LSB	–0.0078V	11111110	10000001	01111110	00000001
–1/8FS	–0.2500V	11011111	10100000	01011111	00100000
–1/4FS	–0.5000V	10111111	11000000	00111111	01000000
–1/2FS	–1.0000V	01111111	00000000	11111111	10000000
–3/4FS	–1.5000V	00111111	01000000	10111111	11000000
–7/8FS	–1.7500V	00011111	01100000	10011111	11100000
–FS + 1SLB	–1.9922V	00000000	01111111	10000000	11111111

APPLICATION CIRCUITS



NOTE: 28-pin DIP package shown

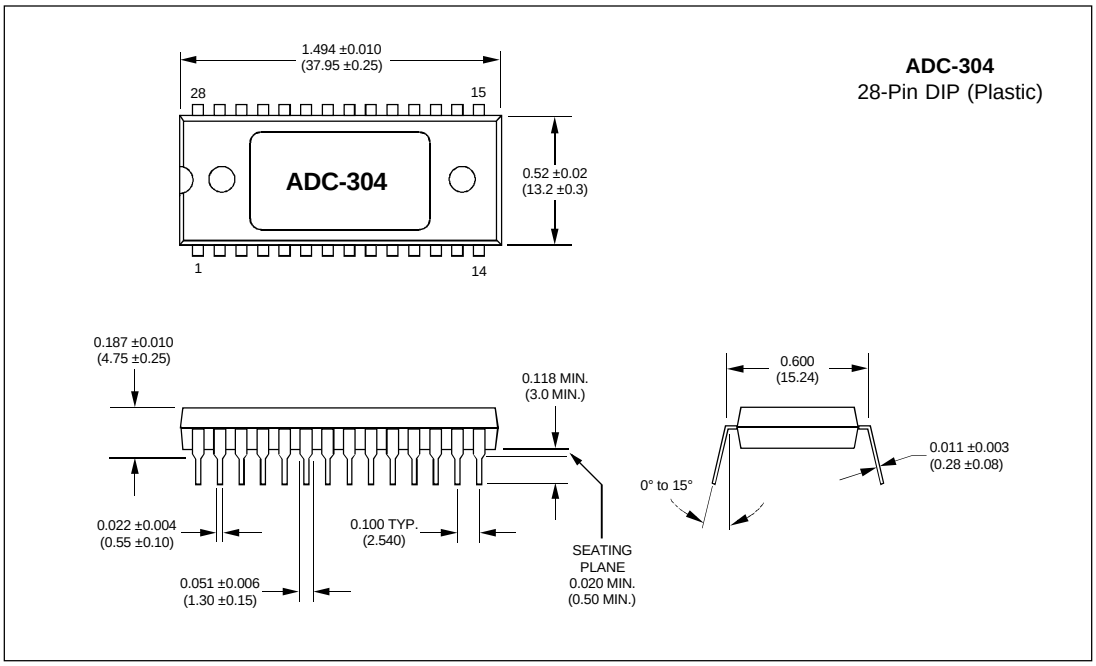
Figure 4. Connections for +5V Power Supply Operation

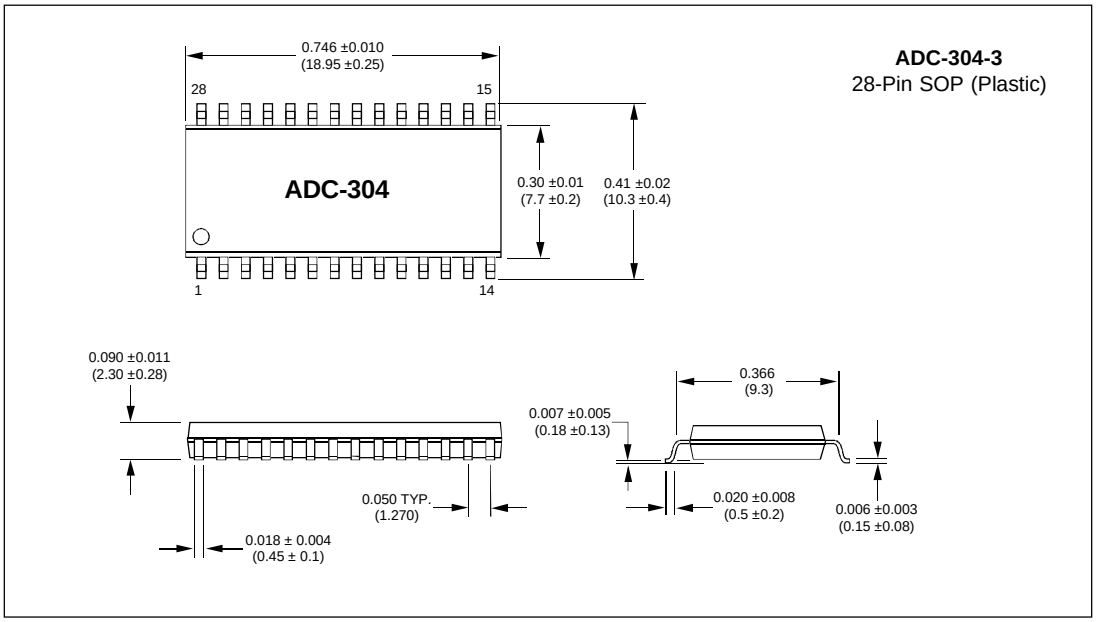


NOTE: 28-pin DIP package shown

Figure 5. Connections for ±5V Power Supply Operation

MECHANICAL DIMENSIONS





ORDERING INFORMATION

MODEL	PACKAGE
ADC-304	28-pin DIP (plastic)
ADC-304-3	28-pin SOP (plastic)

INNOVATION and EXCELLENCE

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DS-0075B 10/96

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