

ADC0819 8-Bit Serial I/O A/D Converter with 19-Channel Multiplexer

General Description

The ADC0819 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 19 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

- Separate asynchronous converter clock and serial data I/O clock.
- 19-Channel multiplexer with 5-Bit serial address logic.
- Built-in sample and hold function.

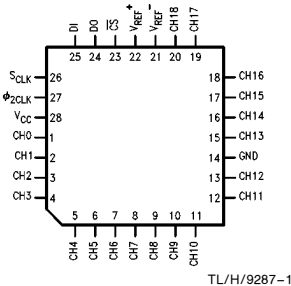
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- TTL/MOS input/output compatible.
- 28-pin molded chip carrier or 28-pin molded DIP

Key Specifications

- Resolution 8-Bits
- Total unadjusted error $\pm 1/2$ LSB and ± 1 LSB
- Single supply 5V_{DC}
- Low Power 15 mW
- Conversion Time 16 μ s

Connection Diagrams Functional Diagram

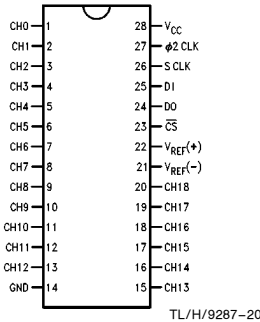
Molded Chip Carrier (PCC) Package



Top View

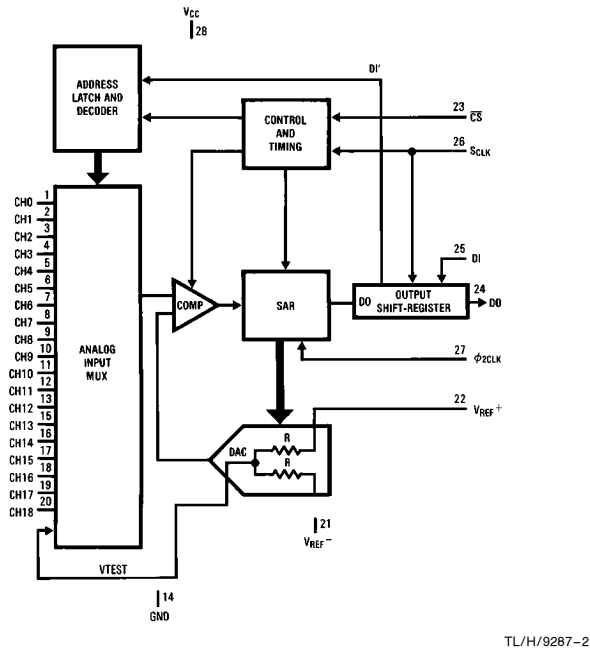
Order Number ADC0819BCV, CCV
See NS Package Number V28A

Dual-In-Line Package



Top View

Order Number ADC0819BCN, CIN
See NS Package Number N28B



TL/H/9287-2

ADC0819 8-Bit Serial I/O A/D Converter with 19-Channel Multiplexer

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Inputs and Outputs	-0.3V to $V_{CC} + 0.3V$
Input Current Per Pin (Note 3)	$\pm 5mA$
Total Package Input Current (Note 3)	$\pm 20mA$
Storage Temperature	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ C$	875 mW

Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 11)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0819BCV, ADC0819CCV	-40°C $\leq T_A \leq$ +85°C
ADC0819BCN	0°C $\leq T_A \leq$ +70°C
ADC0819CIN	-40°C $\leq T_A \leq$ +85°C

Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $\phi_2 CLK = 2.097 MHz$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$.

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Maximum Total Unadjusted Error ADC0819BCV, BCN ADC0819CCV, CIN	$V_{REF} = 5.00 V_{DC}$ (Note 4)		$\pm 1/2$ ± 1	$\pm 1/2$ ± 1	LSB LSB
Minimum Reference Input Resistance		8		5	k Ω
Maximum Reference Input Resistance		8	11	11	k Ω
Maximum Analog Input Range	(Note 5)		$V_{CC} + 0.05$	$V_{CC} + 0.05$	V
Minimum Analog Input Range			$GND - 0.05$	$GND - 0.05$	V
On Channel Leakage Current	(Note 9) On Channel = 5V Off Channel = 0V		400	1000	nA
	On Channel = 0V Off Channel = 5V (Note 9)		-400	-1000	nA
Off Channel Leakage Current	(Note 9) On Channel = 5V Off Channel = 0V		-400	-1000	nA
	On Channel = 0V Off Channel = 5V (Note 9)		400	1000	nA
Minimum V_{TEST} Internal Test Voltage	$V_{REF} = V_{CC}$, CH 19 Selected		125	125	(Note 10) Counts
Maximum V_{TEST} Internal Test Voltage	$V_{REF} = V_{CC}$, CH 19 Selected		130	130	(Note 10) Counts
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC} = 5.25V$		2.0	2.0	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC} = 4.75V$		0.8	0.8	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN} = 5.0V$	0.005	2.5	2.5	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	-0.005	-2.5	-2.5	μA

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $\phi_2 CLK = 2.097$ MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$.

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360 \mu A$ $I_{OUT} = -10 \mu A$		2.4	2.4	V
			4.5	4.5	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 5.25V$ $I_{OUT} = 1.6 mA$		0.4	0.4	V
I_{OUT} , TRI-STATE Output Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	-0.01	-3	-3	μA
		0.01	3	3	μA
I_{SOURCE} , Output Source Current (Min)	$V_{OUT} = 0V$	-14	-6.5	-6.5	mA
I_{SINK} , Output Sink Current (Min)	$V_{OUT} = V_{CC}$	16	8.0	8.0	mA
I_{CC} , Supply Current (Max)	$\overline{CS} = 1$, V_{REF} Open	1	2.5	2.5	mA
I_{REF} (Max)	$V_{REF} = 5V$	0.7	1	1	mA

AC CHARACTERISTICS

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units	
$\phi_2 CLK$, ϕ_2 Clock Frequency	MIN	0.70		1.0	MHz	
	MAX	4.0	2.0	2.1		
S_{CLK} , Serial Data Clock Frequency	MIN			5.0	KHz	
	MAX	1000	525	525		
T_C , Conversion Process Time	MIN	Not Including MUX Addressing and Analog Input Sampling Times	26		26	ϕ_2 cycles
	MAX		32		32	
t_{ACC} , Access Time Delay From \overline{CS} Falling Edge to DO Data Valid	MIN				1	ϕ_2 cycles
	MAX				3	
t_{SET-UP} , Minimum Set-up Time of \overline{CS} Falling Edge to S_{CLK} Rising Edge					$4/\phi_2 CLK + \frac{1}{2 S_{CLK}}$	sec
$t_{H\overline{CS}}$, \overline{CS} Hold Time After the Falling Edge of S_{CLK}					0	ns
$t_{\overline{CS}}$, Total \overline{CS} Low Time	MIN				$t_{set-up} + 8/S_{CLK}$	sec
	MAX				$t_{CS(min)} + 26/\phi_2 CLK$	sec
t_{HDI} , Minimum DI Hold Time from S_{CLK} Rising Edge			0		0	ns
t_{HDO} , Minimum DO Hold Time from S_{CLK} Falling Edge	$R_L = 30k$, $C_L = 100 pF$				10	ns
t_{SDI} , Minimum DI Set-up Time to S_{CLK} Rising Edge		200			400	ns
t_{DDO} , Maximum Delay From S_{CLK} Falling Edge to DO Data Valid	$R_L = 30k$, $C_L = 100 pF$	180	200		250	ns
t_{TRI} , Maximum DO Hold Time, (\overline{CS} Rising edge to DO TRI-STATE)	$R_L = 3k$, $C_L = 100 pF$	90	150		150	ns

Electrical Characteristics The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20\text{ ns}$, $V_{REF} = 5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$.

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units	
AC CHARACTERISTICS (Continued)						
t_{CA} , Analog Sampling Time	After Address Is Latched $\overline{CS} = \text{Low}$			$3/S_{CLK} + 1\ \mu\text{s}$	sec	
t_{RDO} , Maximum DO Rise Time	$R_L = 30\text{ k}\Omega$, $C_L = 100\text{ pf}$	“TRI-STATE” to “HIGH” State	75	150	150	ns
		“LOW” to “HIGH” State	150	300	300	
t_{FDO} , Maximum DO Fall Time	$R_L = 30\text{ k}\Omega$, $C_L = 100\text{ pf}$	“TRI-STATE” to “LOW” State	75	150	150	ns
		“HIGH” to “LOW” State	150	300	300	
C_{IN} , Maximum Input Capacitance	Analog Inputs, AN0–AN10 and V_{REF}	11		55	pF	
	All Others	5		15		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Under over voltage conditions ($V_{IN} < 0V$ and $V_{IN} > V_{CC}$) the maximum input current at any one pin is $\pm 5\text{ mA}$. If the voltage at more than one pin exceeds $V_{CC} + .3V$ the total package current must be limited to 20 mA. For example the maximum number of pins that can be over driven at the maximum current level of $\pm 5\text{ mA}$ is four.

Note 4: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 5: Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of $4.950 V_{DC}$ over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Note 8: Design Limits are guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

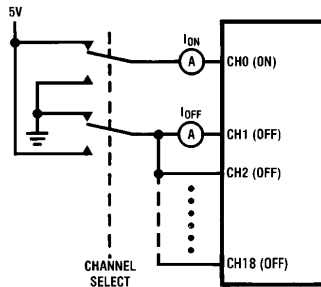
Note 9: Channel leakage current is measured after the channel selection.

Note 10: 1 count = $V_{REF}/256$.

Note 11: Human body model; 100 pF discharged through a 1.5 k Ω resistor.

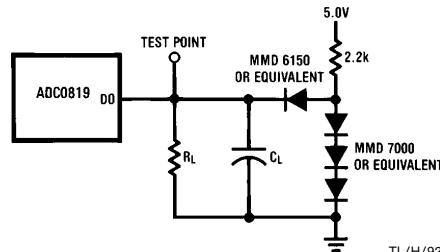
Test Circuits

Leakage Current



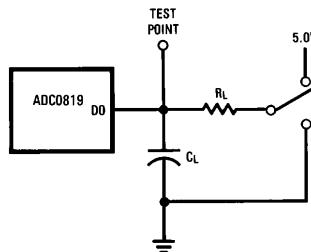
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D0 Except “TRI-STATE”



TL/H/9287-4

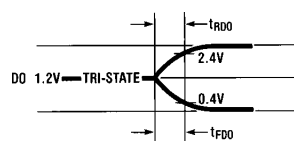
t_{TRI} “TRI-STATE”



TL/H/9287-5

Timing Diagrams

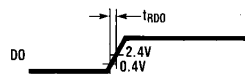
D0 “TRI-STATE” Rise & Fall Times



TL/H/9287-6

Timing Diagrams (Continued)

D0 Low to High State



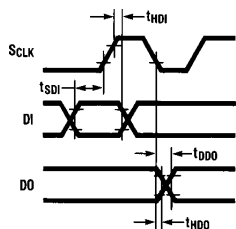
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D0 High to Low State



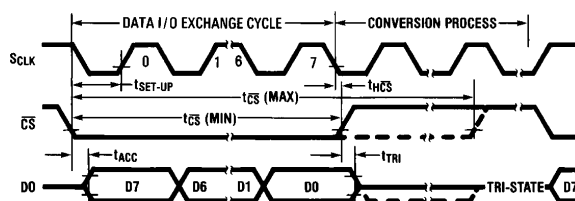
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Data Input and Output Timing



TL/H/9287-9

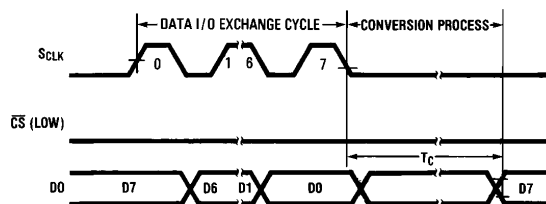
Timing with a continuous SCLK



TL/H/9287-10

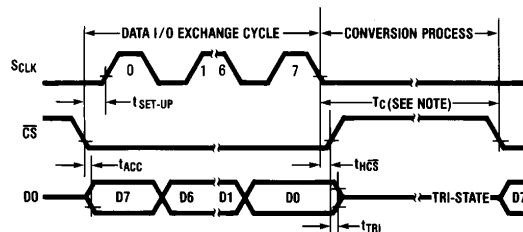
*Strobing \overline{CS} High and Low will abort the present conversion and initiate a new serial I/O exchange.

Timing with a gated SCLK and \overline{CS} Continuously Low



TL/H/9287-11

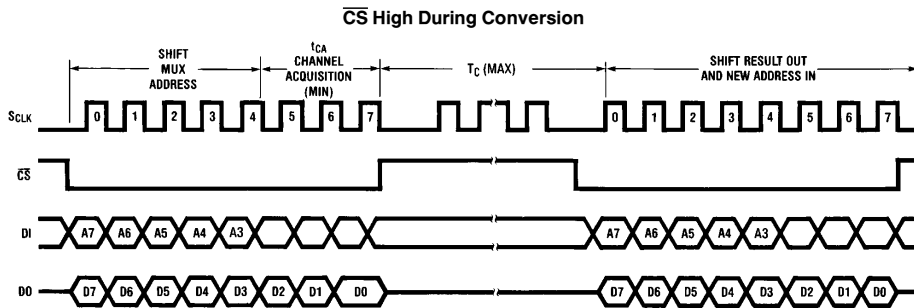
Using \overline{CS} To TRI-STATE D0



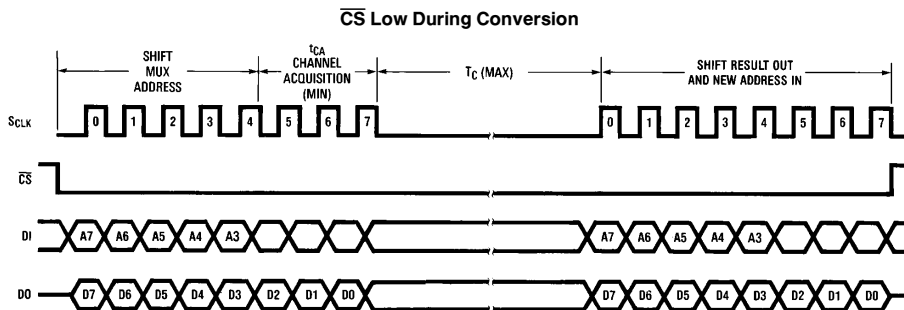
TL/H/9287-12

Note: Strobing \overline{CS} Low during this time interval will abort the conversion in process.

Timing Diagrams (Continued)



TL/H/9287-13



TL/H/9287-14

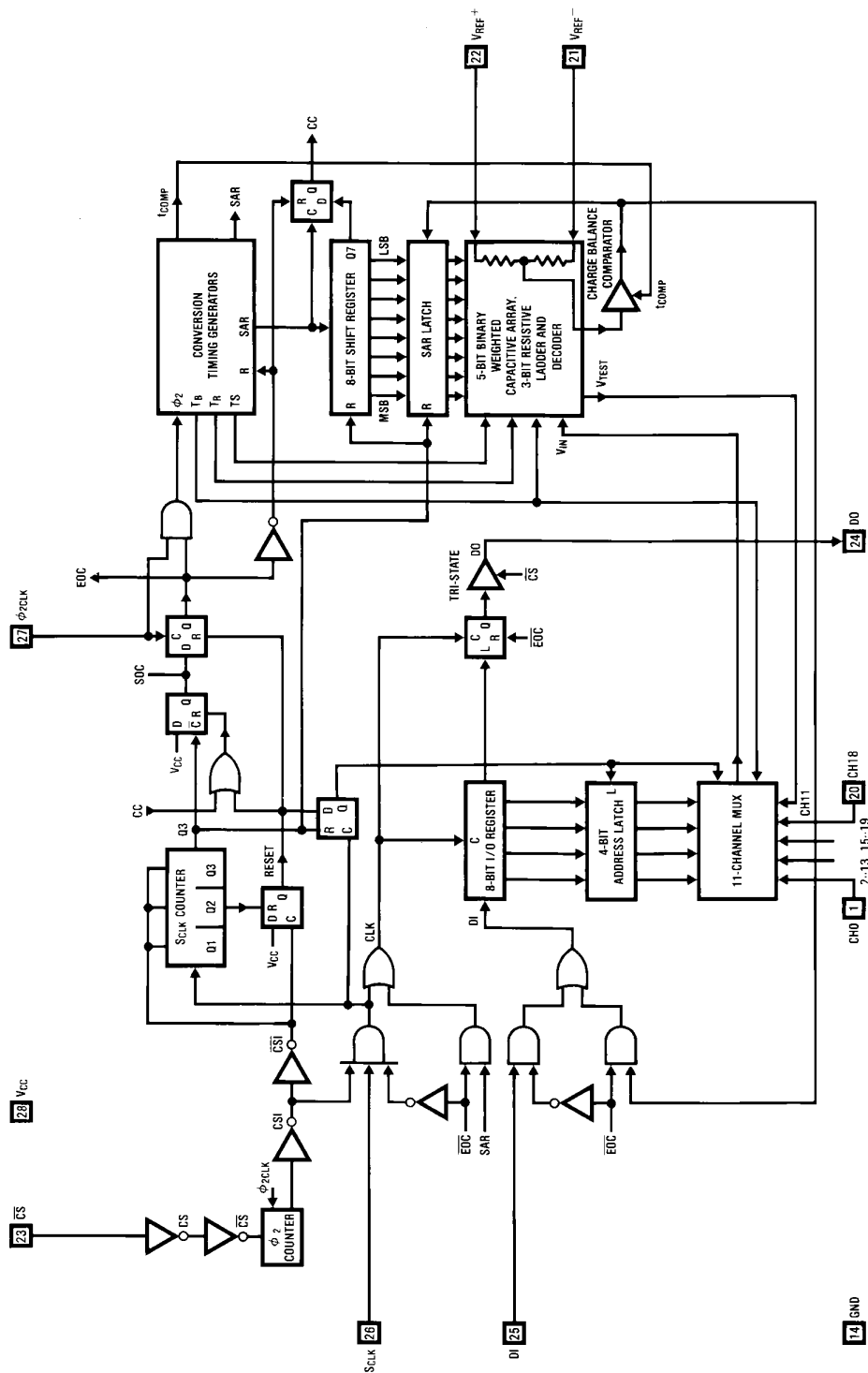
Channel Addressing Table

TABLE I. ADC 0819 Channel Addressing

MUX ADDRESS								ANALOG CHANNEL SELECTED
A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	X	X	X	CH0
0	0	0	0	1	X	X	X	CH1
0	0	0	1	0	X	X	X	CH2
0	0	0	1	1	X	X	X	CH3
0	0	1	0	0	X	X	X	CH4
0	0	1	0	1	X	X	X	CH5
0	0	1	1	0	X	X	X	CH6
0	0	1	1	1	X	X	X	CH7
0	1	0	0	0	X	X	X	CH8
0	1	0	0	1	X	X	X	CH9
0	1	0	1	0	X	X	X	CH10
0	1	0	1	1	X	X	X	CH11
0	1	1	0	0	X	X	X	CH12
0	1	1	0	1	X	X	X	CH13
0	1	1	1	0	X	X	X	CH14
0	1	1	1	1	X	X	X	CH15
1	0	0	0	0	X	X	X	CH16
1	0	0	0	1	X	X	X	CH17
1	0	0	1	0	X	X	X	CH18
1	0	0	1	1	X	X	X	V _{TEST}
1	0	1	0	0	X	X	X	No Channel Select
1	0	1	0	1	X	X	X	No Channel Select
1	0	1	1	0	X	X	X	No Channel Select
1	0	1	1	1	X	X	X	No Channel Select
1	1	X	X	X	X	X	X	Logic Test Mode*

*Analog channel inputs CH0 thru CH4 are logic outputs

Functional Block Diagram



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Functional Description

1.0 DIGITAL INTERFACE

The ADC0819 uses five input/output pins to implement the serial interface. Taking chip select (\overline{CS}) low enables the I/O data lines (DO and DI) and the serial clock input (SCLK). The result of the last conversion is transmitted by the A/D on the DO line, while simultaneously the DI line receives the address data that selects the mux channel for the next conversion. The mux address is shifted in on the rising edge of SCLK and the conversion data is shifted out on the falling edge. It takes eight SCLK cycles to complete the serial I/O. A second clock (ϕ_2) controls the SAR during the conversion process and must be continuously enabled.

1.1 CONTINUOUS SCLK

With a continuous SCLK input \overline{CS} must be used to synchronize the serial data exchange (see Figure 1). The ADC0819 recognizes a valid \overline{CS} one to three ϕ_2 clock periods after the actual falling edge of \overline{CS} . This is implemented to ensure noise immunity of the \overline{CS} signal. Any spikes on \overline{CS} less than one ϕ_2 clock period will be ignored. \overline{CS} must remain low during the complete I/O exchange which takes eight SCLK cycles. Although \overline{CS} is not immediately acknowledged for the purpose of starting a new conversion, the falling edge of \overline{CS} immediately enables DO to output the MSB (D7) of the previous conversion.

The first SCLK rising edge will be acknowledged after a set-up time (t_{set-up}) has elapsed from the falling edge of \overline{CS} . This and the following seven SCLK rising edges will shift in the channel address for the analog multiplexer. Since there are 19 channels only five address bits are utilized. The first five SCLK cycles clock in the mux address, during the next three SCLK cycles the analog input is selected and sampled. During

this mux address/sample cycle, data from the last conversion is also clocked out on DO. Since D7 was clocked out on the falling edge of \overline{CS} only data bits D6–D0 remain to be received. The following seven falling edges of SCLK shift out this data on DO.

The 8th SCLK falling edge initiates the beginning of the A/D's actual conversion process which takes between 26 and 32 ϕ_2 cycles (T_C). During this time \overline{CS} can go high to TRISTATE DO and disable the SCLK input or it can remain low. If \overline{CS} is held low a new I/O exchange will not start until the conversion sequence has been completed, however once the conversion ends serial I/O will immediately begin. Since there is an ambiguity in the conversion time (T_C) synchronizing the data exchange is impossible. Therefore \overline{CS} should go high before the 26th ϕ_2 clock has elapsed and return low after the 32nd ϕ_2 to synchronize serial communication.

A conversion or I/O operation can be aborted at any time by strobing \overline{CS} . If \overline{CS} is high or low less than one ϕ_2 clock it will be ignored by the A/D. If the \overline{CS} is strobed high or low between 1 to 3 ϕ_2 clocks the A/D may or may not respond. Therefore \overline{CS} must be strobed high or low greater than 3 ϕ_2 clocks to ensure recognition. If a conversion or I/O exchange is aborted while in process the consequent data output will be erroneous until a complete conversion sequence has been implemented.

1.2 DISCONTINUOUS SCLK

Another way to accomplish synchronous serial communication is to tie \overline{CS} low continuously and disable SCLK after its 8th falling edge (see Figure 2). SCLK must remain low for

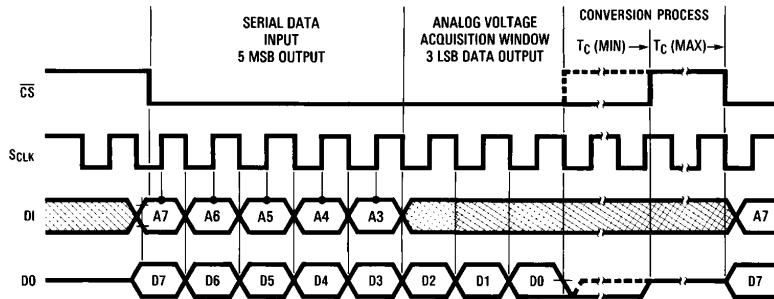


FIGURE 1

TL/H/9287-16

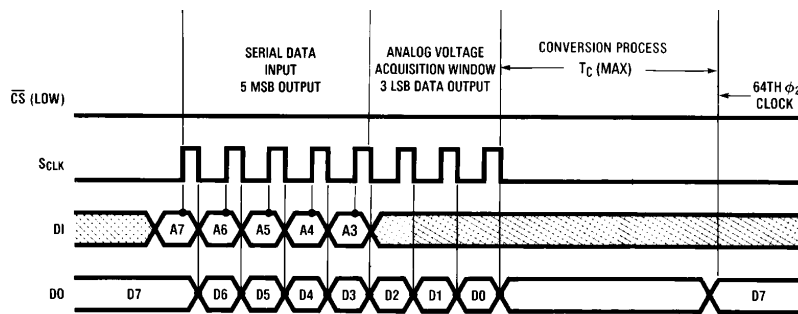


FIGURE 2

TL/H/9287-17

Functional Description (Continued)

at least $32 \phi_2$ clocks to ensure that the A/D has completed its conversion. If S_{CLK} is enabled sooner, synchronizing to the data output on DO is not possible since an end of conversion signal from the A/D is not available and the actual conversion time is not known. With \overline{CS} low during the conversion time ($32 \phi_2$ max) DO will go high or low after the eighth falling edge of S_{CLK} until the conversion is completed. Once the conversion is through DO will transmit the MSB. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously.

If \overline{CS} goes high during the conversion sequence DO is tristated, and the result is not affected so long as \overline{CS} remains high until the end of the conversion.

1.2 MULTIPLEXER ADDRESSING

The five bit mux address is shifted, MSB first, into DI. Input data corresponds to the channel selected as shown in table 1. Care should be taken not to send an address greater than or equal to twenty four (11XXX) as this puts the A/D in a digital testing mode. In this mode the analog inputs CH0 thru CH4 become digital outputs, for our use in production testing.

2.0 ANALOG INPUT

2.1 THE INPUT SAMPLE AND HOLD

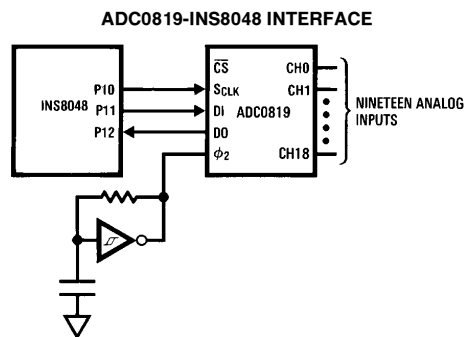
The ADC0819's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for $1 \mu\text{sec}$ after the

eighth S_{CLK} falling edge. The hold mode is initiated with the start of the conversion process. An acquisition window of $3t_{S_{CLK}} + 1 \mu\text{sec}$ is therefore available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (3K) of the multiplexer switches and the total ladder capacitance (90pf). These values yield an acquisition time of about $2 \mu\text{sec}$ for a full scale reading. Therefore the analog input must be stable for at least $2 \mu\text{sec}$ before and $1 \mu\text{sec}$ after the eighth S_{CLK} falling edge to ensure a proper conversion. External input source resistance and capacitance will lengthen the acquisition time and should be accounted for.

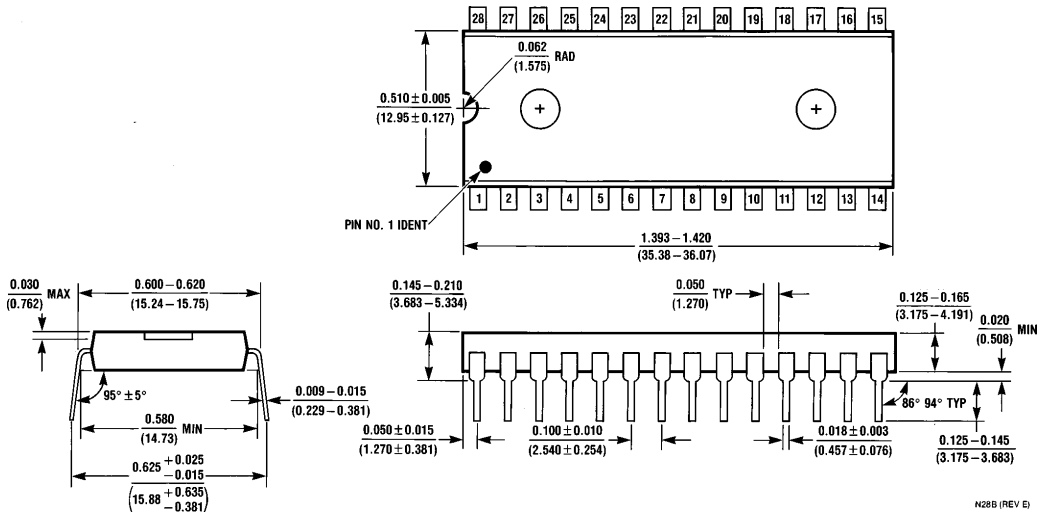
Other conventional sample and hold error specifications are included in the error and timing specs of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC0819's total unadjusted error, while the hold settling time is included in the A/D's max conversion time of $32 \phi_2$ clock periods. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

Typical Applications



TL/H/9287-18

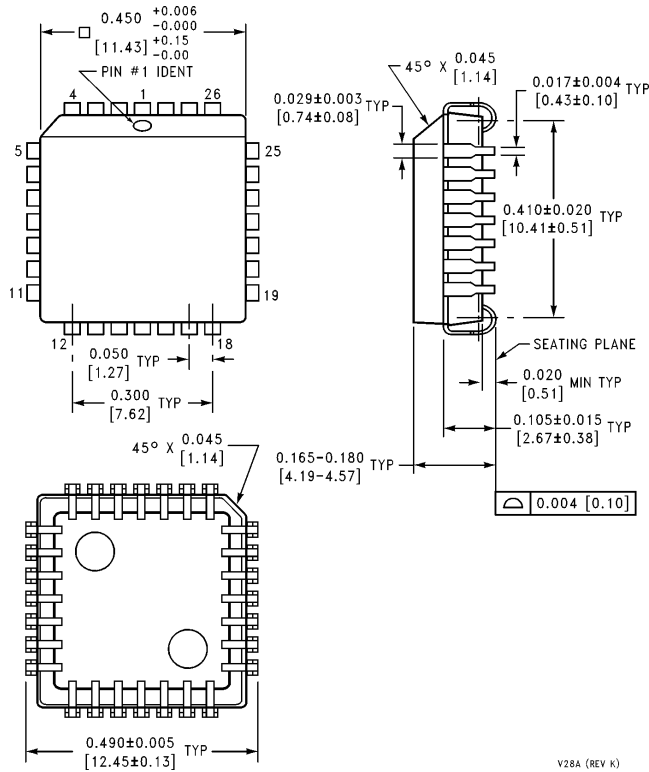
Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number ADC0819BCN or ADC0819CIN
NS Package Number N28B

N28B (REV D)

Physical Dimensions inches (millimeters) (Continued)



V28A (REV K)

Molded Chip Carrier (V)
Order Number ADC0819BCV, CCV
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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