

# Olive Family

## **ADM6308 - Eight-port 10/100M Ethernet Switch Controller**

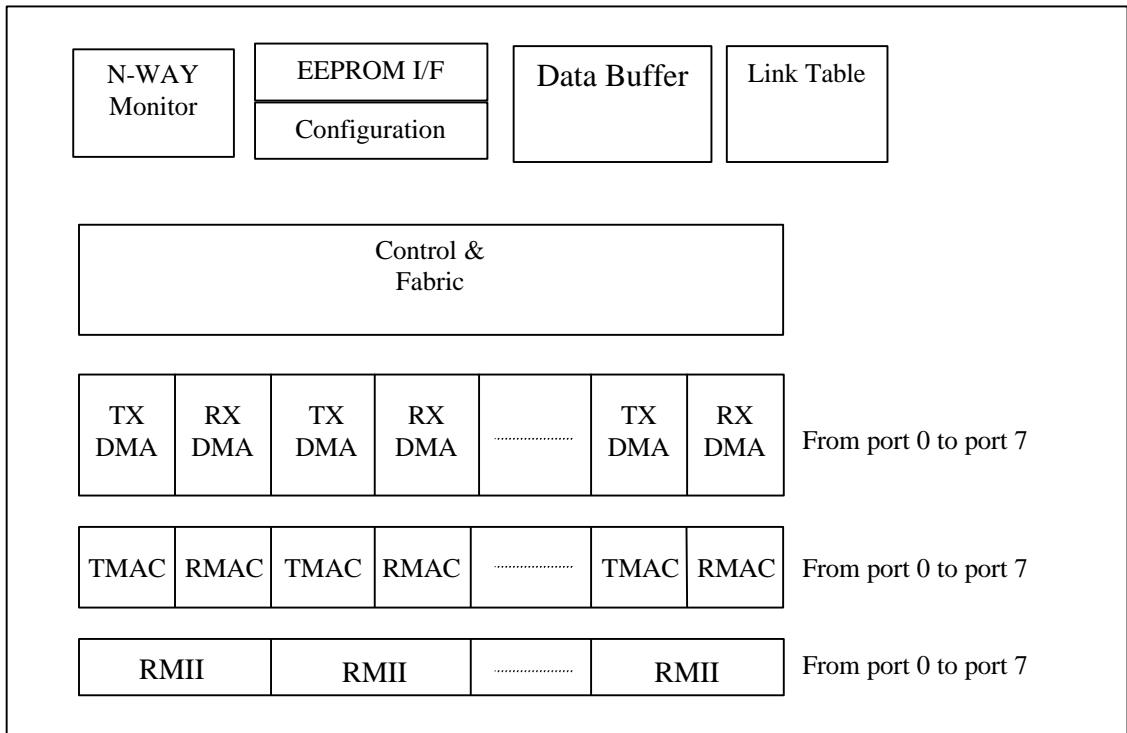
### **Overview**

ADM6308, a single chip, is a 10/100Mbps eight-port stand-alone switching controller with built-in data buffer memory which provides low cost and simple solution through a high integration design. Eight Reduced MII interfaces are designed for 10BASE/100BASE ports. MAC controller, switch engines and data buffer memory are built-in. The chip can fit to desktop or SOHO applications, and each 10/100M port directly connects either 10BASE or 100BASE devices. Additionally, ADM6308 breaks the distance limitation of 10BASE or any class 100BASE repeaters, and increases throughput.

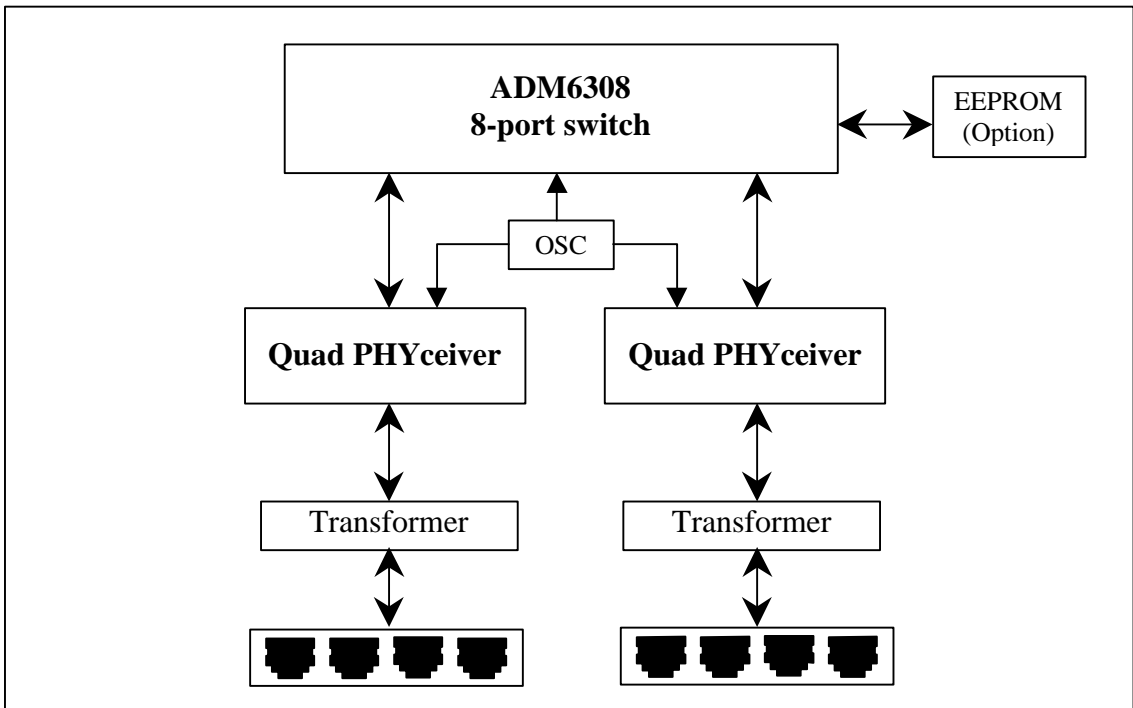
### **Features**

- ⇒ Non-blocking eight-port 10/100M switching controller with MAC controller and switching engine included low cost and a simple solution for 100BASE-TX, 100BASE-FX, and 10BASE applications.
- ⇒ Configurable 10/100BASE Reduced MII interfaces and 1MII+ 7RMII mode provided.
- ⇒ The single clock input, 50M, for RMII and system
- ⇒ Speed auto negotiation function for all ports
- ⇒ Store-and-forward operation support.
- ⇒ Full line speed capability of 14880 packet/sec for 10M and 148810 packet/sec for 100M, with no HOL blocking.
- ⇒ Broadcast storming prevention
- ⇒ Support 4 groups port-based VLAN.
- ⇒ Full-duplex (IEEE802.3x) and three-way half-duplex flow control (Back pressure).
- ⇒ Data buffer SSRAM embedded,
- ⇒ CoS support: Port-based, VLAN tag, TCP/IP TOS/DS.
- ⇒ Intelligently back-pressure and flow control turned on/off in the port with priority frames
- ⇒ Buffer management included.
- ⇒ 93C46 EEPROM interface or Dynamic configured by 8051
- ⇒ Buffer full and faulty LED provided.
- ⇒ Bridging functions such as:
  - ◆ Local MAC address filtering.
  - ◆ CRC or direct mapping hashing schemes for better address coverage.
  - ◆ Short routing decision time.
  - ◆ Aging function included with configurable aging time.
  - ◆ Embedded 1K entries of address table.
- ⇒ Low power 2.5 V CMOS technology with 3.3V tolerance I/O
- ⇒ 100-pins Plastic Quad Flat Package.

**Block Diagram**



**Example of System Diagram**



Pin Diagram



## Pin Descriptions

| Pin Name   | Pin #   | Type      | Descriptions  |
|--|---|-----------|---|
| <b>EEPROM Interface</b>  |   |           |   |
| EEDO   | 51  | I         | EEDO: Data Output of serial EEPROM. Internally pull up (50K Ohm). Inputs configuration information to ADM6308.  |
| EEDI   | 50  | BI<br>4ma | EEDI: Data Input of serial EEPROM. Internally pull down (50K Ohm). ADM6308 outputs data to EEPROM   |
| EESK   | 48  | BI<br>4ma | EESK: Clock input of serial EEPROM. Internally pull up. ADM6308 outputs clock signal to EEPROM  |
| EECS   | 49  | BI<br>4ma | Chip Select of serial EEPROM. Internally pull down. EECK/s:50ns, h:0ns  |
| <b>Reduced MII Interface</b>   |   |           |   |
| TXE0<br>TXE1<br>TXE2<br>TXE3<br>TXE4<br>TXE5<br>TXE6<br>TXE7   | 72, 86<br>95, 2<br>12, 20<br>28, 35   | O<br>8ma  | Transmit Enable. TXE0~7 shows that ADM6308 is presenting the recovered and decoded data on the TXD0~7[1:0].<br>TXE0~7 indicates that the MAC is presenting di-bits on TXD0~7[1:0] on the Reduced MII for transmission. TXE0~7 shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the Reduced MII. TXE0~7 shall be negative prior to the first REFCLK rising edge following the final di-bit of a frame. TXE0~7 shall transition synchronously with REFCLK.  |
| TXD0[1:0]<br>TXD1[1:0]<br>TXD2[1:0]<br>TXD3[1:0]<br>TXD4[1:0]<br>TXD5[1:0]<br>TXD6[1:0]<br>TXD7[1:0] | 74, 73<br>88, 87,<br>97, 96<br>4, 3<br>14, 13<br>22, 21<br>30, 29<br>37, 36 | O<br>4ma  | Transmit Data. These bundle signals are output from ADM6308 to Reduced MII connecting device. These signals are transited synchronously with the rising edge of TXE0~7. When TXE0~7 is being asserted, for each period of TXE0~7, ADM6308 drives the recovered and encoded data into TXD0~7[1:0] for transmission. While TXE0~7 is de-asserted, the TXD0~7[1:0] will have no effect upon the Reduced MII connecting device.<br>TXD0~7[1:0] shall transition synchronously with REFCLK. When TXE0~7 is being asserted, TXD0~7[1:0] is accepted for transmission by the PHY. TXD0~7[1:0] shall be "00" to indicate idle when TXE0~7 is de-asserted. Values of TXD0~7[1:0] other than "00" when TXE0~7 is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on TXD0~7[1:0] while TXE0~7 is de-asserted shall be ignored by the PHY. |
| TXC0   | 78  | BI<br>4ma | Transmit Clock for port0 MII mode.  |
| TXD0[3:2]  | 77, 76  | O<br>4ma  | Transmit Data for port0 MII mode.   |

|  |   |           |  |
|--|---|-----------|--|
| RXDV0<br>RXDV1<br>RXDV2<br>RXDV3<br>RXDV4<br>RXDV5<br>RXDV6<br>RXDV7                                 | 80, 90<br>98, 5<br>15, 24<br>31, 39   | I         | <p>Carrier Sense and Receive Data Valid. RXDV2, RXDV3, RXDV5, RDDV6, RXDV7 internally pull down. RXDV0~7 shall be asserted by the PHY when the receiver is not idle. The specific definition of idle for 10BASE-T and 100BASE-X is contained in IEEE 802.3 and IEEE 802.3u.</p> <p>RXDV0~7 also shows that the receiving data is presented on the RXD0~7[1:0] from Reduced MII connecting device. RXDV0~7 is being asserted asynchronous on detection of carrier due to criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected, carrier is said to be detected.</p> <p>Loss of carrier shall result in the de-assertion of RXDV0~7 synchronous to the cycles of REFCLK which presents the first di-bit of a nibble onto RXD0~7[1:0]. If the PHY has additional bits to be presented on RXD0~7[1:0] following the initial de-assertion of RXDV0~7, then the PHY shall assert RXDV0~7 on cycles of REFCLK which present the second di-bit of each nibble, and de-assert RXDV0~7 on cycles of REFCLK which present the first di-bit of a nibble. During a false carrier event, RXDV0~7 shall remain asserted for the duration of carrier activity.</p> <p>The data on RXD0~7[1:0] is considered valid once RXDV0~7 is being asserted. However, since the assertion of RXDV0~7 is asynchronous relative to REFCLK, the data on RXD0~7[1:0] shall be "00" until proper receive signal decoding takes place.</p> |
| RXD0[1:0]<br>RXD1[1:0]<br>RXD2[1:0]<br>RXD3[1:0]<br>RXD4[1:0]<br>RXD5[1:0]<br>RXD6[1:0]<br>RXD7[1:0] | 82, 81<br>93, 92<br>100, 99<br>8, 7<br>17, 16<br>26, 25<br>33, 32<br>41, 40 | I         | <p>Receive Data. RXD 2[1:0], RXD 3[1:0], RXD 5[1:0], RXD 6[1:0], RXD 7[1:0] internally pull down. These bundle signals are input from the Reduced MII connecting device. RXD0~7[1:0] shall transition synchronously to REFCLK. For each clock period in which RXDV0~7 is being asserted, RXD0~7[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g. before data recovery or during error conditions) a pre-determined value for RXD0~7[1:0] is transferred instead of the recovered data. RXD0~7[1:0] shall be "00" to indicate idle when RXDV0~7 is de-asserted. Values of RXD0~7[1:0] other than "00" when RXDV0~7 as recovered from RXDV0~7 is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on RXD0~7[1:0] while RXDV0~7 as recovered from RXDV0~7 is de-asserted shall be ignored by the MAC. Upon assertion of RXDV0~7, the PHY shall ensure that RXD0~7[1:0]="00" until proper receive decoding takes place.</p> <p>These pins will be in high impedance, and ignore the input when RXDV0~7 is negative.</p>   |
| RXC0   | 79  | BI<br>4ma | Receive Clock for port0 MII mode.  |
| RXD0[3:2]  | 84, 83  | BI<br>4ma | Receive Data. RXD 0[3:2] internally pull down for port0 MII mode..   |
| CRS0   | 69  | BI<br>4ma | Carrier Sense for port0 MII mode.  |
| COL0   | 70  | BI<br>4ma | Collision for port0 MII mode.  |
| MII#   | 67  | I         | <p>Internally pull up. Active low. This pin can be tied to low for reversing the Reduced MII to MII (port0 only). There is an internal pull high for default configuration.</p> <p>ADM6308 also provides the 1MII+7RMII mode for customer specific requirement. The default address IDs for PHY are the consecutive numbers as follows: 7(for port 0 MII), 8, 9, 10, 11,12,13,14,(for port 1~7 RMII).</p> <p>P.S.: The ID addresses must be the consecutive numbers, otherwise, ADM6308 won't recognize the ID address for PHY.</p>  |

|                            |                       |            |  |
|----------------------------|-----------------------|------------|--|
| MDC                        | 43                    | O<br>8ma   | Management Data Clock. Provides the reference clock for the MDIO signal  |
| MDIO                       | 45                    | BI<br>8ma  | Management Data Input/output. This pin provides the channels for ADM6308 and Transceivers to transfer the control information and status.  |
| <b>LED Display</b>         |                       |            |  |
| QFLED#                     | 46                    | tri<br>8ma | Buffer Full or Faulty LED Display. This occurs when the packet is lost and flow control is disabled. Or, if flow control is enabled and jam or PAUSE frames are sent, buffer full LED will flash. If it is found faulty, the LED will always be on. (See LED function description)   |
| <b>High Priority Frame</b> |                       |            |  |
| high_port[0]               | 53                    | BI         | Priority setting for port0~port7. Internally pull down.<br>High = high priority  |
| high_port[1]               | 54                    |            |  |
| high_port[2]               | 55                    |            |  |
| high_port[3]               | 56                    |            |  |
| high_port[4]               | 58                    |            |  |
| high_port[5]               | 59                    |            |  |
| high_port[6]               | 60                    |            |  |
| high_port[7]               | 61                    |            |  |
| <b>Configuration</b>       |                       |            |  |
| BP0                        | 50                    | I          | Back Pressure Mode. Internally pull down. The BP0~1 modes define 4 different back-pressure methods. Each BPA1~3 has different algorithm described in EEPROM section. The following shows ADM6308 configuration of back-pressure.<br>BP1    BP0<br>0    0    Back Pressure Disable<br>0    1    BPA1 (Back Pressure Algorithm 1) Enable<br>1    0    BPA2 (Back Pressure Algorithm 2) Enable<br>1    1    BPA3 (Back Pressure Algorithm 3) Enable |
| BP1                        | 49                    |            |  |
| NA16#                      | 51                    | I          | Not aborted after continuous 16- times of collision if pull down. Internally pull up.  |
| XFC#                       | 48                    | I          | Full Duplex Flow Control. Internally pull up. When 802.3 x flow control is disable, no PAUSE frame will be sent. (default)   |
| <b>Miscellaneous</b>       |                       |            |  |
| REFCLK                     | 10                    | I          | Clock reference input of 50MHz Reduced MII. Synchronous clock reference for receiving, transmitting, and control interface.  |
| RESET#                     | 63                    | I          | RESET#. Active low. For power on reset to initiate ADM6308 and let all the state machines and statuses enter the initial and default state. Besides, all the LED will be turned on when power is on or RAM testing failed.   |
| RECALL                     | 52                    | I          | Whenever the level is changed, ADM6308 recalls EEPROM or 8051-like controller to get configuration data. Internally pull down.   |
| TEST[0]                    | 65                    | I          | Test mode. Internally pull down  |
| TEST[1]                    | 66                    | I          | Test mode. Internally pull down  |
| <b>Power</b>               |                       |            |  |
| Vddi                       | 6, 23, 38, 57, 68, 89 |            | 2.5V   |
| Vddo                       | 11, 27, 44, 71, 94    |            | 3.3V   |

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|     |  |  |
|-----|--|--|
| Vss | 9, 19, 42, 64, 75, 91<br>1, 18, 34, 47, 62, 85 |  |
|-----|--|--|

**EEPROM Content**

The EEPROM setting must be in 16-bit mode.

| Offset | Content                    | Description  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
|--------|----------------------------|--|-------|---------------------------------|-------|----------|----|--------------|---|---|---|---------------------------------|---|---|---|---|-----------------------|---|---|---|---|------------------------|---|---|---|---|------------------------|---|---|---|---|------------------------|---|---|---|---|------------------------|---|---|---|---|-------------------------|-------|-------|--|---|---|-------------------|---|---|------------|---|---|------------|---|---|------------|--------|--------|--|---|---|--|---|---|------------------------------|---|---|------------------------------|---|---|----------|
| 00H    | Check Pattern              | Must be set to 017C  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 01H    | System Configuration       | <p>Bit 3~0 – Inter Frame Gap in half-duplex mode only. Default is zero (96 bit-time). Bit 3 is a sign bit. When bit 3 is zero, it means negative. Bit 0 ~ 2 present decimal value of bit time (times four). For example, 1010, the IFG is equal to <math>96 + 2 \times 4 = 104</math>.</p> <p>Bit 7~4 – Configurable aging time. Default is 300 sec. When bit 7 is one, fast aging time (15 sec) is set. If all zero, aging timer is disabled. For the other value, list below.</p> <table style="margin-left: 40px;"> <tr> <td>bit 7</td> <td>bit 6</td> <td>bit 5</td> <td>bit 4</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Aging time is 300 sec (Default)</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Aging time is 600 sec</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Aging time is 1200 sec</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Aging time is 2400 sec</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Aging time is 4800 sec</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Aging time is 9600 sec</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Aging time is 38400 sec</td> </tr> </table> <p>Bit 9~ 8 – Broadcast storming mode. This mode is only for broadcast destination address, FF FF FF FF FF FF.</p> <table style="margin-left: 40px;"> <tr> <td>bit 9</td> <td>bit 8</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Disable (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>256 blocks</td> </tr> <tr> <td>1</td> <td>0</td> <td>192 blocks</td> </tr> <tr> <td>1</td> <td>1</td> <td>128 blocks</td> </tr> </table> <p>Bit 11 ~ 10 – Maximum Length of the data field of frame format.</p> <table style="margin-left: 40px;"> <tr> <td>Bit 11</td> <td>bit 10</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Maximum length is 1536 bytes (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Maximum length is 1518 bytes</td> </tr> <tr> <td>1</td> <td>0</td> <td>Maximum length is 1522 bytes</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </table> <p>Bit 12 – Continuous 16-time collision abort per packet is enabled if set to zero. Default is zero. EEPROM setting has higher priority than pin's.</p> <p>Bit 13 – Hashing algorithm selection. If zero, direct mapping algorithm is selected. Otherwise, CRC hashing algorithm is adopted. Default is zero.</p> <p>Bit 14 – Over written address. Default is zero, which means over written address is not allowed whenever the same addresses entry condition occurred after hashing algorithm implementation finished.</p> <p>Bit 15 - Must be set to zero.</p> | bit 7 | bit 6                           | bit 5 | bit 4    |    | 0            | 0 | 0 | 1 | Aging time is 300 sec (Default) | 0 | 0 | 1 | 0 | Aging time is 600 sec | 0 | 0 | 1 | 1 | Aging time is 1200 sec | 0 | 1 | 0 | 0 | Aging time is 2400 sec | 0 | 1 | 0 | 1 | Aging time is 4800 sec | 0 | 1 | 1 | 0 | Aging time is 9600 sec | 0 | 1 | 1 | 1 | Aging time is 38400 sec | bit 9 | bit 8 |  | 0 | 0 | Disable (Default) | 0 | 1 | 256 blocks | 1 | 0 | 192 blocks | 1 | 1 | 128 blocks | Bit 11 | bit 10 |  | 0 | 0 | Maximum length is 1536 bytes (Default) | 0 | 1 | Maximum length is 1518 bytes | 1 | 0 | Maximum length is 1522 bytes | 1 | 1 | Reserved |
| bit 7  | bit 6                      | bit 5  | bit 4 |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 0                          | 0  | 1     | Aging time is 300 sec (Default) |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 0                          | 1  | 0     | Aging time is 600 sec           |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 0                          | 1  | 1     | Aging time is 1200 sec          |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | 0  | 0     | Aging time is 2400 sec          |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | 0  | 1     | Aging time is 4800 sec          |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | 1  | 0     | Aging time is 9600 sec          |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | 1  | 1     | Aging time is 38400 sec         |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| bit 9  | bit 8                      |  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 0                          | Disable (Default)  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | 256 blocks   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 1      | 0                          | 192 blocks   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 1      | 1                          | 128 blocks   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| Bit 11 | bit 10                     |  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 0                          | Maximum length is 1536 bytes (Default)   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 0      | 1                          | Maximum length is 1518 bytes   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 1      | 0                          | Maximum length is 1522 bytes   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 1      | 1                          | Reserved   |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 02H    | Back Pressure and Back-off | <p>Bit 2 ~ 0 - Must be "0 0 1".</p> <p>Bit 6 ~ 4 - Must be "1 0 1".</p> <p>Bit 11 ~ 8 –Jam number for BP algorithm 1</p> <p>Bit 13 ~ 12 – BP mode</p> <table style="margin-left: 40px;"> <tr> <td>00</td> <td>: disable BP</td> </tr> <tr> <td>01</td> <td>: BP jam</td> </tr> <tr> <td>10</td> <td>: BP iam ALL</td> </tr> </table>   | 00    | : disable BP                    | 01    | : BP jam | 10 | : BP iam ALL |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 00     | : disable BP               |  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 01     | : BP jam                   |  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |
| 10     | : BP iam ALL               |  |       |                                 |       |          |    |              |   |   |   |                                 |   |   |   |   |                       |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                        |   |   |   |   |                         |       |       |  |   |   |                   |   |   |            |   |   |            |   |   |            |        |        |  |   |   |  |   |   |                              |   |   |                              |   |   |          |



|       |   |  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
|-------|---|--|-------|------------------------------|------|------|--|---|---|---|---|-----------------------------|---|---|---|---|--------------------|---|---|---|---|--------------------|---|---|---|---|------------------------------|
|       |   | 11 : BP carrier<br>Bit 14 – 1 (Default)<br>Bit 15 – 0 (Default)  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 03H   | Auto-negotiation monitor                                      | Bit 7 ~ 0 – N-WAY monitor disable port [7:0]. 0 : Enable (Default)<br>Bit 15 ~ 8 – Port disable port [7:0]. 0 : Enable (Default)   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 04H   | Speed and Half/Full Duplex setting when N-Way monitor disable | Bit 7 ~ 0 – Full/half operation. Each bit presents dedicated port number. Lower bit is intended for smaller port number. 1 stands for full duplex, 0 for half duplex.<br>Bit 15 ~ 8 – Speed setting for port [7:0]. Speed operation, 10Mbps or 100Mbps. One bit per port. 1 stands for 100Mbps, 0 for 10Mbps.  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 05H   | 4 Port-Groups Operation (1)                                   | Bit 7 ~ 0 – Port group II [7:0], Default is 00h.<br>Bit 15 ~ 8 – Port group I [7:0], Default is FFh.   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 06H   | 4 Port-Groups Operation (2)                                   | Bit 7 ~ 0 – Port group IV [7:0], Default is 00h.<br>Bit 15 ~ 8 – Port group III [7:0], Default is 00h.   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 07H   | 802.3x flow control and Back pressure enable                  | Bit 7 ~ 0 – Per port BP enabled port [7:0], 1 stands for Enable (Default). If enabled, it must be in half duplex mode.<br>Bit 15 ~ 8 – Per port 802.3x flow control enabled port [7:0]. 0 stands for Disable (by pin)  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 08H   | 802.3x flow control   | Bit 7 ~ 0 – Force 802.3x flow control on (ignore AN) port [7:0]. If enabled, it must be in full duplex. 0 stands for disable (Default).<br>Bit 15 ~ 8 – Write FC-bit (10 <sup>th</sup> bit) of MII register4 port [7:0], 1 stands for Enable (Default).  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 09H   | Reserved  | Must be set to 112H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0AH   | Reserved  | Must be set to 132H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0BH   | Reserved  | Must be set to B2H   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0CH   | Reserved  | Must be set to D2H   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0DH   | Reserved  | Must be set to 150H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0EH   | Reserved  | Must be set to 170H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0FH   | Reserved  | Must be set to 150H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 10H   | Reserved  | Must be set to 170H  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 11H   | Reserved  | Must be set to e8H   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 12H   | Reserved  | Must be set to c8H   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 13H   | Reserved  | Bit 7~0 - Must be set to 18H<br>Bit 15~8 – Must be set to 0cH  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 14H   | Priority Frame operation                                      | Bit 7 ~ 0 – Auto turn off BP/FC, if get priority packet port [7:0]. 0 stands for disable (Default)<br>Bit 11 ~ 8 – Round-robin(sequential) number of high and low priority frame<br>For example as follows:<br><table style="margin-left: 40px;"> <tr> <td>bit11</td> <td>bit10</td> <td>bit9</td> <td>bit8</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Weighted ratio is unlimited</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Weighted ratio 1:1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Weighted ratio 2:1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Weighted ratio 8:1 (Default)</td> </tr> </table><br>Bit 13 – Must be set to 0.<br>Bit 14 – Must be set to 0.<br>Bit 15 – Priority is enabled, 1 stands for enable (Default). | bit11 | bit10                        | bit9 | bit8 |  | 0 | 0 | 0 | 0 | Weighted ratio is unlimited | 0 | 0 | 0 | 1 | Weighted ratio 1:1 | 0 | 0 | 1 | 0 | Weighted ratio 2:1 | 1 | 0 | 0 | 0 | Weighted ratio 8:1 (Default) |
| bit11 | bit10   | bit9   | bit8  |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0     | 0   | 0  | 0     | Weighted ratio is unlimited  |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0     | 0   | 0  | 1     | Weighted ratio 1:1           |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 0     | 0   | 1  | 0     | Weighted ratio 2:1           |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 1     | 0   | 0  | 0     | Weighted ratio 8:1 (Default) |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 15H   | TOS priority port   | Bit 15 ~ 8 – Set TOS priority port [7:0], 0 stands for no check (Default).<br>One bit per port. e.g. bit 8 for port 0 and bit 15 for port 7.   |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |
| 16H   | VLAN  | Bit 7 ~ 0 - Set VLAN priority port [7:0], 0 stands for no check (Default).<br>One bit per port. e.g. bit 0 for port 0 and bit 7 for port 7.  |       |                              |      |      |  |   |   |   |   |                             |   |   |   |   |                    |   |   |   |   |                    |   |   |   |   |                              |

|     |                   |  |
|-----|-------------------|--|
|     |                   | Bit 15 ~ 8 – First, ADM6308 will check the specific bits recorded in the type field of packet format to verify the VLAN status of packets, then set the threshold of VLAN. The default of threshold is 4. If threshold is greater than the packet is high priority.  |
| 17H | TOS bit map       | Bit 15 ~ 0 - TOS bit map [63:48](tos_pri)(tos_pri_drop), Default is 0. First, ADM6308 will check the specific bits recorded in the type field of TCP/IP packet format, to verify the TOS status of packets, then Implement the bits mapping for priority setting of each port.   |
| 18H | TOS bit map       | Bit 15 ~ 0 - TOS bit map [47:32](tos_pri)(tos_pri_drop), Default is 0. First, ADM6308 will check the specific bits recorded in the type field of TCP/IP packet format, to verify the TOS status of packets, then Implement the bits mapping for priority setting of each port.   |
| 19H | TOS bit map       | Bit 15 ~ 0 - TOS bit map [31:16](tos_pri)(tos_pri_drop), Default is 0. First, ADM6308 will check the specific bits recorded in the type field of TCP/IP packet format, to verify the TOS status of packets, then Implement the bits mapping for priority setting of each port.   |
| 1AH | TOS bit map       | Bit 15 ~ 0 - TOS bit map [15: 0](tos_pri)(tos_pri_drop), Default is 0. First, ADM6308 will check the specific bits recorded in the type field of TCP/IP packet format, to verify the TOS status of packets, then Implement the bits mapping for priority setting of each port.   |
| 1BH | PHY operation (1) | Bit 4 ~ 0 – PHY rewrite register address. These bits present PHY register address selection.<br>Bit 7 – PHY rewrite. Default is zero (Disable ).<br>Bit 12 ~ 8 – PHY start ID. Default is 00H. This means PHY IDs range from 00 H to 07H in sequence if default value is set. Remember start ID always has to remain consistent with the first port ID setting in PHY.<br>Bit 15 ~ 13 – N/A. |
| 1CH | PHY operation (2) | Bit 15 ~ 0 – PHY rewrite data. After PHY rewrite register address is selected, the register in each port is set to rewrite data.   |
| 1DH | Reserved          | Must be set to 10dH  |

## Function Description

ADM6308 is a high performance, low cost, quality assurance 8-port Fast Ethernet Controller dedicated to 8-port switch solutions. This chip operates at 50MHz and fully complies with IEEE 802 series specifications, including MAC and Physical layers.

The switch operations include forwarding scheme, packet filtering, address learning, buffer management, LED display, etc. Packets from Reduced MII interface should be stored in the memory. Then, source address learning, packet filtering, and retransmission to known or unknown port(s) is implemented based on real application.

## Reset and Restart

When ADM6308 is on, it starts in embedded memory self-test mode.

## Port Interface

### 10/100Mbps Reduced MII Interface

Each port of ADM6308 supports Reduced MII interfaces, which uses six pins, TXE0~7, TXD0~7[1:0], RXDV0~7, RXD0~7[1:0]. Feature setting can be chosen by configuration pin. The RMI specification has the following characteristics:

1. It supports 10Mbps and 100Mbps data rates
2. A single clock reference sources from the MAC to PHY (or from an external source)
3. It provides independent 2-bit wide (di-bit) transmit and receive data paths

### RMI Specification Signals

| Signal Name | Direction with respect to PHY | Direction with respect to the MAC | Usage   |
|-------------|-------------------------------|-----------------------------------|---|
| REFCLK      | Input                         | Input or Output                   | Synchronous clock reference for receive, transmit and control interface |
| RXDV        | Output                        | Input                             | Carrier Sense   |
| RXD[1:0]    | Output                        | Input                             | Receive Data  |
| TXE         | Input                         | Output                            | Transmit Enable   |
| TXD[1:0]    | Input                         | Output                            | Transmit Data   |

All detail pin description (please see pin assignment).

In addition, ADM6308 also provides the MII mode at port 0 only. The relevant settings are described in the previous pages of pin description.

## Buffer Management

The buffer memory is embedded in ADM6308 for eight port switch operations, which are designed based on output queuing and dynamic shared memory management architecture.

## Media Access Control

ADM6308 implements all functions of IEEE 802.3 MAC protocol such as frame formatting, collision handling, etc. ADM6308 generates 56-bit preamble and Start of Frame delimiter while a packet is being sent. In half-duplex mode, listening before transmitting allows to prevent traffic jam. Whenever a collision occurs, packet will be delayed for a random time, then be re-sent.

## EEPROM or Dynamic configured by 8051

EEPROM is a configuration option for 8-port switch setting. This setting can also be called through Recall pin triggered by the controller like 8051.

1. EEPROM recall after power-on is reset.

2. The configuration can be changed without a reset. Toggling the “recall” pin will read the EEPROM again, while 8051 will emulate the signal like EEPROM

## Operation Modes

Reduced MII interface to PHYs or transceivers can operate at 10/100Mbps full or half-duplex mode. To keep a consistent operation speed, these two parts (PHY and switching controller) will be automatically adjusted the mode through MDC/MDIO pins. ADM6308 also provides fixed speed and operation mode configured by EEPROM, and dynamic configuration by the controller like 8051. All modes support full wire speed operations without any interference.

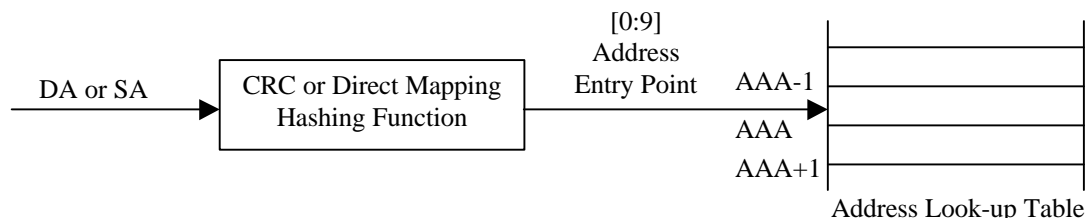
## Automatic Address Learning, Forwarding, and Filtering Function

### Address Recognition

ADM6308 provides 1Kbytes embedded MAC address table to implement the address recognition. Self-learning bridge function is based on source address packets field. Look-up table and two different hashing algorithms strengthen the bridge ability with high performance assurance. Configurable aging time is also supported. An entry of hashing table is calculated by 32-bit polynomial (called CRC hashing function) or direct mapping (called simple hashing function), as well as MAC address (called input data). Direct mapping function is allocated the lowest 10 bits of SA/DA address as buffer address entry. Hashing function selection is set to bit 13 of offset 01H in EEPROM. Each DA (Destination Address) passes through hashing function and gets a 10-bit entry point of embedded SRAM. If the record is empty, the packet is broadcast, treated as an unknown frame. Otherwise, the record is read, then MAC address in storage and DA from current packet are compared. If the two addresses are the same, a port number is decided, and the packet is forwarded to the assigned port. If the two addresses are different, the incoming packet is also treated as an unknown packet. A broadcast packet will pass through the other ports without address recognition.

### Learning Process

Address learning process is composed of SA packets and a hashing function described above. For each incoming packet, ADM6308 will check and see whether the packet is errorless and whether the content of the entry address in SRAM is assigned. If it is, the packet will be compared to source MAC address, and the port number. If both fields match the packet information, aging status is revised to new learnt address. If MAC addresses matches, but the port number is different, port number is re-assigned. When the entry collides, the new SA address is ignored and the record keeps the old one. Last possibility, if the record is free, MAC address and port number of the incoming packet are stored. The following diagram describes the general operations of address learning and recognition.



**Fig. 1 Address Learning and Recognition**

### Forwarding Scheme

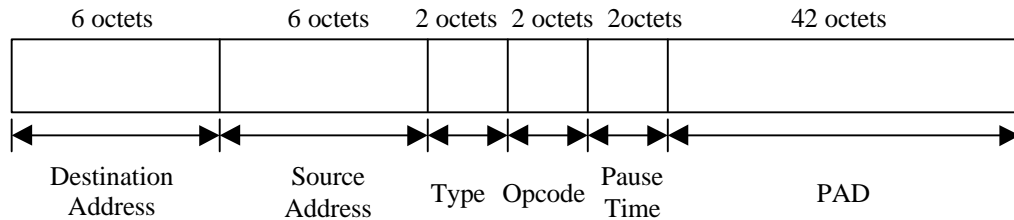
ADM6308 forwarding scheme adopts store-and-forward method. Each determined outgoing packet in the buffer of incoming port is directly sent to the assigned port. The forwarding scheme of unknown packets is treated the same as broadcast packet. ADM6308 also requires first-in-first-out service, to prevent packets disorder.

## IEEE 802.3 Congestion Control

In half duplex operation, ADM6308 supports back pressure feature. When the buffer is full, jam packet or 802.3x control frame is sent to the connected segment, which is called back - pressure.

ADM6308 implements Alternative back - pressure based on either one of three algorithms described in EEPROM section. If free blocks in the buffer memory match or are below the threshold, jam packet is directly transmitted regardless of routing decision.

In Full duplex flow control, ADM6308 follows IEEE 802.3x standard. The delay time in PAUSE frame can be set to zero or to the maximum value. The feature allows ADM6308 to handle remote-side PAUSE frame. In full duplex flow control, the state machine and threshold values are described in EEPROM, too.



**Fig 2 IEEE 802.3x PAUSE Frame Format**

The diagram shown above is IEEE 802.3x Pause frame format. All fields are listed below.

Destination Address: destination MAC address (Generally the content is 0x0180C2000001)

Source Address: source MAC address

Type: the PAUSE frame type is 0x8808

Opcode : the value is fixed, 0x0001 (PAUSE operation)

Pause Time: Number of slot-time

PAD: All zeroes

In ADM6308, if a PAUSE frame is received from a certain port with DA 0x0180C2000001 or 0xFFFFFFFFFFFF, ADM6308 will stop the ports transmission of packets and the timer until timeout or another PAUSE frame with zero time. If the buffer is full and in full duplex mode, ADM6308 will send PAUSE frame with the maximum delay time, to defer receiving packet. When enough buffer is released, PAUSE frame with zero delay is sent.

### Auto-negotiation Operations

When MDC/MDIO pins do not communicate with transceivers, ADM6308 can be set to 10/100Mbps or half/full duplex mode independently. Otherwise, ADM6308 can adjust its speed itself according to auto-negotiation with PHYceiver.

### Priority Frame (CoS) Operations

ADM6308 can set the packets as high priority as follows: Port Number (set by pin), VLAN tag, TCP/IP TOS/DS (both can be set by EEPROM or 8051-like controller) and the scheme of weighted round robin. The priority setting by port means that all the packets received by the port will be priority frames; ADM6308 can also judge the priority of frames by checking the specific bits of VLAN tag or TCP/IP TOS/DS included in the frame format. ADM6308 will check the specific bits recorded in the type field of packet format to ensure the VLAN or TCP/IP TOS/DS status of packets, then set the threshold of VLAN or TCP/IP TOS/DS to declare the priority of packets. In addition, the scheme of weighted round robin is used for judging the high and low priority of frames, which utilizes the notion of weighted ratio of priority frame vs. normal frame to decide the frame priority level. When the port receives the priority frame, back pressure & 802.3x flow control will be turned off until no priority frame occurs within 1 or 2 seconds, then turn on back pressure and 802.3x flow control again.

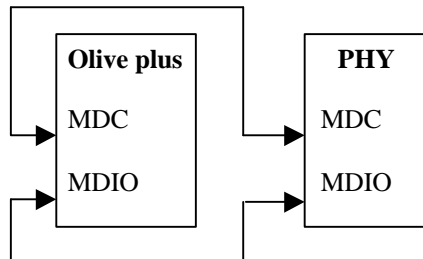
### VLAN and Broadcast Storming Prevention

ADM6308 supports VLAN function to ease the administration of logical groups of stations that can communicate as if they were on the same LAN, and move, add or change in numbers of these groups. ADM6308 also supports 4 port-groups scheme to effectively prevent the broadcast storming from interfering with the whole transmission efficiency between ports. The 8 ports can be divided into 4 groups while broadcast storming is starting, then the broadcast frames to be transmitted to the destination port belonging to other groups will be prohibited. During this time, the ports belonging to different groups are independent. Only the destination port of broadcast frames in the same group will be allowed. Furthermore, the scheme of port-group dividing is very flexible. The overlapped port-groups are allowed during some operations, for example, one port can be shared by two groups, and all the other operations between these two groups remain independent except for the overlapped port. Only the overlapped port could use the same DA for two different VLAN port-groups.

## Inter-Frame Gap

IFG is the idle time between any two continuous packets from the same port. The default value of 10Mbps is 9.6usec and 0.96usec for 100Mbps. IFG mode can only be from CRS to TXE.

## MDC, MDIO Interface



**Fig. 3 A specific application of Serial Management Interface**

There are two pins of Serial Management Interface for ADM6308. MDC (Management Data Clock) is an input pin. It functions MII interface of PHY device. The MDIO pin is a bi-directional I/O pin of MII interface to PHY device. If the following conditions are true, ADM6308 will set bit 1 of register 4 to 1 and bit 9 of register 0 to 1 in connected transceiver. First, IEEE 802.3x flow control is enabled. Then, the port number of Flow Control Write in EEPROM offset 05H is enabled. Then, ADM6308 is in full duplex simultaneously with the Transceiver. After write operation through MDIO, auto-negotiation is restarted and ADM6308 can gain the information of remote 802.3x flow control. Finally, the ultimate operation of flow control is set.

## LED Interface

ADM6308 supports one LED only assigned to Pin 46, which represents the buffer as full and RAM test fault. When ADM6308 is reset, LED is off. While in testing mode, LED is on. If the test for embedded data buffer & address table fails, the LED will flash once, for about 1.6 sec, and then stay on. Next, if the testing for the other embedded memory fails, LED will flash twice, for about 1.6sec. After RAM tests are successful, LED status is down, for about 3.2sec. minimum. If back -pressure or full duplex flow control is set, the buffer full LED will flash every 200ms, then stay on for 3.2sec based on jam packet or if PAUSE frame is sent. If an arrival packet is dropped, the LED will flash every 50ms, then stay on for 3.2sec.

**Absolute Maximum Ratings**

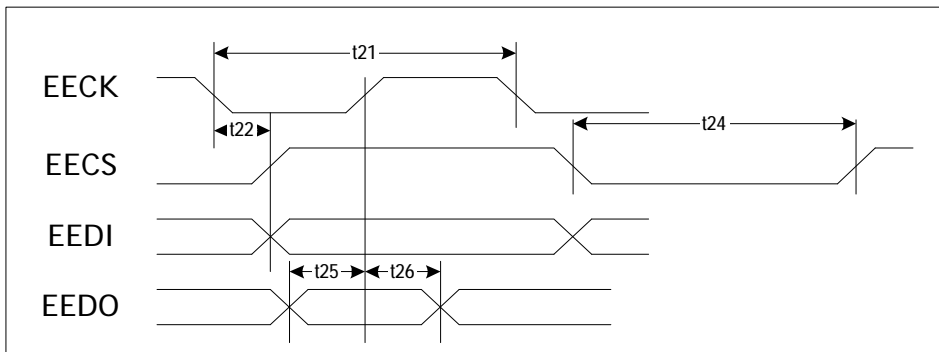
|                     |                                  |
|---------------------|----------------------------------|
| Supply Voltage(Vcc) | -0.5 V to 2.7 V                  |
| Input Voltage       | -0.5 V to VCC + 0.3 V            |
| Output Voltage      | -0.5 V to VCC + 0.3 V            |
| Storage Temperature | -65 °C to 150 °C(-85°F to 302°F) |
| Ambient Temperature | 0°C to 70°C(32°F to 158°F)       |
| ESD Protection      | 2000V                            |

**DC Specifications**

| Parameter | Description                | Condition     | Min  | Typical | Max | Units |
|-----------|----------------------------|---------------|------|---------|-----|-------|
| Vcc       | Supply Voltage             |               | 2.3  | 2.5     | 2.7 | V     |
| Icc       | Power Supply               | Vcc = 2.5V    |      |         | 420 | mA    |
| Vil       | Input LOW Voltage          |               | -0.5 |         | 0.8 | V     |
| Vih       | Input HIGH Voltage         |               | 2.0  |         | 3.8 | V     |
| Iil       | Input LOW Leakage Current  | Vin = 0.8V    | -10  |         | 10  | uA    |
| Iih       | Input HIGH Leakage Current | Vin = 2.0V    | -10  |         | 10  | uA    |
| Vol       | Output LOW Voltage         | Iout =2~8mA   | .    |         | 0.4 | V     |
| Voh       | Output HIGH Voltage        | Iout =-2~-8mA | 2.4  |         |     | V     |
| Cinp      | Input Pin Capacitance      |               | 5    |         | 8   | pF    |
| Lpinp     | Pin Inductance             |               | N/A  |         |     | nH    |

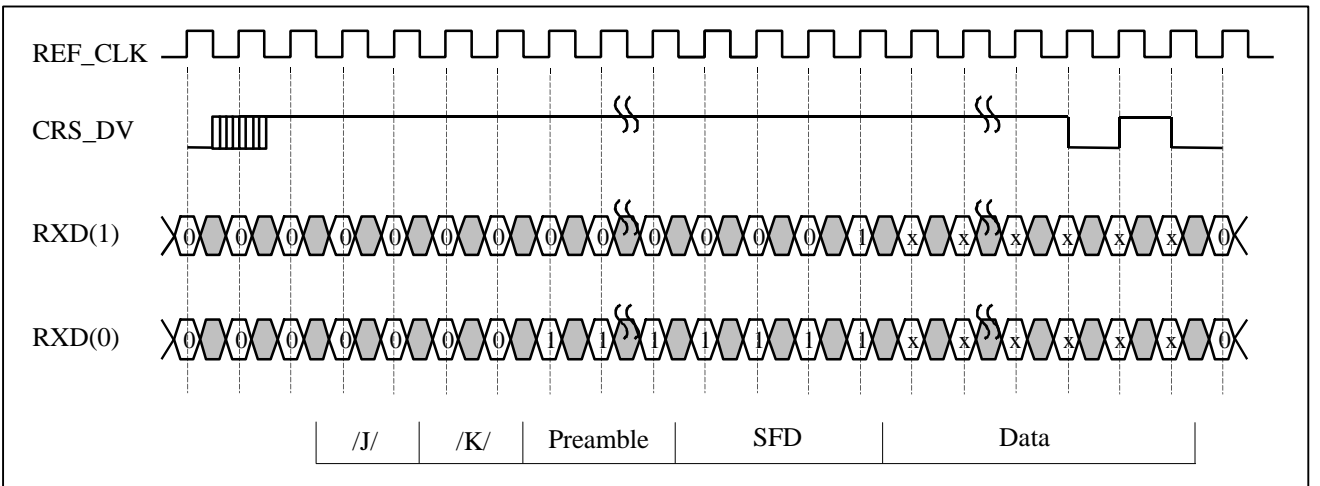
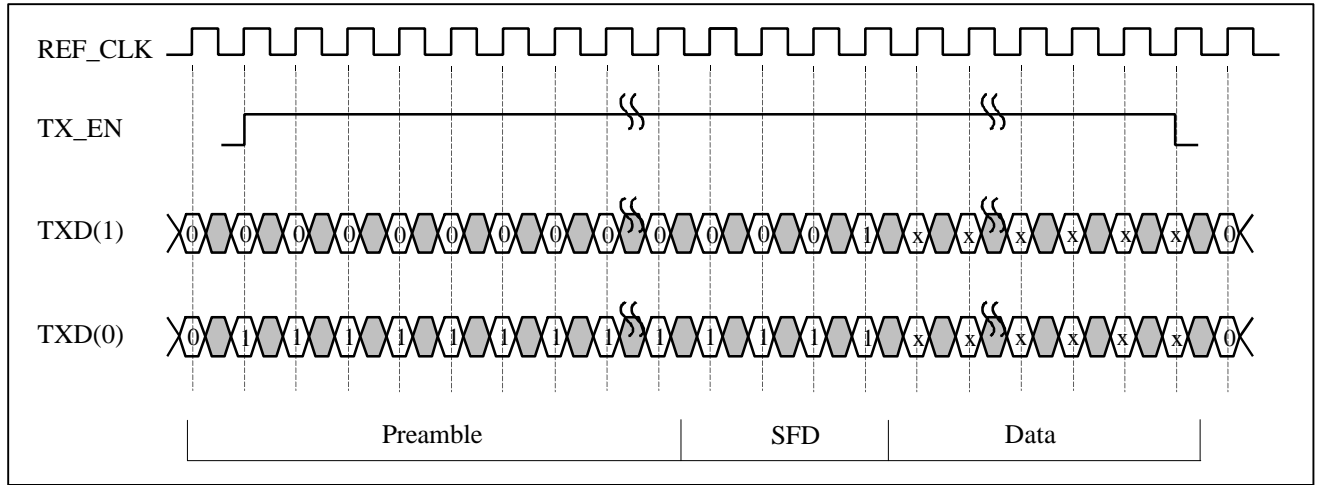
**AC Specifications**

*EEPROM Timing*



| Parameter | Description                          | Condition     | Min  | Max | Units |
|-----------|--------------------------------------|---------------|------|-----|-------|
| t21       | EECK (50% duty cycle)                | Clock = 50MHz | 620  |     | ns    |
| t22       | EECS/EEDI delay from falling of EECK | Clock = 50MHz | 100  |     | ns    |
| t24       | idle time of two EECS                | Clock = 50MHz | 4000 |     | ns    |
| t25       | EEDO valid before rising of EECK     |               | 100  |     | ns    |
| t26       | EEDO hold after rising of EECK       |               | 30   |     | ns    |

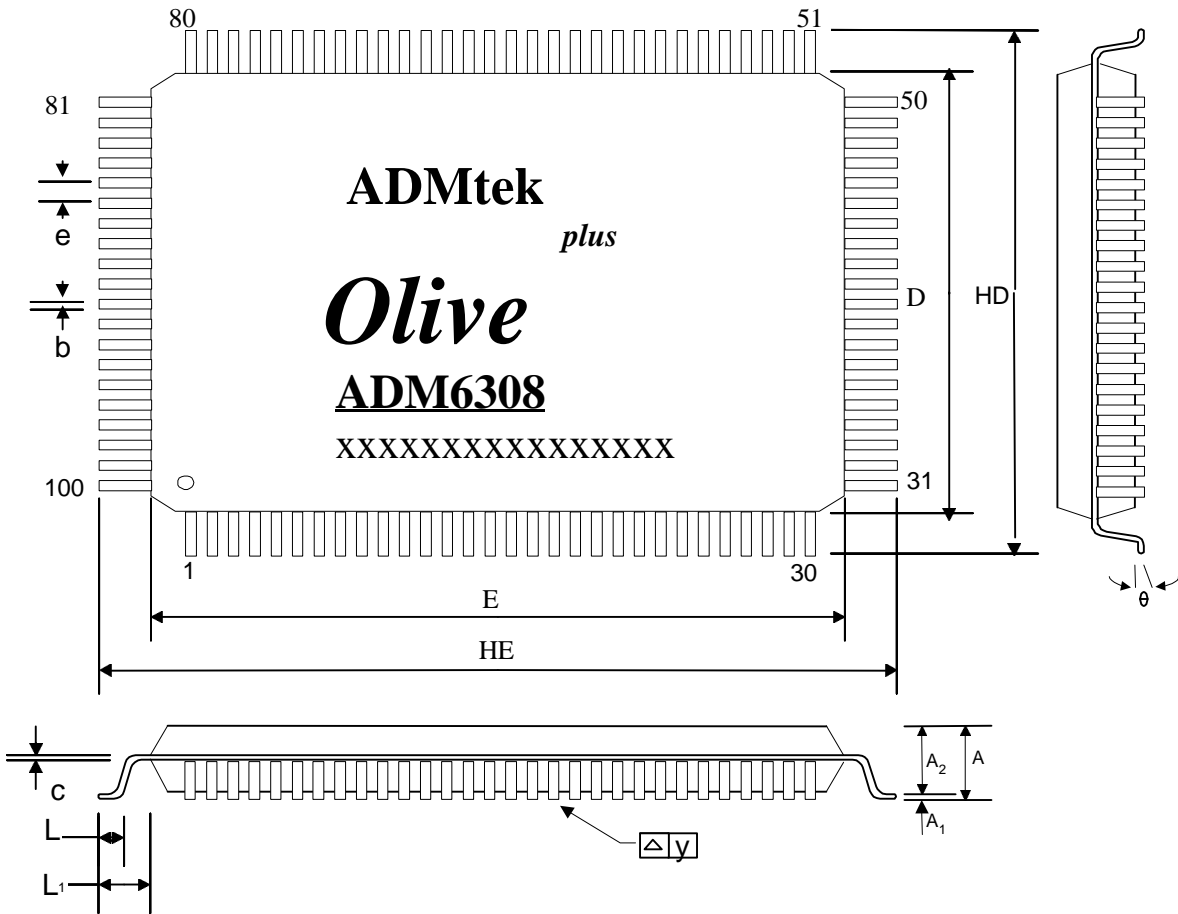
RMII Transmit and Receive Timing



| Symbol | Parameter   | Min | Type | Max | Units |
|--------|---|-----|------|-----|-------|
|        | REF_CLK Frequency   |     | 50   |     | MHz   |
|        | REF_CLK Duty Cycle  | 35  |      | 65  | %     |
| Tsu    | TXD[1:0], TX_EN, RXD[1:0], CRS_DV, Data setup to REF_CLK rising edge  | 4   |      |     | ns    |
| Thold  | TXD[1:0], TX_EN, RXD[1:0], CRS_DV, Data hold from REF_CLK rising edge | 2   |      |     | ns    |



**ADM6308 Package**



| SYMBOL                     | inch      |       |       | mm       |       |       |
|----------------------------|-----------|-------|-------|----------|-------|-------|
|                            | MIN       | NOM   | MAX   | MIN      | NOM   | MAX   |
| <b>A</b>                   | -         | -     | 0.134 | -        | -     | 3.40  |
| <b>A1</b>                  | 0.010     | -     | -     | 0.25     | -     | -     |
| <b>A2</b>                  | 0.098     | 0.107 | 0.114 | 2.50     | 2.72  | 2.90  |
| <b>b</b>                   | 0.009     | 0.012 | 0.015 | 0.22     | 0.30  | 0.38  |
| <b>C</b>                   | 0.004     | -     | 0.008 | 0.09     | -     | 0.20  |
| <b>D</b>                   | 0.547     | 0.551 | 0.555 | 13.9     | 14    | 14.1  |
| <b>E</b>                   | 0.783     | 0.787 | 0.791 | 19.9     | 20.00 | 20.1  |
| <b>e</b>                   | 0.026 BSC |       |       | 0.65 BSC |       |       |
| <b>L</b>                   | 0.018     | 0.024 | 0.030 | 0.45     | 0.60  | 0.75  |
| <b>L1</b>                  | 0.063 REF |       |       | 1.60 REF |       |       |
| <b>y</b>                   | -         | -     | 0.003 | -        | -     | 0.076 |
| <b><math>\theta</math></b> | 0°        | 3.5°  | 7°    | 0°       | 3.5°  | 7°    |

\* HD=17.2mm  
\* HE=23.2mm