ANALOG DEVICES

Dual Bootstrapped, 12 V MOSFET Driver with Output Disable

ADP3120A

FEATURES

All-in-one synchronous buck driver
Bootstrapped high-side drive
One PWM signal generates both drives
Anticross conduction protection circuitry
$\overline{\text{OD}}$ for disabling the driver outputs
  Meets CPU VR requirement when used with Analog Devices Flex -Mode™[1] controller

APPLICATIONS

Multiphase desktop CPU supplies
Single-supply synchronous buck converters

GENERAL DESCRIPTION

The ADP3120A is a dual, high voltage MOSFET driver optimized for driving two N-channel MOSFETs, the two switches in a nonisolated synchronous buck power converter. Each driver is capable of driving a 3000 pF load with a 45 ns propagation delay and a 25 ns transition time. One of the drivers can be bootstrapped and is designed to handle the high voltage slew rate associated with floating high-side gate drivers. The ADP3120A includes overlapping drive protection to prevent shoot-through current in the external MOSFETs.

The $\overline{\text{OD}}$ pin shuts off both the high-side and the low-side MOSFETs to prevent rapid output capacitor discharge during system shutdown.

The ADP3120A is specified over the commercial temperature range of 0°C to 85°C and is available in 8-lead SOIC_N and 8-lead LFCSP_VD packages.

[1] Flex-Mode is protected by U.S. Patent 6683441; other patents pending.

FUNCTIONAL BLOCK DIAGRAM

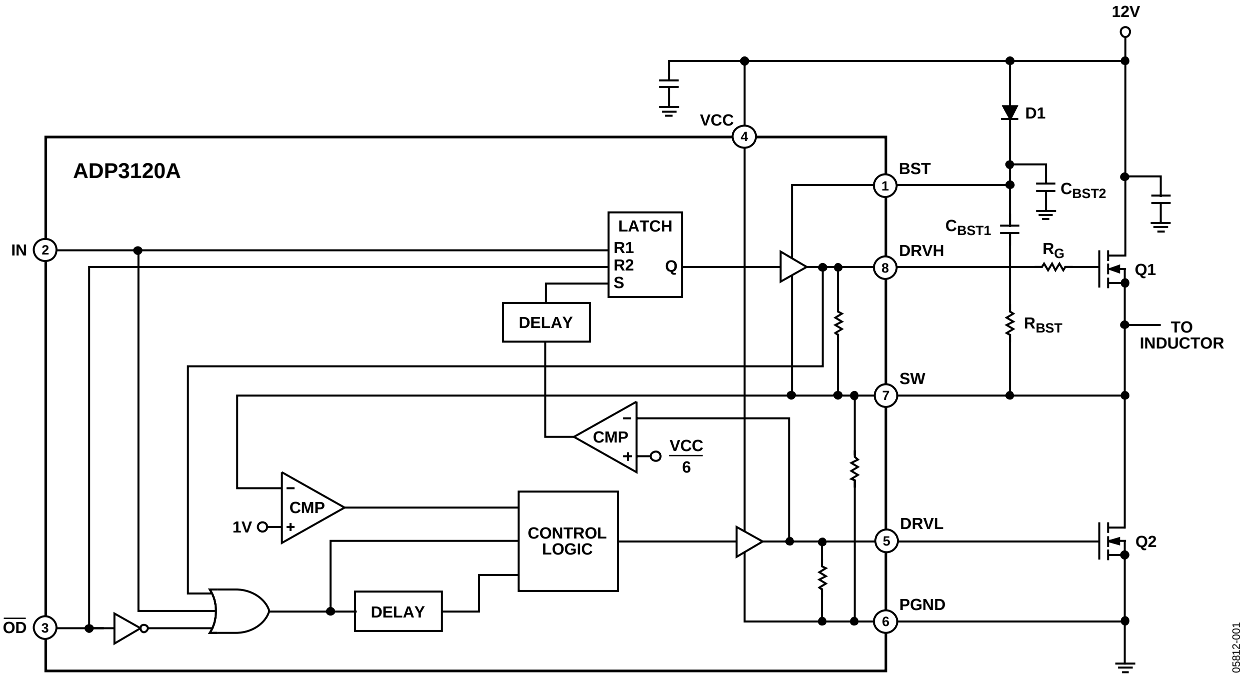


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

3/06—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 12 V, BST = 4 V to 26 V, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS (PWM, $\overline{OD}$)						
Input Voltage High			2.0			V
Input Voltage Low					0.8	V
Input Current			−1		+1	µA
Hysteresis			90	250		mV
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		BST − SW = 12 V ; T_A = 25°C			3.3	Ω
		BST − SW = 12 V ; T_A = 0°C to 85°C		2.5	3.9	Ω
Output Resistance, Sinking Current		BST − SW = 12 V; T_A = 25°C			1.8	Ω
		BST − SW = 12 V; T_A = 0°C to 85°C		1.4	2.6	Ω
Output Resistance, Unbiased		BST − SW = 0 V		10		kΩ
Transition Times	t_{rDRVH}	BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 5		25	40	ns
	t_{fDRVH}	BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 5		20	30	ns
Propagation Delay Times	$t_{pdhDRVH}$	BST − SW = 12 V, C_{LOAD} = 3 nF, 25°C ≤ T_A ≤ 85°C, see Figure 5	32	45	70	ns
	$t_{pdlDRVH}$	BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 5		25	35	ns
	$t_{pdl\overline{OD}}$	See Figure 4		20	35	ns
	$t_{pdh\overline{OD}}$	See Figure 4		40	55	ns
SW Pull-Down Resistance		SW to PGND		10		kΩ
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current		T_A = 25°C			3.3	Ω
		T_A = 0°C to 85°C		2.4	3.9	Ω
Output Resistance, Sinking Current		T_A = 25°C			1.8	Ω
		T_A = 0°C to 85°C		1.4	2.6	Ω
Output Resistance, Unbiased		V_{CC} = PGND		10		kΩ
Transition Times	t_{rDRVL}	C_{LOAD} = 3 nF, see Figure 5		20	35	ns
	t_{fDRVL}	C_{LOAD} = 3 nF, see Figure 5		16	30	ns
Propagation Delay Times	$t_{pdhDRVL}$	C_{LOAD} = 3 nF, see Figure 5		12	35	ns
	$t_{pdlDRVL}$	C_{LOAD} = 3 nF, see Figure 5		30	45	ns
	$t_{pdl\overline{OD}}$	See Figure 4		20	35	ns
	$t_{pdh\overline{OD}}$	See Figure 4	110	190		ns
Timeout Delay		SW = 5 V	110	190		ns
		SW = PGND	95	150		ns
SUPPLY						
Supply Voltage Range	V_{CC}		4.15		13.2	V
Supply Current	I_{SYS}	BST = 12 V, IN = 0 V		2	5	mA
UVLO Voltage		V_{CC} rising	1.5		3.0	V
Hysteresis				350		mV

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
BST	
DC	−0.3 V to V_{CC} + 15 V
<200 ns	−0.3 V to +35 V
BST to SW	−0.3 V to +15 V
SW	
DC	−5 V to +15 V
<200 ns	−10 V to +25 V
DRVH	
DC	SW − 0.3 V to BST + 0.3 V
<200 ns	SW − 2 V to BST + 0.3 V
DRVL	
DC	−0.3 V to V_{CC} + 0.3 V
<200 ns	−2 V to V_{CC} + 0.3 V
IN, $\overline{OD}$	−0.3 V to +6.5 V
θ_{JA}, SOIC_N	
2-Layer Board	123°C/W
4-Layer Board	90°C/W
θ_{JA}, LFCSP_VD[1]	
4-Layer Board	50°C/W
Operating Ambient Temperature Range	0°C to 85°C
Junction Temperature Range	0°C to 150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	260°C

[1] For LFCSP_VD, θ_{JA} is measured per JEDEC STD with exposed pad soldered to PCB.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Unless otherwise specified, all voltages are referenced to PGND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

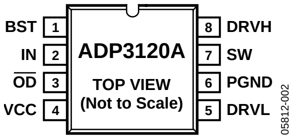


Figure 2. 8-Lead SOIC_N Pin Configuration

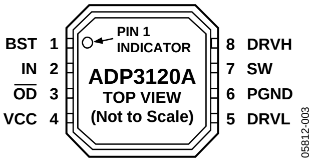


Figure 3. 8-Lead LFCSP_VD Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high-side MOSFET while it is switching.
2	IN	Logic Level PWM Input. This pin has primary control of the drive outputs. In normal operation, pulling this pin low turns on the low-side driver; pulling it high turns on the high-side driver.
3	$\overline{\text{OD}}$	Output Disable. When low, this pin disables normal operation, forcing DRVH and DRVL low.
4	VCC	Input Supply. This pin should be bypassed to PGND with an ~1 µF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. This pin should be closely connected to the source of the lower MOSFET.
7	SW	Switch Node Connection. This pin is connected to the buck switching node, close to the upper MOSFET source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent the lower MOSFET from turning on until the voltage is below ~1 V.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.

TIMING CHARACTERISTICS

Timing is referenced to the 90% and 10% points, unless otherwise noted.

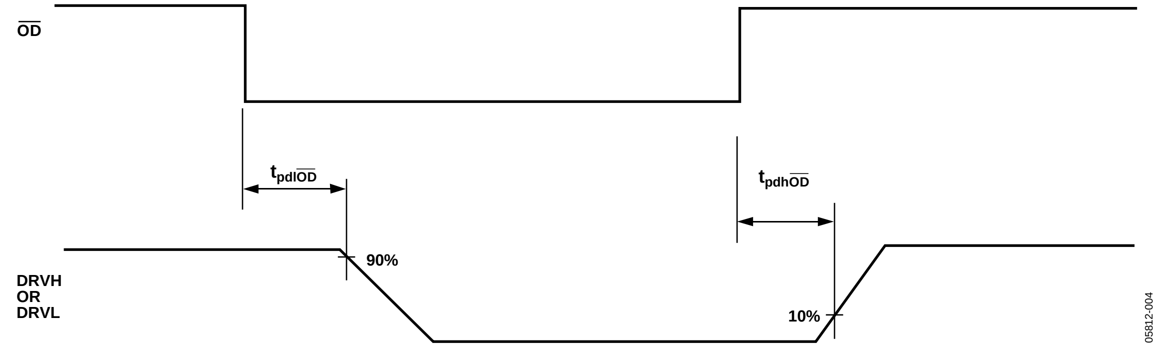


Figure 4. Output Disable Timing Diagram

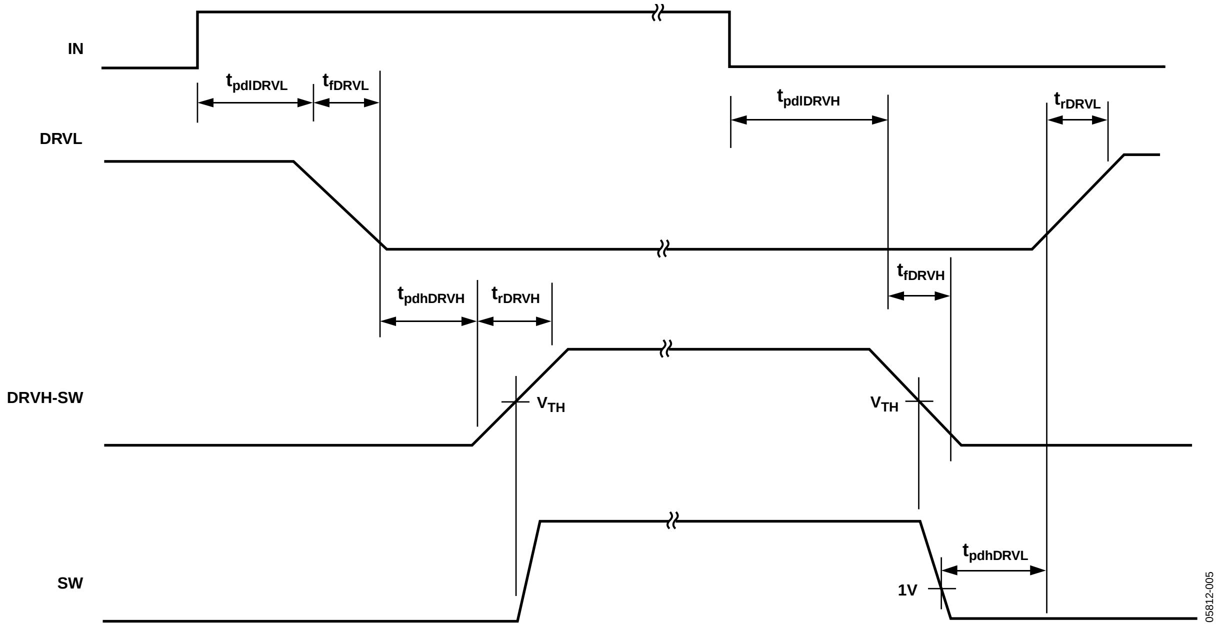


Figure 5. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

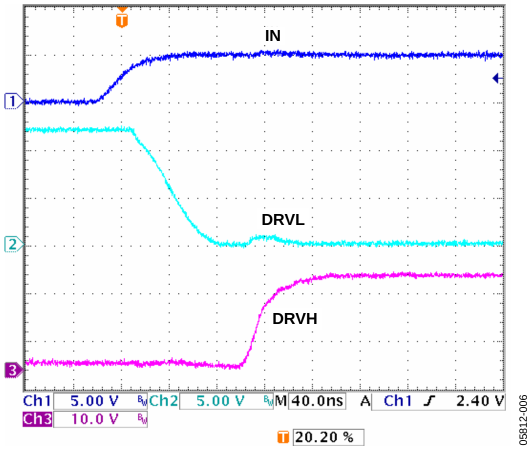


Figure 6. DRVH Rise and DRVL Fall Times
C_{LOAD} = 6 nF for DRVL, C_{LOAD} = 2 nF for DRVH

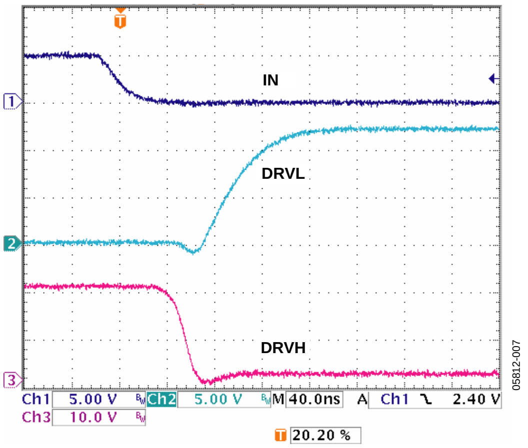


Figure 7. DRVH Fall and DRVL Rise Times
C_{LOAD} = 6 nF for DRVL, C_{LOAD} = 2 nF for DRVH

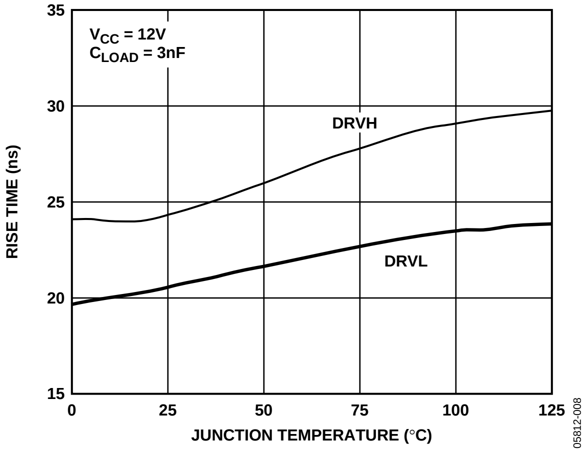


Figure 8. DRVH and DRVL Rise Times vs. Temperature

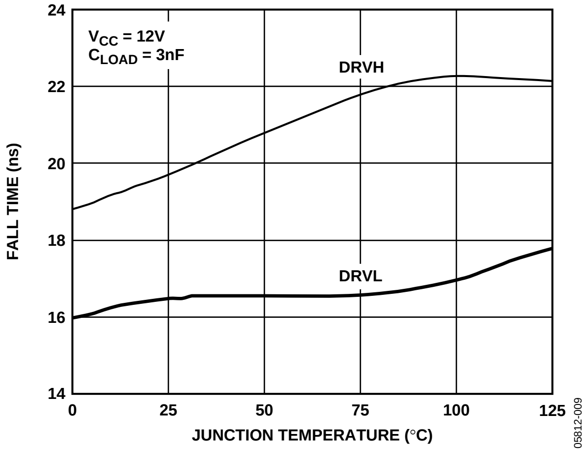


Figure 9. DRVH and DRVL Fall Times vs. Temperature

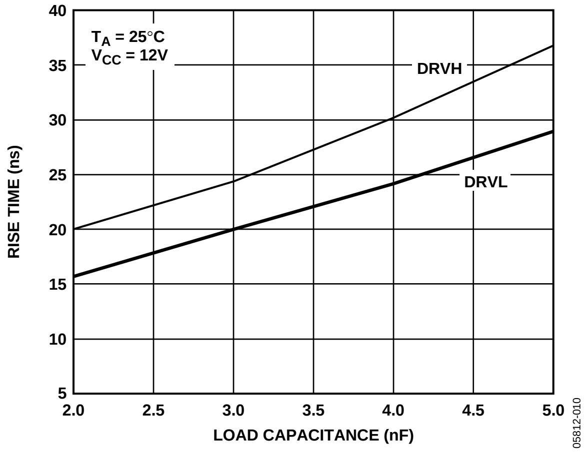


Figure 10. DRVH and DRVL Rise Times vs. Load Capacitance

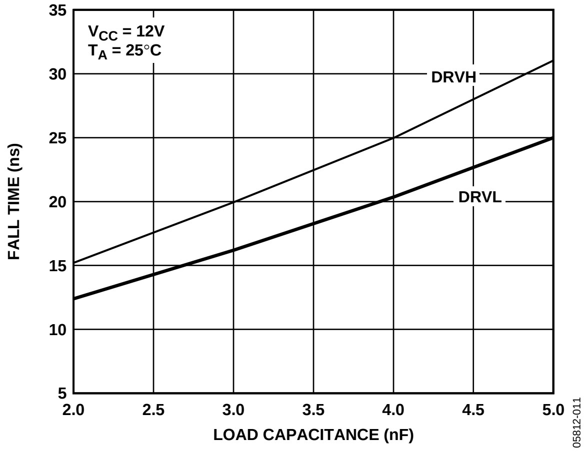


Figure 11. DRVH and DRVL Fall Times vs. Load Capacitance

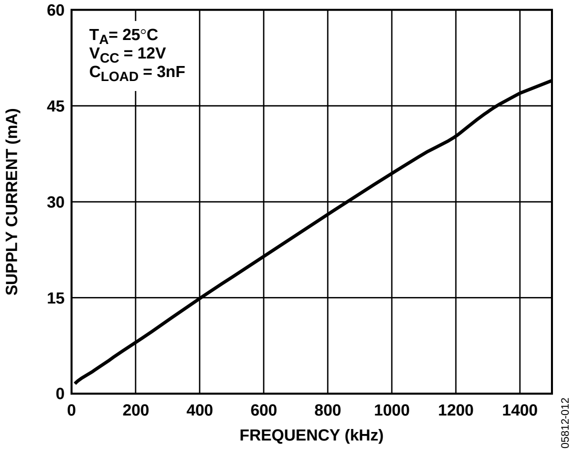


Figure 12. Supply Current vs. Frequency

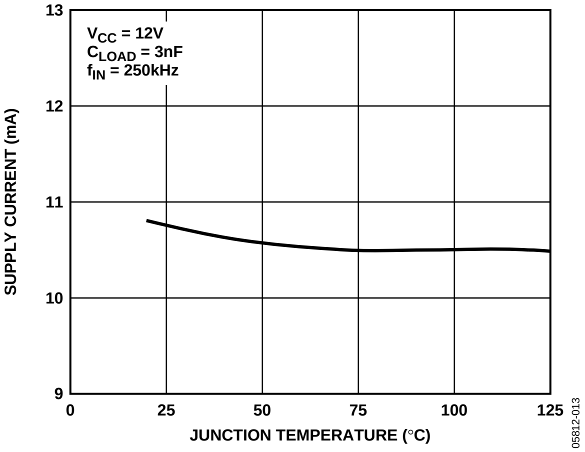


Figure 13. Supply Current vs. Temperature

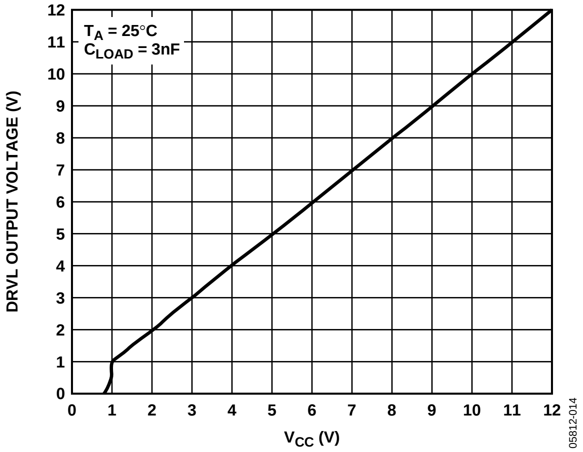


Figure 14. DRVL Output Voltage vs. Supply Voltage

THEORY OF OPERATION

The ADP3120A is optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 500 kHz. A functional block diagram of ADP3120A is shown in Figure 1.

LOW-SIDE DRIVER

The low-side driver is designed to drive a ground referenced N-channel MOSFET. The bias to the low-side driver is internally connected to the V_{CC} supply and PGND.

When the driver is enabled, the driver output is 180° out of phase with the PWM input. When the ADP3120A is disabled, the low-side gate is held low.

HIGH-SIDE DRIVER

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit that is connected between the BST and SW pins.

The bootstrap circuit comprises Diode D1 and Bootstrap Capacitor C_{BST1}. C_{BST2} and R_{BST} are included to reduce the high-side gate drive voltage and to limit the switch node slew rate (called a Boot-Snap™ circuit—see the Application Information section for more details). When the ADP3120A starts up, the SW pin is at ground, so the bootstrap capacitor charges up to V_{CC} through D1. When the PWM input goes high, the high-side driver begins to turn on the high-side MOSFET, Q1, by pulling charge out of C_{BST1} and C_{BST2}. As Q1 turns on, the SW pin rises up to V_{IN} and forces the BST pin to $V_{IN} + V_{C(BST)}$. This holds Q1 on because enough gate-to-source voltage is provided. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET, Q2, turns on, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to V_{CC} again.

The output of the high-side driver is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

OVERLAP PROTECTION CIRCUIT

The overlap protection circuit prevents both of the main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on/off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from the Q1 turn-off to the Q2 turn-on, and by internally setting the delay from the Q2 turn-off to the Q1 turn-on.

To prevent the overlap of the gate drives during the Q1 turn-off and the Q2 turn-on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 begins to turn off (after propagation delay). Before Q2 can turn on, the overlap protection circuit makes sure that SW has first gone high and then waits for the voltage at the SW pin to fall from V_{IN} to 1 V. Once the voltage on the SW pin falls to 1 V, Q2 begins turn-on. If the SW pin has not gone high first, the Q2 turn-on is delayed by a fixed 150 ns. By waiting for the voltage on the SW pin to reach 1 V or for the fixed delay time, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, input pulse width, gate charge, and drive current. If SW does not go below 1 V after 190 ns, DRVL turns on. This can occur if the current flowing in the output inductor is negative and flows through the high-side MOSFET body diode.

APPLICATION INFORMATION

SUPPLY CAPACITOR SELECTION

For the supply input (V_{CC}) of the ADP3120A, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents that are drawn. Use a 4.7 μF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the ADP3120A.

BOOTSTRAP CIRCUIT

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a diode, as shown in Figure 1. These components can be selected after the high-side MOSFET is chosen. The bootstrap capacitor must have a voltage rating that can handle twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitor values are determined by

$$C_{BST1} + C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} \tag{1}$$

$$\frac{C_{BST1}}{C_{BST1} + C_{BST2}} = \frac{V_{GATE}}{V_{CC} - V_D} \tag{2}$$

where:

Q_{GATE} is the total gate charge of the high-side MOSFET at V_{GATE}.
V_{GATE} is the desired gate drive voltage (usually in the range of 5 V to 10 V, 7 V being typical).
V_D is the voltage drop across D1.

Rearranging Equation 1 and Equation 2 to solve for C_{BST1} yields

$$C_{BST1} = 10 \times \frac{Q_{GATE}}{V_{CC} - V_D}$$

C_{BST2} can then be found by rearranging Equation 1

$$C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} - C_{BST1}$$

For example, an NTD60N02 has a total gate charge of about 12 nC at $V_{GATE} = 7$ V. Using $V_{CC} = 12$ V and $V_D = 1$ V, then $C_{BST1} = 12$ nF and $C_{BST2} = 6.8$ nF. Good quality ceramic capacitors should be used.

R_{BST} is used to limit slew rate and minimize ringing at the switch node. It also provides peak current limiting through D1. An R_{BST} value of 1.5 Ω to 2.2 Ω is a good choice. The resistor needs to handle at least 250 mW due to the peak currents that flow through it.

A small signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15 V rating to withstand the maximum supply voltage. The average forward current can be estimated by

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \tag{3}$$

where f_{MAX} is the maximum switching frequency of the controller.

The peak surge current rating should be calculated by

$$I_{F(PEAK)} = \frac{V_{CC} - V_D}{R_{BST}} \tag{4}$$

MOSFET SELECTION

When interfacing the ADP3120A to external MOSFETs, the designer should consider ways to make a robust design that minimizes stresses on both the driver and the MOSFETs. These stresses include exceeding the short time duration voltage ratings on the driver pins as well as the external MOSFET.

It is also highly recommended to use the Boot-Snap circuit to improve the interaction of the driver with the characteristics of the MOSFETs. If a simple bootstrap arrangement is used, make sure to include a proper snubber network on the SW node.

HIGH-SIDE (CONTROL) MOSFETS

A high-side, high speed MOSFET is usually selected to minimize switching losses (see the ADP3186 or ADP3188 data sheet for Flex-Mode controller details). This typically implies a low gate resistance and low input capacitance/charge device. Yet, a significant source lead inductance can also exist that depends mainly on the MOSFET package; it is best to contact the MOSFET vendor for this information.

The ADP3120A DRVH output impedance and the input resistance of the MOSFETs determine the rate of charge delivery to the internal capacitance of the gate. This determines the speed at which the MOSFETs turn on and off. However, because of potentially large currents flowing in the MOSFETs at the on and off times (this current is usually larger at turn-off due to ramping up of the output current in the output inductor), the source lead inductance generates a significant voltage when the high-side MOSFETs switch off. This creates a significant drain-source voltage spike across the internal die of the MOSFETs and can lead to a catastrophic avalanche. The mechanisms involved in this avalanche condition are referenced in literature from the MOSFET suppliers.

The MOSFET vendor should provide a rating for the maximum voltage slew rate at drain current around which this can be designed. Once this specification is obtained, determine the maximum current expected in the MOSFET by

$$I_{MAX} = I_{DC}(per\ phase) + (V_{CC} - V_{OUT}) \times \frac{D_{MAX}}{f_{MAX} \times L_{OUT}} \quad (5)$$

where:

D_{MAX} is determined for the VR controller being used with the driver. This current is divided roughly equally between MOSFETs if more than one is used (assume a worst-case mismatch of 30% for design margin).

L_{OUT} is the output inductor value.

When producing the design, there is no exact method for calculating the dV/dt due to the parasitic effects in the external MOSFETs as well as the PCB. However, it can be measured to determine if it is safe. If it appears that the dV/dt is too fast, an optional gate resistor can be added between DRVH and the high-side MOSFETs. This resistor slows down the dV/dt, but it increases the switching losses in the high-side MOSFETs. The ADP3120A is optimally designed with an internal drive impedance that works with most MOSFETs to switch them efficiently, yet minimizes dV/dt. However, some high speed MOSFETs can require this external gate resistor depending on the currents being switched in the MOSFET.

LOW-SIDE (SYNCHRONOUS) MOSFETS

The low-side MOSFETs are usually selected to have a low on resistance to minimize conduction losses. This usually implies a large input gate capacitance and gate charge. The first concern is to make sure the power delivery from the ADP3120A DRVL does not exceed the thermal rating of the driver (see the ADP3186, ADP3188, or ADP3189 data sheets for Flex-Mode controller details).

The next concern for the low-side MOSFETs is to prevent them from being inadvertently switched on when the high-side MOSFET turns on. This occurs due to the drain-gate (Miller capacitance, also specified as C_{rss} capacitance) of the MOSFET. When the drain of the low-side MOSFET is switched to V_{CC} by the high-side turning on (at a dV/dt rate), the internal gate of the low-side MOSFET is pulled up by an amount roughly equal to $V_{CC} \times (C_{rss}/C_{iss})$. It is important to make sure this does not put the MOSFET into conduction.

Another consideration is the nonoverlap circuitry of the ADP3120A that attempts to minimize the nonoverlap period. During the state of the high-side turning off to low-side turning on, the SW pin is monitored (as well as the conditions of SW prior to switching) to adequately prevent overlap.

However, during the low-side turn-off to high-side turn-on, the SW pin does not contain information for determining the proper switching time, so the state of the DRVL pin is monitored to go below one sixth of V_{CC}; then, a delay is added. Due to the Miller capacitance and internal delays of the low-side MOSFET gate, ensure that the Miller-to-input capacitance ratio is low enough, and that the low-side MOSFET internal delays are not so large as to allow accidental turn-on of the low-side when the high-side turns on.

Contact ADI for an updated list of recommended low-side MOSFETs.

PC BOARD LAYOUT CONSIDERATIONS

Use these general guidelines when designing printed circuit boards:

- Trace out the high current paths and use short, wide (>20 mil) traces to make these connections.
- Minimize trace inductance between DRVH and DRVL outputs and MOSFET gates.
- Connect the PGND pin of the ADP3120A as closely as possible to the source of the lower MOSFET.
- Locate the V_{CC} bypass capacitor as close as possible to the VCC and PGND pins.
- Use vias to other layers, when possible, to maximize thermal conduction away from the IC.

The circuit in Figure 16 shows how four drivers can be combined with an ADP3188 to form a total power conversion solution for generating $V_{CC\,(CORE)}$ for an Intel CPU that is VRD 10.x-compliant.

Figure 15 shows an example of the typical land patterns based on the guidelines given previously. For more detailed layout guidelines for a complete CPU voltage regulator subsystem, refer to the PC Board Layout Considerations section of the ADP3188 data sheet.

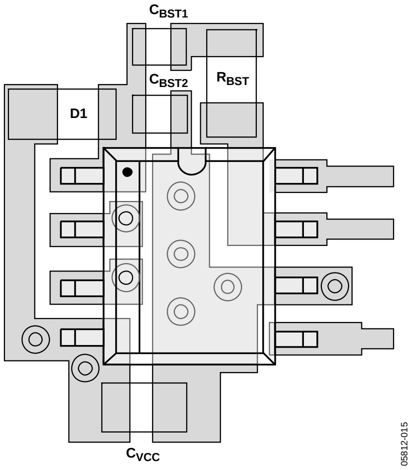
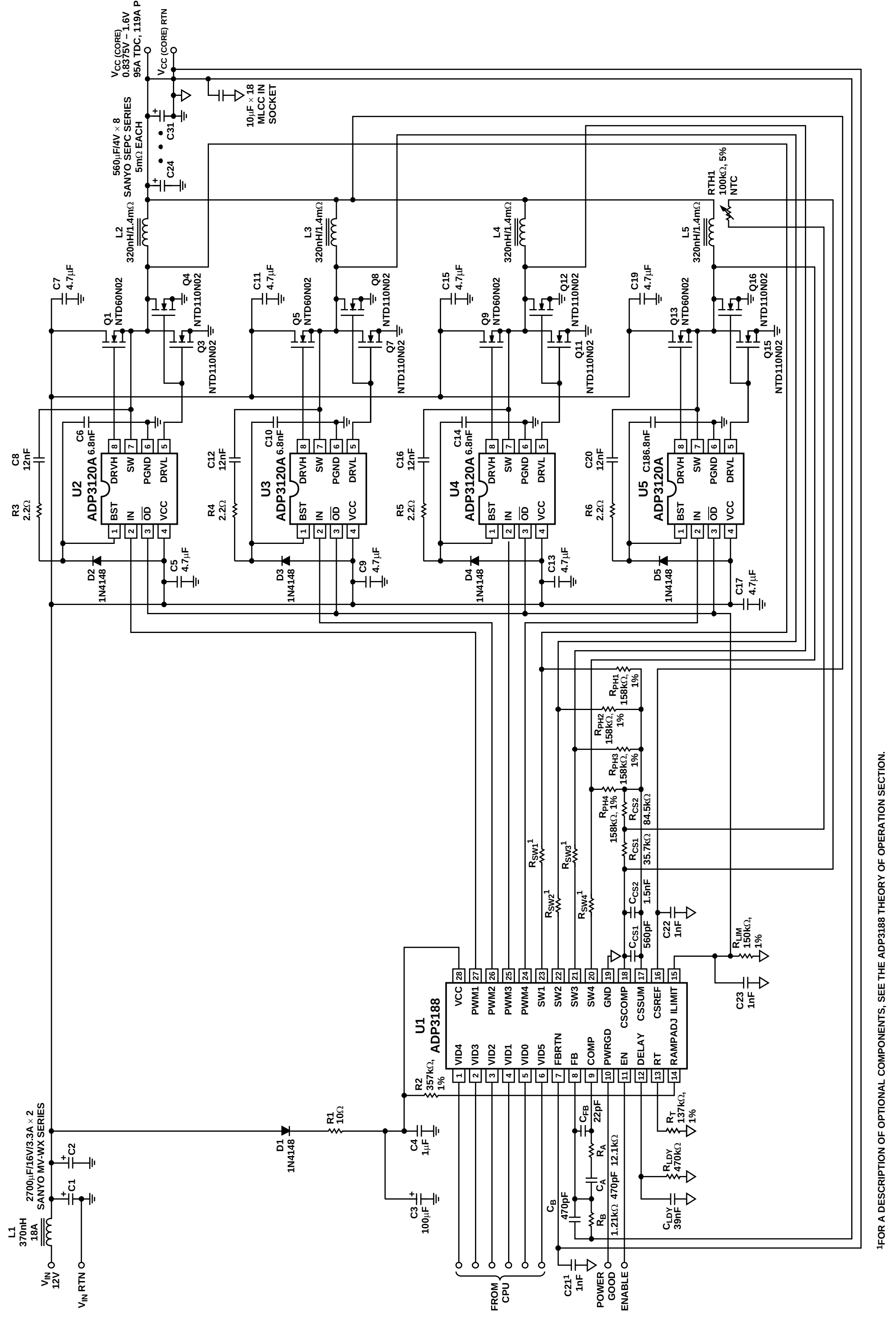


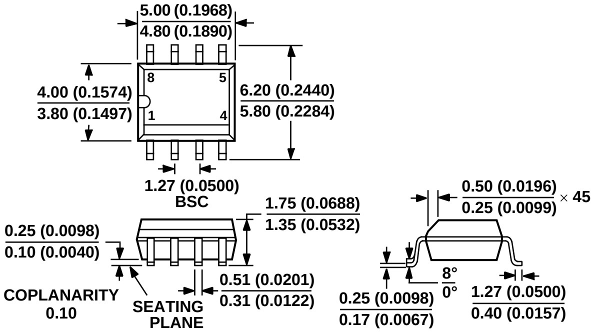
Figure 15. External Component Placement Example



[1]FOR A DESCRIPTION OF OPTIONAL COMPONENTS, SEE THE ADP3188 THEORY OF OPERATION SECTION.

Figure 16. VRD 10.x-Compliant Power Supply Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 17. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

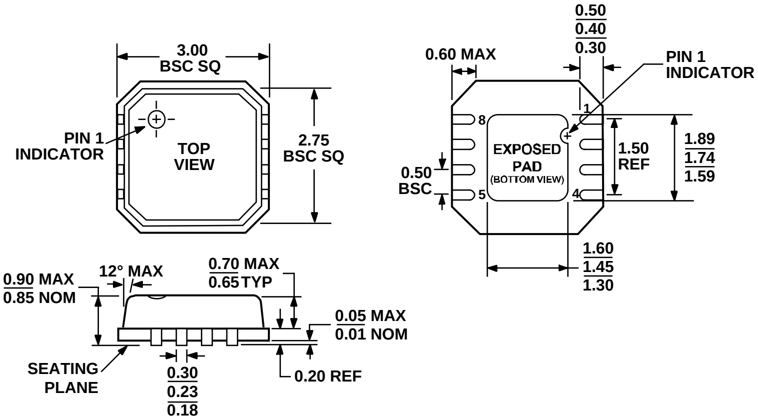


Figure 18. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm x 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADP3120AJRZ[1]	0°C to 85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	N/A	
ADP3120AJRZ-RL[1]	0°C to 85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	2,500	
ADP3120AJCPZ-RL[1]	0°C to 85°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	5,000	L3C

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

D05812-0-3/06(0)