VRM 8.5 Compatible Single Phase Core Controller

ADP3170

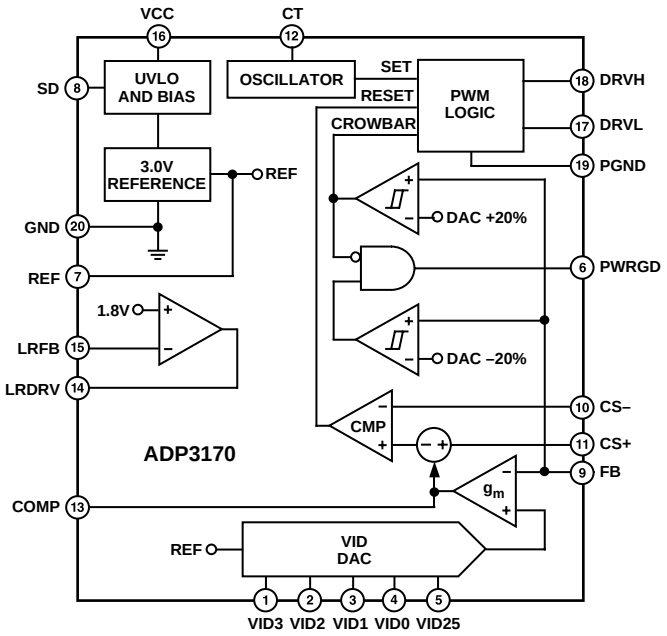
FEATURES

Optimally Compensated Active Voltage Positioning with Gain and Offset Adjustment (ADOPT™) for Superior Load Transient Response
Complies with VRM 8.5 Specifications with Lowest System Cost
5-Bit Digitally Programmable 1.05 V to 1.825 V Output
N-Channel Synchronous Buck Controller
Onboard 1.8 V Linear Regulator Controller
Total Accuracy ±1% Over Temperature
High Efficiency Current-Mode Operation
Short Circuit Protection
Power Good Output
Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

APPLICATIONS

Core and 1.8 V Standby Supplies for Next Generation Intel Pentium® III Processors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3170 is a highly efficient output synchronous buck switching regulator controller optimized for converting a 5 V main supply into the core supply voltage required by next generation Intel Celeron processors. The ADP3170 uses an internal 5-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.05 V and 1.825 V. The ADP3170 uses a current mode, constant off-time architecture to drive two N-channel MOSFETs at a programmable switching frequency that can be optimized for regulator size and efficiency.

The ADP3170 also uses a unique supplemental regulation technique called Analog Devices Optimal Positioning Technology (ADOPT) to enhance load transient performance. Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for high performance processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3170 also provides accurate and reliable short circuit protection and adjustable current limiting. It also includes an integrated overvoltage crowbar function to protect the microprocessor from destruction in case the core supply exceeds the nominal programmed voltage by more than 20%.

The ADP3170 contains a 1.8 V linear regulator controller that is designed to drive an external N-channel MOSFET. This linear regulator can be used to generate auxiliary voltages (such as 1.8 V standby power) required in most motherboard designs, and has been designed to provide a high bandwidth load-transient response.

The ADP3170 is specified over the commercial temperature range of 0°C to 70°C and is available in a 20-lead TSSOP package.

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Pentium is a registered trademark of Intel Corporation

REV. 0

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ADP3170—SPECIFICATIONS[1] (VCC = 12 V, I_{REF} = 150 μA, T_A = 0°C to 70°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FEEDBACK INPUT						
Output Accuracy	V_{FB}					
1.05 V Output		Figure 1	1.039	1.05	1.061	V
1.5 V Output		Figure 1	1.485	1.5	1.515	V
1.825 V Output		Figure 1	1.807	1.825	1.843	V
Line Regulation	ΔV_{OUT}	VCC = 10 V to 14 V		0.06		%
Input Bias Current	I_{FB}			5	50	nA
Crowbar Trip Point	$V_{CROWBAR}$	% of Nominal DAC Voltage	115	120	125	%
Crowbar Reset Point		% of Nominal DAC Voltage	40	50	60	%
Crowbar Response Time	$t_{CROWBAR}$	Overvoltage to DRVL Going High		400		ns
REFERENCE						
Output Voltage	V_{REF}		2.937	3.0	3.048	V
Output Current	I_{REF}		300			μA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$				0.8	V
Input High Voltage	$V_{IH(VID)}$		2.3			V
Input Current	I_{VID}	VID(X) = 0 V		300	425	μA
Pull-up Resistance	R_{VID}			16		kΩ
Internal Pull-up Voltage			2.75	3.1	3.4	V
SHUTDOWN INPUT						
Input Low Voltage	$V_{IL(SD)}$				0.8	V
Input High Voltage	$V_{IH(SD)}$		2.0			V
Input Current	I_{SD}				1	μA
OSCILLATOR						
Off Time		T_A = 25°C, CT = 200 pF	3.5	4.0	4.5	μs
CT Charge Current	I_{CT}	T_A = 25°C, V_{OUT} in Regulation	130	150	170	μA
		T_A = 25°C, V_{OUT} = 0 V	25	35	45	μA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$			1		MΩ
Transconductance	$g_{m(ERR)}$		2.05	2.2	2.35	mmho
Output Current	$I_{O(ERR)}$	FB = 0		625		μA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} – 3%		3.0		V
Output Disable Threshold	$V_{COMP(OFF)}$		600	750	900	mV
–3 dB Bandwidth	BW_{ERR}	COMP = Open		500		kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	FB Forced to V_{OUT} – 3%	69	78	87	mV
		FB ≤ 0.45 V	35	45	54	mV
		0.8 V ≤ COMP ≤ 1 V		1	5	mV
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS– = V_{OUT}		0.5	5	μA
Response Time	t_{CS}	CS+ – (CS–) > 87 mV to DRVH going low		50		ns
OUTPUT DRIVERS						
Output Resistance	$R_{O(DRV[X])}$	I_L = 50 mA		4.5		Ω
Output Transition Time	t_R, t_F	C_L = 3000 pF		75		ns
LINEAR REGULATOR						
Feedback Current	I_{LRFB}			0.3	1	μA
LR Feedback Voltage	V_{LRFB}	Figure 2, VCC = 4.5 V to 12.6 V	1.75	1.8	1.85	V
Driver Output Voltage	V_{LRDRV}	VCC = 4.5 V, $V_{LRFB(X)}$ = 0 V	4.2			V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	% of Nominal DAC Voltage	74	80	86	%
Undervoltage Hysteresis		% of Nominal DAC Voltage		5		%
Overvoltage Threshold	$V_{PWRGD(OV)}$	% of Nominal DAC Voltage	114	120	126	%
Overvoltage Reset Point		% of Nominal DAC Voltage	40	50	60	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 1 mA		250	500	mV
Response Time				200		ns
SUPPLY						
DC Supply Current[2]	I_{CC}			7.5	9.5	mA
UVLO Threshold Voltage	V_{UVLO}		6.75	7	7.25	V
UVLO Hysteresis			0.8	1	1.2	V

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
[2]Dynamic supply current is higher due to the gate charge being delivered to the external MOSFETs.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

VCC . . . . . –0.3 V to +15 V
DRVH, DRVL, LRDRV . . . . . –0.3 V to VCC + 0.3 V
All Other Inputs & Outputs . . . . . –0.3 V to +10 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
θ_{JA} . . . . . 143°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

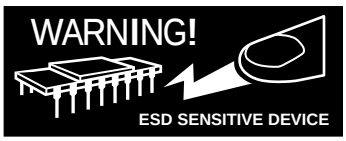
*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3170JRU	0°C to 70°C	TSSOP	RU-20

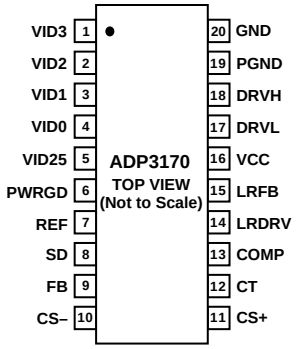
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3170 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION

RU-20



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1–5	VID3, VID2, VID1, VID0, VID25	Voltage Identification DAC Inputs. These pins are pulled up to an internal reference, providing a logic one if left open. The DAC output programs the FB regulation voltage from 1.05 V to 1.825 V.
6	PWRGD	Open drain output that signals when the output voltage is in the proper operating range.
7	REF	3.0 V Reference Output.
8	SD	Regulator Shutdown. Pulling this pin high turns off both MOSFETs of the switching regulator. SD has no effect on the linear regulator controller.
9	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
10	CS–	Current Sense Negative Node. Negative input for the current comparator.
11	CS+	Current Sense Positive Node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–.
12	CT	External capacitor connected from CT to ground sets the OFF-Time of the device.
13	COMP	Error Amplifier Output and Compensation Point. The voltage at this output programs the output current control level between CS+ and CS–.
14	LRDRV	Gate Drive for the 1.8 V linear regulator N-channel MOSFET.
15	LRFB	Feedback Connections for the 1.8 V linear regulator controller.
16	VCC	Supply Voltage for the ADP3170.
17	DRVL	Low-Side MOSFET Drive. Gate drive for the synchronous rectifier N-channel MOSFET. The voltage at DRVL swings from GND to VCC.
18	DRVH	High-Side MOSFET Drive. Gate drive for the buck switch N-channel MOSFET. The voltage at DRVH swings from GND to VCC.
19	PGND	Power Ground. PGND should have a low impedance path to the source of the synchronous MOSFET.
20	GND	Small-Signal Ground. This ground reference can be used in conjunction with FB to provide remote sensing of the output voltage at the CPU pins.

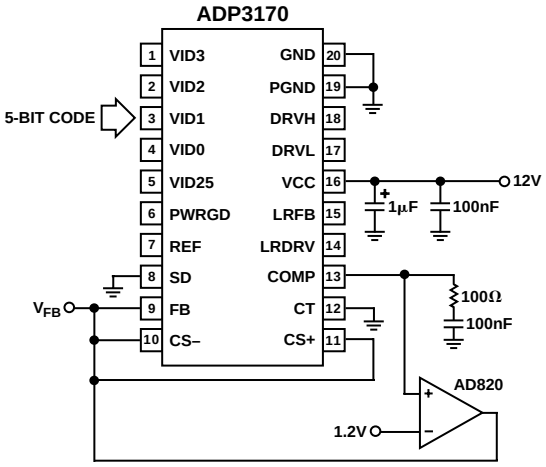


Figure 1. Closed-Loop Output Voltage Accuracy Test Circuit

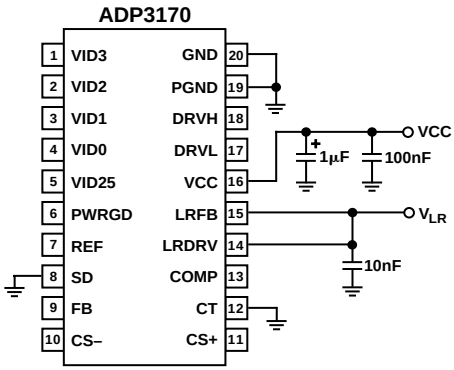
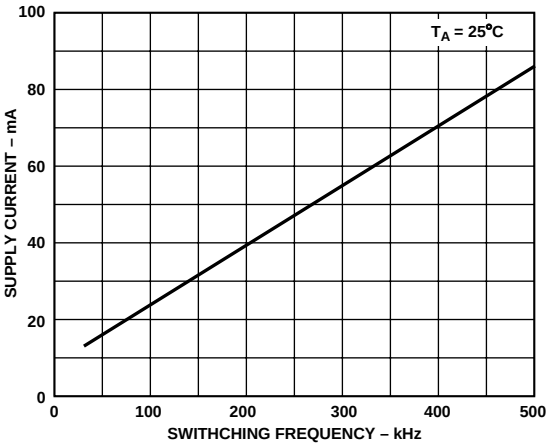
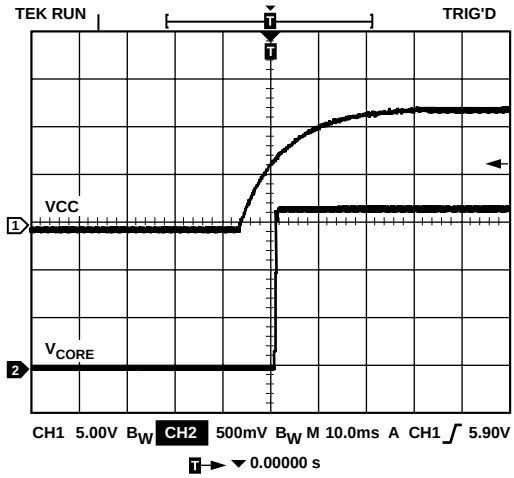


Figure 2. Linear Regulator Output Voltage Accuracy Test Circuit

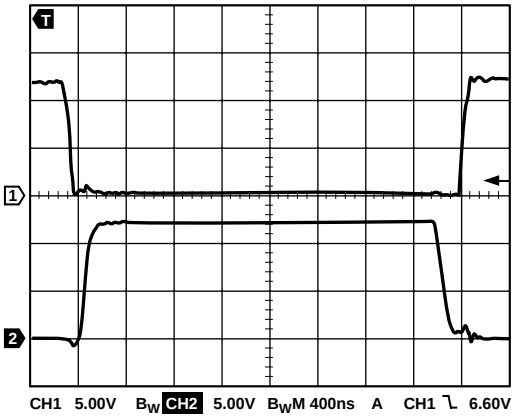
ADP3170–Typical Performance Characteristics



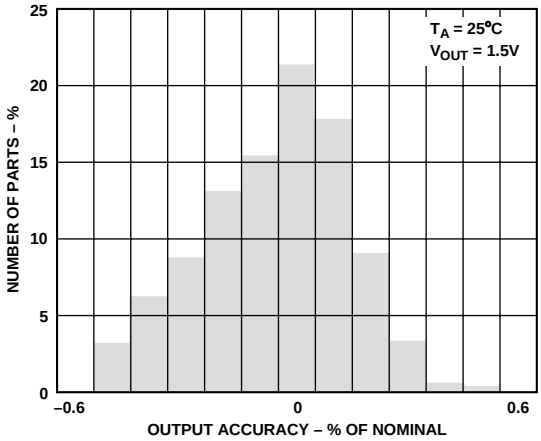
TPC 1. Supply Current vs. Operating Frequency Using MOSFETs of Figure 3



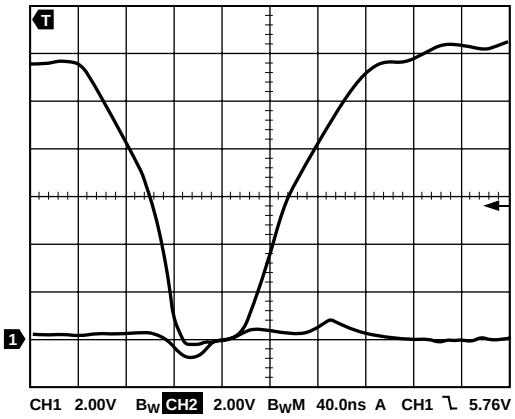
TPC 4. Power-On Start-Up Waveform



TPC 2. Gate Switching Waveforms Using MOSFETs of Figure 3



TPC 5. Output Accuracy Distribution



TPC 3. Driver Transition Waveforms Using MOSFETs of Figure 3

THEORY OF OPERATION

The ADP3170 uses a current-mode, constant off-time control technique to switch a pair of external N-channel MOSFETs in a synchronous buck topology. Constant off-time operation offers several performance advantages, including that no slope compensation is required for stable operation. A unique feature of the constant off-time control technique is that since the off-time is fixed, the converter's switching frequency is a function of the ratio of input voltage to output voltage. The fixed off-time is programmed by the value of an external capacitor connected to the CT pin. The on-time varies in such a way that a regulated output voltage is maintained as described below in the cycle-by-cycle operation. Under fixed operating conditions the on-time does not vary, and it varies only slightly as a function of load. This means that switching frequency is fairly constant in standard VRM applications.

Active Voltage Positioning

The output voltage is sensed at the CS– pin. A voltage error amplifier, (g_m), amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed to between 1.05 V and 1.825 V by an internal 5-bit DAC, which reads the code at the voltage identification (VID) pins. (Refer to Table I for output voltage vs. VID pin code information.) A unique supplemental regulation technique called Analog Devices Optimal Positioning Technology (ADOPT) adjusts the output voltage as a function of the load current so that it is always optimally positioned for a load transient. Standard (passive) voltage positioning, sometimes recommended for use with other architectures, has poor dynamic performance that renders it ineffective under the stringent repetitive transient conditions specified in Intel VRM documents. Consequently, such techniques do not allow the minimum possible number of output capacitors to be used. ADOPT, as used in the ADP3170, provides a bandwidth for transient response that is limited only by parasitic output inductance. This yields optimal load transient response with the minimum number of output capacitors.

Reference Output

A 3.0 V reference is available on the ADP3170. This reference is normally used to accurately set the voltage positioning using a resistor divider to the COMP pin. In addition, the reference can be used for other functions such as generating a regulated voltage with an external amplifier. The reference is bypassed with a 1 nF capacitor to ground. It is not intended to drive larger capacitive loads, and it should not be used to provide more than 300 μA of output current.

Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage error amplifier and the current comparator are the main control elements. During the on-time of the high side MOSFET, the current comparator monitors the voltage between the CS+ and CS– pins. When the voltage level between the two pins reaches the threshold level, the DRVH output is switched to ground, which turns off the high side MOSFET. The timing capacitor CT is then charged at a rate determined by the off-time controller. While the timing capacitor is charging, the DRVL output goes high, turning on the low side MOSFET. When the voltage level on the timing capacitor has charged to the upper threshold voltage level, a comparator resets a latch. The output of the latch forces the low side drive output to go low and the high side drive output to go high. As a result, the low side switch is turned off and the high side switch is turned on. The sequence is then repeated. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the voltage-error amplifier, which, in turn, leads to an increase in the current comparator threshold, thus tracking the load current. To prevent cross conduction of the external MOSFETs, feedback is incorporated to sense the state of the driver output pins. Before the low side drive output can go high, the high side drive output must be low. Likewise, the high side drive output is unable to go high while the low side drive output is high.

Output Crowbar

An added feature of using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. If the output voltage is 20% greater than the targeted value, the ADP3170 will turn on the lower MOSFET, which will current-limit the source power supply or blow its fuse, pull down the output voltage, and thus save the microprocessor from destruction. The crowbar function releases at approximately 50% of the nominal output voltage. For example, if the output is programmed to 1.5 V, but is pulled up to 1.85 V or above, the crowbar will turn on the lower MOSFET. If in this case the output is pulled down to less than 0.75 V, the crowbar will release, allowing the output voltage to recover to 1.5 V if the fault condition has been removed.

Onboard Linear Regulator Controller

The ADP3170 includes a linear regulator controller to provide a low cost solution for generating an additional supply rail. This regulator is internally set to 1.8 V with ±2.8% accuracy. The output voltage is sensed by the high input impedance LRFB pin and compared to an internal fixed reference. The LRDRV pin controls the gate of an external N-channel MOSFET resulting in a negative feedback loop. The only additional components required are a capacitor and resistor for stability. Higher output voltages can be generated by placing a resistor divider between the linear regulator output and its LRFB pin. The maximum output load current is determined by the size and thermal impedance of the external power MOSFET that is placed in series with the supply and controlled by the ADP3170.

APPLICATION INFORMATION

Specifications for a Design Example

The design parameters for a typical VRM 8.5-compliant Pentium III application (shown in Figure 3) are as follows:

Input voltage: (V_{IN}) = 5 V

Auxiliary input: (V_{CC}) = 12 V

VID setting voltage: (V_{OUT}) = 1.8 V

Nominal output voltage at no load (V_{ONL}) = 1.845 V

Nominal output voltage at maximum load (V_{OFL}) = 1.771 V

Static output voltage drop based on a 3.2 mW load line (R_{OUT}) from no load to full load (V_{Δ}) = $V_{ONL} - V_{OFL}$ = 1.845 V – 1.771 V = 74 mV

Maximum output current ($I_{O[MAX]}$) = 23 A

CT Selection for Operating Frequency

The ADP3170 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor CT. Each time the high-side N-channel MOSFET switch turns on, the voltage across CT is reset to approximately 0 V. During the off-time, CT is charged by a constant current of 150 μA. Once CT reaches 3.0 V, a new on-time cycle is initiated. The value of the off-time is calculated using the continuous-mode operating frequency. Assuming a nominal operating frequency (f_{NOM}) of 200 kHz at an output voltage of 1.8 V, the corresponding off-time is:

$$t_{OFF} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{f_{NOM}} = \left(1 - \frac{1.8\,V}{5\,V}\right) \times \frac{1}{200\,kHz} = 3.2\,\mu s \quad (1)$$

The timing capacitor cab be calculated from the equation:

$$C_T = \frac{t_{OFF} \times I_{CT}}{V_{T(TH)}} = \frac{3.2\,\mu s \times 150\,\mu A}{3\,V} \approx 150\,pF \quad (2)$$

The converter operates at the nominal operating frequency only at the above-specified V_{OUT} and at light load. At higher values of V_{OUT}, or under heavy load, the operating frequency decreases due to the parasitic voltage drops across the power devices. The actual minimum frequency at V_{OUT} = 1.8 *V* is calculated to be 183 *kHz* (see Equation 3), where:

$R_{DS(ON)HSF}$ is the resistance of the high-side MOSFET (estimated value: 6 mΩ)

$R_{DS(ON)LSF}$ is the resistance of the low-side MOSFET (estimated value: 6 mΩ)

R_{SENSE} is the resistance of the sense resistor (estimated value: 2.5 mΩ)

R_L is the resistance of the inductor (estimated value: 3 mΩ)

Table I. Output Voltage vs. VID Code

VID3	VID2	VID1	VID0	VID25	$V_{OUT(NOM)}$
0	1	0	0	0	1.050 V
0	1	0	0	1	1.075 V
0	0	1	1	0	1.100 V
0	0	1	1	1	1.125 V
0	0	1	0	0	1.150 V
0	0	1	0	1	1.175 V
0	0	0	1	0	1.200 V
0	0	0	1	1	1.225 V
0	0	0	0	0	1.250 V
0	0	0	0	1	1.275 V
1	1	1	1	0	1.300 V
1	1	1	1	1	1.325 V
1	1	1	0	0	1.350 V
1	1	1	0	1	1.375 V
1	1	0	1	0	1.400 V
1	1	0	1	1	1.425 V
1	1	0	0	0	1.450 V
1	1	0	0	1	1.475 V
1	0	1	1	0	1.500 V
1	0	1	1	1	1.525 V
1	0	1	0	0	1.550 V
1	0	1	0	1	1.575 V
1	0	0	1	0	1.600 V
1	0	0	1	1	1.625 V
1	0	0	0	0	1.650 V
1	0	0	0	1	1.675 V
0	1	1	1	0	1.700 V
0	1	1	1	1	1.725 V
0	1	1	0	0	1.750 V
0	1	1	0	1	1.775 V
0	1	0	1	0	1.800 V
0	1	0	1	1	1.825 V

$$f_{MIN} = \frac{1}{t_{OFF}} \times \frac{V_{IN} - I_{O(MAX)} \times \left(R_{DS(ON)HSF} + R_{SENSE} + R_L\right) - V_{OUT}}{V_{IN} - I_{O(MAX)} \times \left(R_{DS(ON)HSF} + R_{SENSE} + R_L - R_{DS(ON)LSF}\right)} = \frac{1}{3.3\,\mu s} \times \frac{5V - 23\,A \times (6\,m\Omega + 3\,m\Omega) - 1.8\,V}{5V - 23\,A \times (6\,m\Omega + 2.5\,m\Omega + 3\,m\Omega - 6\,m\Omega)} = 183\,kHz \quad (3)$$

Inductance Selection

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, output capacitors with less total capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. The following equation shows the relationship between the inductance, oscillator frequency, peak-to-peak ripple current in an inductor and input and output voltages:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{L(RIPPLE)}} \quad (4)$$

For 6 A peak-to-peak ripple current, which corresponds to approximately 25% of the 23 A full-load dc current in an inductor, Equation 4 yields an inductance of:

$$L = \frac{1.8\,V \times 3.3\,\mu s}{6\,A} = 990\,nH$$

A 1 μH inductor can be used, which gives a calculated ripple current of 5.9 A at no load. The inductor should not saturate at the peak current of 26 A and should be able to handle the sum of the power dissipation caused by the average current of 23 A in the winding and the core loss.

Designing an Inductor

Once the inductance is known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-M® from Magnetics, Inc.) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

Two main core types can be used in this application. Open magnetic loop types, such as beads, beads on leads, and rods and slugs, provide lower cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed-loop types, such as pot cores, PQ, U, and E cores, or toroids, cost more, but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table II gives some examples.

Table II. Magnetics Design References

Magnetic Designer Software
Intusoft (http://www.intusoft.com)
Designing Magnetic Components for High-Frequency DC-DC Converters
McLyman, Kg Magnetics
ISBN 1-883107-00-08

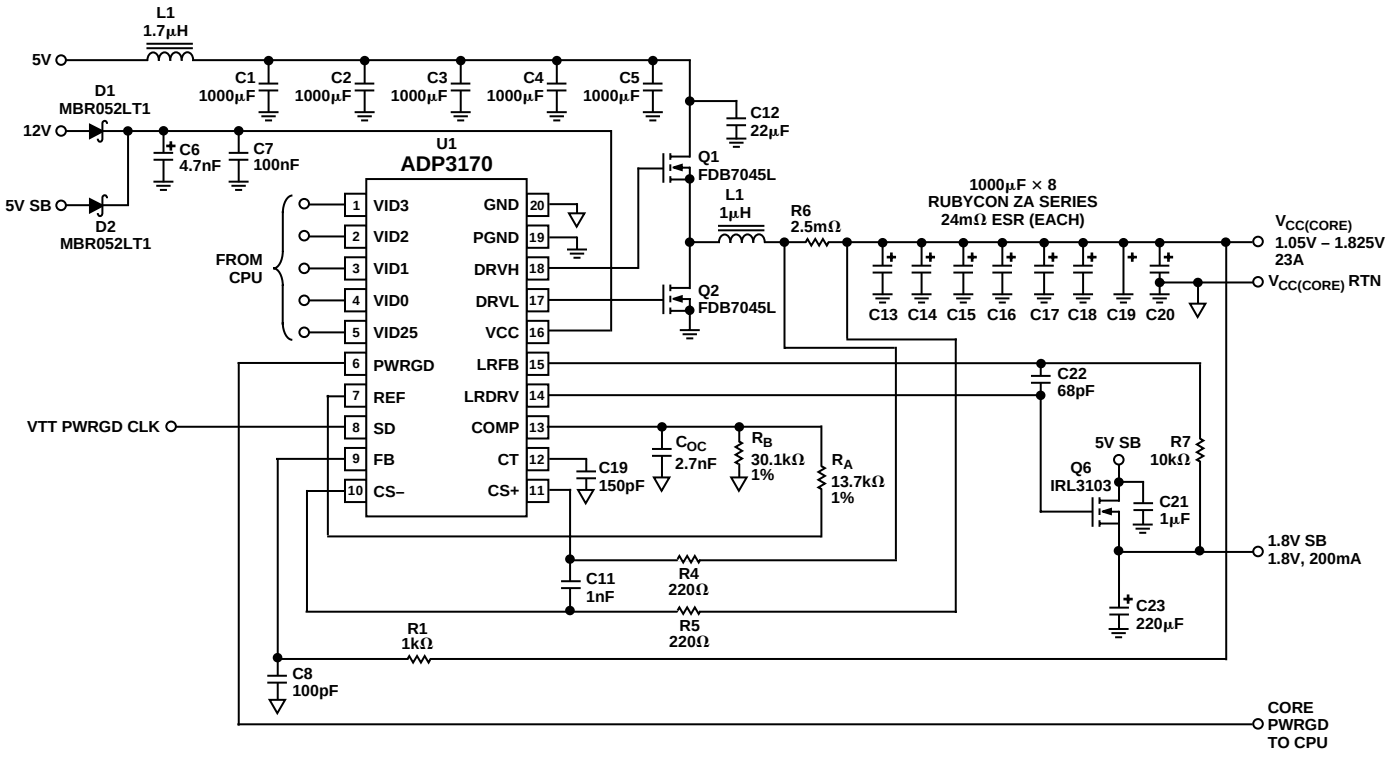


Figure 3. 24 A VRM 8.5-Compliant CPU Supply

Selecting a Standard Inductor

The companies listed in Table III can provide design consultation and deliver power inductors optimized for high power applications upon request.

Table III. Power Inductor Manufacturers

Coilcraft (847) 639-6400 http://www.coilcraft.com
Coiltronics (561) 752-5000 http://www.coiltronics.com
Sumida Electric Company (408) 982-9660 http://www.sumida.com

R_{SENSE}

The value of R_{SENSE} is based on the required maximum output current. The current comparator of the ADP3170 has a minimum threshold of 69 mV. Note that this minimum value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and transients.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, $I_{O(MAX)}$, which equals the peak value less half of the peak-to-peak ripple current. Solving for R_{SENSE} allowing a 20% margin for overhead and using the minimum current sense threshold of 69 mV yields:

$$R_{SENSE} = \frac{V_{CS(TH)(MIN)}}{I_{O(MAX)} + \frac{I_{RIPPLE}}{2}} = \frac{69\ mV}{23\ A + \frac{5.9\ A}{2}} = 2.66\ m\Omega \quad (5)$$

In this case, 2.5 $m\Omega$ was chosen, assuming two 5 mΩ, 1 W resistors in parallel (for power dissipation reasons). Once R_{SENSE} has been chosen, the output current at the point where current limit is reached, $I_{OUT(CL)}$, can be calculated using the maximum current sense threshold of 87 mV:

$$I_{OUT(CL)} = \frac{V_{CS(TH)(MAX)}}{R_{SENSE}} - \frac{I_{L(RIPPLE)}}{2}$$
$$I_{OUT(CL)} = \frac{87\ mV}{2.5\ m\Omega} - \frac{5.9\ A}{2} = 31.6\ A \quad (6)$$

At output voltages below 450 mV, the current sense threshold is reduced to 54 mV, and the ripple current is negligible. Therefore, the worst-case dead short output current is reduced to:

$$I_{OUT(SC)} = \frac{V_{CS(SC)}}{R_{SENSE}} = \frac{54\ mV}{2.5\ m\Omega} = 21.6\ A \quad (7)$$

To safely carry the current under maximum load conditions, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = {I_O}^2 \times R_{SENSE} = 23\ A^2 \times 2.5\ m\Omega = 1.33\ W \quad (8)$$

Output Resistance

Intel's VRM 8.5 specification requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a dc output resistance of:

$$R_{OUT} = \frac{V_{ONL} - V_{OFL}}{\Delta I_O} = \frac{1.845\ V - 1.771\ V}{23\ A} = 3.2\ m\Omega \quad (9)$$

The required dc output resistance can be achieved by terminating the g_m amplifier with a resistor. The value of the total termination resistance that will yield the correct dc output resistance is:

$$R_T = \frac{n_I \times R_{SENSE}}{g_m \times R_{OUT}} = \frac{25 \times 2.5\ m\Omega}{2.2\ mmho \times 3.2\ m\Omega} = 8.88\ k\Omega \quad (10)$$

where n_I is the division ratio from the output voltage signal of the g_m amplifier to the PWM comparator and g_m is the transconductance of the g_m amplifier itself.

Output Offset

Intel's VRM 8.5 specification requires that at no load the output voltage of the regulator module be offset to a higher value than the nominal voltage corresponding to the VID code. The offset is introduced by realizing the total termination resistance of the g_m amplifier with a divider connected between the REF pin and ground. The resistive divider introduces an offset to the output of the g_m amplifier that, when reflected back through the gain of the g_m stage, accurately positions the output voltage near its allowed maximum at light load. Furthermore, the output of the g_m amplifier sets the current sense threshold voltage. At no load, the current sense threshold is increased by the peak of the ripple current in the inductor and reduced by the delay between sensing when the current threshold has been reached and when the high side MOSFET actually turns off. These two factors are combined with the inherent voltage (V_{GNL0}), at the output of the g_m amplifier that commands a current sense threshold of 0 mV:

$$V_{GNL} = V_{ONL} + \frac{I_{L(RIPPLE)} \times R_{OUT} \times n_I}{2}$$
$$\frac{V_{IN} - V_{OUT}}{L} \times t_D \times R_{SENSE} \times n_I$$
$$V_{GNL} = 1\ V + \frac{5.9\ A \times 3.2\ m\Omega \times 25}{2} -$$
$$\frac{5\ V - 1.8\ V}{1\ \mu H} \times 60\ ns \times 2.5\ m\Omega \times 25 = 1.224\ V \quad (11)$$

The divider resistors (R_A for the upper, and R_B for the lower) can now be calculated assuming that the internal resistance of the g_m amplifier (R_{OGM}) is 130 kΩ:

$$R_B = \frac{V_{REF}}{\frac{V_{REF} - V_{GNL}}{R_T} - g_m \times V +}$$
$$R_B = \frac{3\ V}{\frac{3\ V - 1.224\ V}{8.88\ k\Omega} - 2.2\ mmho \times 45\ mV} = 29.7\ k\Omega \quad (12)$$

Choosing the nearest 1% resistor value gives R_B = 30.1 $k\Omega$. Finally, R_A is calculated:

$$R_A = \frac{1}{\frac{1}{R_T} - \frac{1}{R_{OGM}} - \frac{1}{R_B}} \quad (13)$$

$$R_A = \frac{1}{\frac{1}{8.88\ k\Omega} - \frac{1}{1\ M\Omega} - \frac{1}{29.7\ k\Omega}} = 12.83\ k\Omega$$

Choosing the nearest 1% resistor value gives R_A = 12.7 kΩ.

C_{OUT} Selection

The required equivalent series resistance (ESR) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR of the output filter capacitor bank must be equal to or less than the specified output resistance of the voltage regulator (3.2 mΩ). The capacitance must be large enough that the voltage across the capacitor, which is the sum of the resistive and capacitive voltage drops, does not move below or above the initial resistive step while the inductor current ramps up or down to the value corresponding to the new load current. One can use, for example, eight ZA series capacitors from Rubycon, which have a maximum ESR of 24 mΩ. These eight 1000 µF capacitors would give an ESR of 3 mΩ.

As long as the capacitance of the output capacitor is above a critical value, and the regulating loop is compensated with Analog Devices' proprietary compensation technique (ADOPT), the actual value has no influence on the peak-to-peak deviation of the output voltage to a full step change in the load current. The critical capacitance can be calculated as follows:

$$C_{OUT(CRIT)} = \frac{I_O}{R_{OUT} \times (V_{OUT} + V-)} \times L \quad (14)$$

$$C_{OUT(CRIT)} = \frac{23A}{3.2\ m\Omega \times (1.8\ V + [-29\ mV])} \times 1\ \mu H = 4.06\ mF$$

The equivalent capacitance of the eight ZA series Rubycon capacitors is 8 × 1 mF = 8 mF. In this case, the total capacitance is safely above the critical value.

Feedback Loop Compensation Design for ADOPT

Optimized compensation of the ADP3170 allows the best possible containment of the peak-to-peak output voltage deviation. The output current slew rate of any practical switching power converter is inherently limited by the inductor to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and assuming that the capacitance of the output capacitor is larger than the critical value defined by Equation 14, this will produce a peak output voltage deviation equal to the ESR of the output capacitor times the load current change.

The optimal implementation of voltage positioning, ADOPT, will create an output impedance of the power converter that is entirely resistive over the widest possible frequency range, including dc, and equal to the specified dc output resistance. With the wide-band resistive output impedance the output voltage will droop in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output capacitor.

With an ideal current-mode controlled converter, where the inductor current would respond without delay to the command signal, the resistive output impedance could be achieved by having a single-pole roll-off of the voltage gain of the voltage-error amplifier. The pole frequency must coincide with the ESR zero of the output capacitor.

The ADP3170 uses peak-current control, which is known to have a nonideal, frequency-dependent command signal-to-inductor current transfer function. The frequency dependence manifests in the form of a pair of complex conjugate poles at one-half of the switching frequency. A purely resistive output impedance could be achieved by canceling the complex conjugate with zeros at the same complex frequencies and adding a third pole equal to the ESR zero of the output capacitor. Such a compensating network would be quite complicated. Fortunately, in practice, it is sufficient to cancel the pair of complex conjugate poles with a single real zero placed at one-half of the switching frequency.

Although the end result is not a perfectly resistive output impedance, the remaining frequency dependence causes only a slight percentage of deviation from the ideal resistive response. The single-pole and single-zero compensation can be easily implemented by terminating the g_m error amplifier with the parallel combination of a resistor (R_T) and a series RC network. The value of the terminating resistor R_T was determined previously; the capacitance and resistance of the series RC network are calculated as follows:

$$C_{OC} = \frac{C_{OUT} \times ESR}{R_T} \quad (15)$$

$$C_{OC} = \frac{8\ mF \times 3\ m\Omega}{8.88\ k\Omega} = 2.7\ nF$$

The closest standard value is 2.7 *nF*. The series resistance is:

$$R_Z = \frac{2}{C_{OC} \times \pi \times f_{MIN}} \quad (16)$$

$$R_Z = \frac{2}{2.7\ nF \times \pi \times 188\ kHz} = 1255\ \Omega$$

The nearest standard 5% resistor value is 1.2 kΩ. Note that this resistor is only required when C_{OUT} approaches C_{CRIT} (within 25% or less). In this example, C_{OUT} >> C_{CRIT}, and R_Z can therefore be omitted.

Power MOSFETs

Two external N-channel power MOSFETs must be selected for use with the ADP3170, one for the main switch and one for the synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage ($V_{GS(TH)}$), the ON-resistance ($R_{DS(ON)}$), and the gate charge (Q_G). Logic-level MOSFETs are highly recommended. Only logic-level MOSFETs with V_{GS} ratings higher than the absolute maximum value of V_{CC} should be used.

The maximum output current $I_{O(MAX)}$ determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3170 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. For V_{IN} = 5 V and V_{OUT} = 1.8 V, the maximum duty ratio of the high-side FET is:

$$D_{HSF(MAX)} = 1 - \left(f_{MIN} \times t_{OFF}\right)$$
$$D_{HSF(MAX)} = 1 - (183\,kHz \times 3.3\,\mu s) = 40\% \quad (17)$$

The maximum duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF(MAX)} = 1 - D_{HSF(MAX)} = 60\% \quad (18)$$

The maximum rms current of the high-side MOSFET is:

$$I_{HSF(MAX)} = \sqrt{D_{HSF(MAX)} \times \frac{I_{L(VALLEY)}^2 + \left(I_{L(VALLEY)} \times I_{L(PEAK)}\right) + vI_{L(PEAK)}^2}{3}}$$
$$I_{HSF(MAX)} = \sqrt{0.4 \times \frac{17.4\,A^2 + (17.4\,A \times 28.6\,A) + 28.6\,A^2}{3}} = 14.7\,A \quad (19)$$

The maximum rms current of the low-side MOSFET is:

$$I_{LSF(MAX)} = \sqrt{D_{LSF(MAX)} \times \frac{I_{L(VALLEY)}^2 + \left(I_{L(VALLEY)} \times I_{L(PEAK)}\right) + I_{L(PEAK)}^2}{3}}$$
$$I_{HSF(MAX)} = \sqrt{0.6 \times \frac{17.4\,A^2 + \left(17.4\,A \times 28.6\,A\right) + 28.6\,A^2}{3}} = 18\,A \quad (20)$$

The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation will be:

$$P_{D(FETS)} = 0.1 \times V_{OUT} \times I_{OUT(MAX)}$$
$$P_{D(FETS)} = 0.1 \times 1.8\,V \times 23\,A = 4.1\,W \quad (21)$$

Allocating half of the total dissipation for the high-side MOSFET and half for the low-side MOSFET, and assuming that the resistive loss of the high-side MOSFET is one-third, and the switching loss is two-thirds of its portion, the required maximum MOSFET resistances will be:

$$R_{DS(ON)HSF} = \frac{P_{D(FETS)}}{3 \times I_{HSF(MAX)}^2} = \frac{4.1\,W}{3 \times 14.7\,A^2} = 6\,m\Omega \quad (22)$$

$$R_{DS(ON)LS} = \frac{P_{D(FETS)}}{I_{LSF(MAX)}^2} = \frac{4.1\,W}{2 \times 18\,A^2} = 6\,m\Omega \quad (23)$$

Note that there is a trade-off between converter efficiency and cost. Larger MOSFETs reduce the conduction losses and allow higher efficiency, but increase the system cost. A Fairchild FDB7045L ($R_{DS(ON)}$ = 4.5 mΩ nominal, 6 mΩ worst-case) is a good choice for both the low-side and high-side MOSFET.

With this choice, the high-side MOSFET dissipation is:

$$P_{HSF} = R_{DS(ON)HSF} \times I_{HSF(MAX)}^2 + \frac{V_{IN} \times I_{L(PEAK)} \times Q_G \times f_{MIN}}{2 \times I_G} + V_{IN} \times Q_{RR} \times f_{MIN}$$
$$P_{HSF} = 6\,m\Omega \times 14.7\,A^2 + \frac{5 \times 28.6\,A \times 50\,nC \times 183\,kHz}{2 \times 1\,A} + 5\,V \times 100\,nC \times 183\,kHz = 2.04\,W \quad (24)$$

where the second term represents the turn-off loss of the MOSFET and the third term represents the turn-on loss due to the stored charge in the body diode of the low-side MOSFET. In the second term, Q_G is the gate charge to be removed from the gate for turnoff and I_G is the gate turn-off current. From the data sheet, the value of Q_G for the FDB7045L is 50 nC and the peak gate drive current provided by the ADP3170 is about 1 A. In the third term, Q_{RR} is the charge stored in the body diode of the low-side MOSFET at the valley of the inductor current. The data sheet of the FDB7045L does not give that information, so an estimated value of 100 nC is used. The estimate is based on information found on the data sheets of similar devices.

The low-side MOSFET dissipation is:

$$P_{LSF} = R_{DS(ON)HSF} \times I_{HSF(MAX)}^2$$
$$P_{LSF} = 6\,m\Omega \times 18\,A^2 = 1.94\,W \quad (25)$$

Note that there are no switching losses in the low-side MOSFET.

Surface mount MOSFETs are preferred in CPU core converter applications due to their ability to be handled by automatic assembly equipment. The TO-263 package offers the power handling of a TO-220 in a surface mount package. However, this package still needs adequate copper area on the PCB to help move the heat away from the package.

The junction temperature for a given area of two-ounce copper can be approximated using:

$$T_J = \left(\theta_{JA} \times P_D\right) + T_A \quad (26)$$

assuming:

θ_{JA} = 45°C/W for 0.5 in^2

θ_{JA} = 36°C/W for 1 in^2

θ_{JA} = 28°C/W for 2 in^2

For 1 in^2 of copper area attached to each transistor and an ambient temperature of 50°C:

$$T_{JHSF} = \left(28^\circ C / W \times 2.06W\right) + 50^\circ C = 108^\circ C$$
$$T_{JLSF} = \left(28^\circ C / W \times 1.94W\right) + 50^\circ C = 104^\circ C$$

All of the above-calculated junction temperatures are safely below the 175°C maximum specified junction temperature of the selected MOSFETs.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is a square wave with a duty ratio of V_{OUT}/V_{IN} and an amplitude of one-half of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{C(RMS)} = I_O \sqrt{D_{HSF} - D_{HSF}^{\ 2}}$$
$$I_{C(RMS)} = 23A \times \sqrt{0.4 - 0.4^2} = 11.3A \quad (27)$$

For a ZA-type capacitor with 1000 µF capacitance and 6.3 V voltage rating, the ESR is 24 mΩ and the maximum allowable ripple current at 100 kHz is 2 A. At 105°C, at least six such capacitors must be connected in parallel to handle the calculated ripple current. At 50°C ambient, however, a higher ripple current can be tolerated, so five capacitors in parallel are adequate.

The ripple voltage across the five paralleled capacitors is:

$$V_{C(RIPPLE)} = I_O \times \left(\frac{ESR_C}{n_C} + \frac{D_{HSF(MAX)}}{n_C \times C_{IN} \times f_{MIN}} \right)$$
$$V_{C(RIPPLE)} = 23\ A \times \left(\frac{24\ m\Omega}{5} \times \frac{0.4}{5 \times 1\ mF \times 183\ kHz} \right) = 120\ mV \quad (28)$$

To further reduce the effect of the ripple voltage on the system supply voltage bus and to reduce the input-current di/dt to below the recommended maximum of 0.1 A/ms, an additional small inductor (L > 1 µH @ 10 A) should be inserted between the converter and the supply bus.

Linear Regulators

The linear regulator provides a low cost, convenient and versatile solution for generating a 1.8 V supply rail. The maximum output load current is determined by the size and thermal impedance of the external N-channel power MOSFET that is placed in series with the supply and controlled by the ADP3170. The output voltage is sensed at the LRFB pin and compared to an internal reference voltage in a negative feedback loop which keeps the output voltage in regulation. If the load is reduced or increased, the MOSFET drive will also be reduced or increased by the ADP3170 to provide a well regulated output voltage. Output voltages higher than the fixed internal reference voltage can be programmed by adding an external resistor divider.

Efficiency of the Linear Regulators

The efficiency and corresponding power dissipation of each of the linear regulators are not determined by the ADP3170. Rather, these are a function of input and output voltage and load current. Efficiency is approximated by the formula:

$$\eta = 100\% \times \frac{V_{OUT}}{V_{IN}} \quad (29)$$

The corresponding power dissipation in the MOSFET, together with any resistance added in series from input to output is given by:

$$P_{LDO} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (30)$$

Minimum power dissipation and maximum efficiency are accomplished by choosing the lowest available input voltage that exceeds the desired output voltage. However, if the chosen input source is itself generated by a linear regulator, its power dissipation will be increased in proportion to the additional current it must now provide.

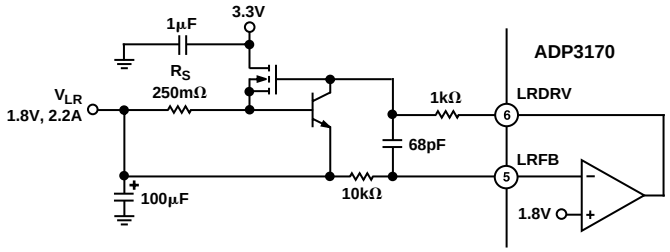


Figure 4. Adding Overcurrent Protection to the Linear Regulator

Implementing Current Limit for the Linear Regulators

The circuit of Figure 4 gives an example of a current limit protection circuit that can be used in conjunction with the linear regulator. The output voltage is internally set by the LRFB pin. The value of the current sense resistor may be calculated as follows:

$$R_S \cong \frac{540m\,V}{I_{O(MAX)}} = \frac{540m\,V}{2.2A} = 250\ m\Omega \quad (31)$$

The power rating of the current sense resistor must be at least:

$$P_{D(R_S)} = R_S \times I_{O(MAX)}^{\ 2} = 1.2\ W \quad (32)$$

The maximum linear regulator MOSFET junction temperature with a shorted output is:

$$T_{J(MAX)} = T_A + (\theta_{JC} \times V_{IN} \times I_{O(MAX)})$$
$$T_{J(MAX)} = 50^\circ C + (1.4^\circ C / W \times 3.3\,V \times 2.2A) = 60^\circ C \quad (33)$$

which is within the maximum allowed by the MOSFET's data sheet specification. The maximum MOSFET junction temperature at nominal output is:

$$T_{J(NOM)} = 50^\circ C + (\theta_{JC} \times [V_{IN} - V_{OUT}] \times I_{O(NOM)}) \quad (34)$$
$$T_{J(NOM)} = 50^\circ C + (1.4^\circ C / W \times [3.3\,V - 1.8\,V] \times 2\ A) = 54^\circ C$$

This example assumes an infinite heat sink. The practical limitation will be based on the actual heat sink used.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system:

General Recommendations

1. For best results, a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the voltage and current sense lines of the ADP3170) must cross through power circuitry, it is best if a ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
4. The GND pin of the ADP3170 should connect first to a ceramic bypass capacitor (on the VCC pin) and then into the analog ground plane. The analog ground plane should be located below the ADP3170 and the surrounding small-signal components, such as, the timing capacitor and compensation network. The analog ground plane should connect to power ground plane at a single point; the best location being the negative terminal of the last output capacitor.
5. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors too should be distributed, and generally in proportion to where the load tends to be more dynamic. It is advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
6. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

7. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system, as well as, noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs and the power Schottky diode, if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing; and it accommodates the high current demand with minimal voltage loss.
8. A power Schottky diode (1 ~ 2 A dc rating) placed from the lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body-drain diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body-drain diode prevents the drain voltage from being pulled high quickly. The upper MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time.
9. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias (if it is a current path); and improved thermal performance—especially if the vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
10. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
11. For best EMI containment, the ground plane should extend fully under all the power components. These are: the input capacitors, the power MOSFETs and Schottky diode, the inductor, the current sense resistor, any snubbing elements that might be added to dampen ringing and the output capacitors.

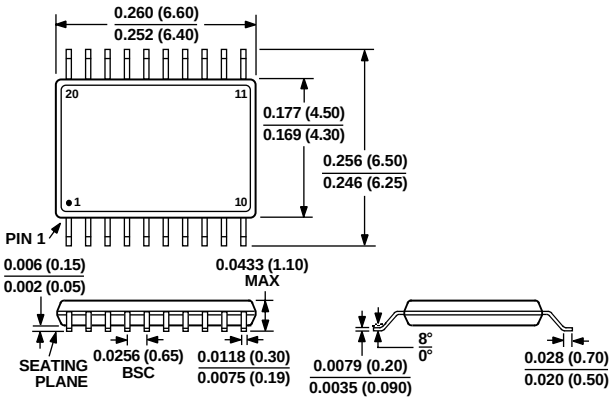
Signal Circuitry

12. The output voltage is sensed and regulated between the GND pin (which connects to the signal ground plane) and the CS– pin. The output current is sensed (as a voltage) and regulated between the CS– pin and the CS+ pin. In order to avoid differential mode noise pickup in those sensed signals, their loop areas should be small. Thus the CS– trace should be routed atop the signal ground plane, and the CS+ and CS– traces should be routed as a closely coupled pair (CS+ should be over the signal ground plane as well).
13. The CS+ and CS– traces should be Kelvin connected to the current sense resistor so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections does not affect the sensed voltage. It is desirable to have the ADP3170 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the GND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead TSSOP
(RU-20)



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