

FEATURES

- 12-bit resolution
- 5MHz minimum sampling rate
- Functionally complete
- Small 24-pin DDIP
- Requires only $\pm 5V$ supplies
- Low-power, 1.3 Watts
- Outstanding dynamic performance
- No missing codes over full military temperature range
- Edge-triggered, no pipeline delay
- Ideal for both time and frequency-domain applications



GENERAL DESCRIPTION

DATEL's ADS-118 and ADS-118A are 12-bit, 5MHz, sampling A/D converters packaged in space-saving 24-pin DDIP's. The ADS-118 offers an input range of $\pm 1V$ and has three-state outputs. The ADS-118A has an input range of $\pm 1.25V$ and features direct adjustment of offset error.

These functionally complete low-power devices (1.3 Watts) contain an internal fast-settling sample/hold amplifier, a 12-bit subranging A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. All timing and control logic operates from the rising edge of a single start convert pulse. Digital input and output levels are TTL. Models are available for use in either commercial (0 to $+70^{\circ}C$) or military (-55 to $+125^{\circ}C$) operating temperature ranges.

Applications include radar, transient signal analysis, process control, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|--------------|-----|--------------------|
| 1 | BIT 12 (LSB) | 24 | NO CONNECTION |
| 2 | BIT 11 | 23 | ANALOG GROUND |
| 3 | BIT 10 | 22 | NO CONNECTION |
| 4 | BIT 9 | 21 | +5V ANALOG SUPPLY |
| 5 | BIT 8 | 20 | -5V SUPPLY |
| 6 | BIT 7 | 19 | ANALOG INPUT |
| 7 | BIT 6 | 18 | ANALOG GROUND |
| 8 | BIT 5 | 17* | ENABLE/OFFSET ADJ. |
| 9 | BIT 4 | 16 | START CONVERT |
| 10 | BIT 3 | 15 | \overline{EOC} |
| 11 | BIT 2 | 14 | DIGITAL GROUND |
| 12 | BIT 1 (MSB) | 13 | +5V DIGITAL SUPPLY |

* ADS-118, Pin 17 is ENABLE
ADS-118A, Pin 17 is OFFSET ADJUST

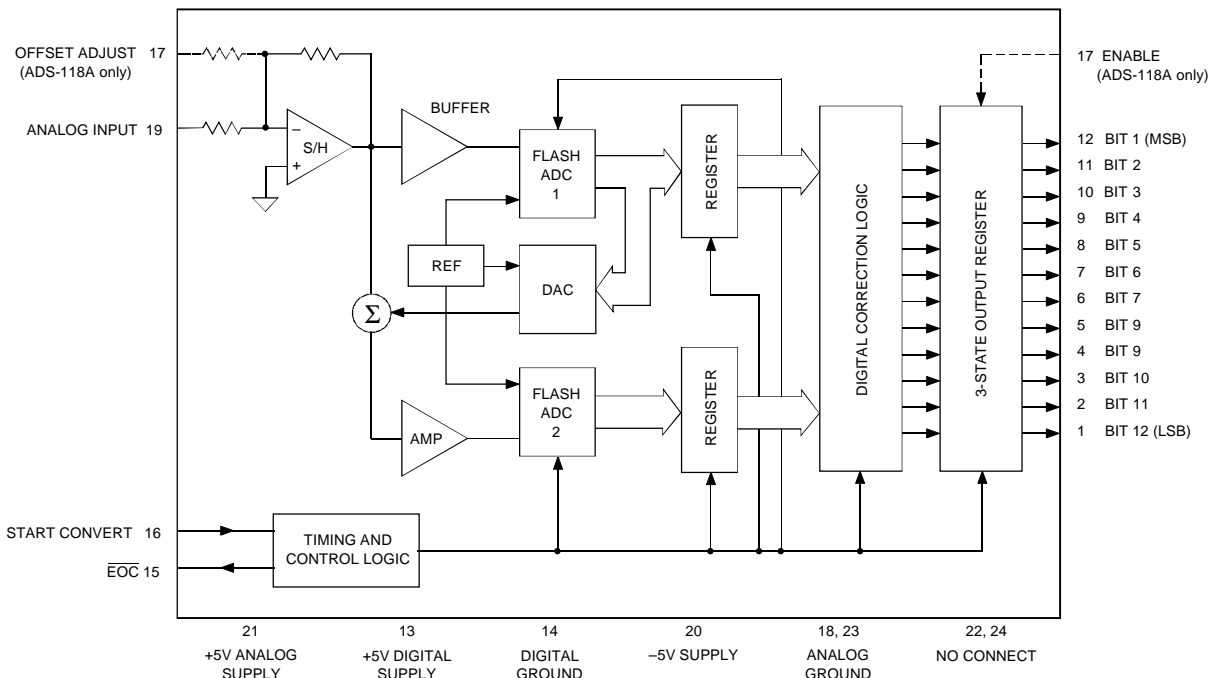


Figure 1. ADS-118/118A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
|-------------------------------|-------------------|-------|
| +5V Supply (Pins 13, 21) | 0 to +6 | Volts |
| -5V Supply (Pin 20) | 0 to -6 | Volts |
| Digital Input (Pin 16, 17) | -0.3 to +VDD +0.3 | Volts |
| Analog Input (Pin 19) | ±5 | Volts |
| Lead Temperature (10 seconds) | +300 | °C |

PHYSICAL/ENVIRONMENTAL

| PARAMETERS | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|---|------|------|---------|
| Operating Temp. Range, Case | 0 | — | +70 | °C |
| | -55 | — | +125 | °C |
| ADS-118/118AMC | | | | |
| ADS-118/118AMM, GM, 883 | | | | |
| Thermal Impedance | — | 2 | — | °C/Watt |
| | — | 23 | — | °C/Watt |
| | — | — | — | °C |
| Storage Temperature Range | -65 | — | +150 | °C |
| Package Type | 24-pin, metal-sealed, ceramic DDIP or SMT | | | |
| Weight | 0.42 ounces (12 grams) | | | |

FUNCTIONAL SPECIFICATIONS

(TA = +25°C, ±VDD = ±5V, 5MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

| ANALOG INPUT | +25°C | | | 0 to +70°C | | | -55 to +125°C | | | UNITS |
|--|-------|-------|-------|------------|------|-------|---------------|-------|-------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Input Voltage Range, ADS-118 ② | — | ±1 | — | — | ±1 | — | — | ±1 | — | Volts |
| Input Resistance | 475 | 500 | — | 475 | 500 | — | 475 | 500 | — | Ω |
| Input Capacitance | — | 6 | 15 | — | 6 | 15 | — | 6 | 15 | pF |
| DIGITAL INPUT | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.0 | — | — | +2.0 | — | — | +2.0 | — | — | Volts |
| Logic "0" | — | — | +0.8 | — | — | +0.8 | — | — | +0.8 | Volts |
| Logic Loading "1" | — | — | +20 | — | — | +20 | — | — | +20 | µA |
| Logic Loading "0" | — | — | -20 | — | — | -20 | — | — | -20 | µA |
| Start Convert Positive Pulse Width ③ | 50 | 100 | — | 50 | 100 | — | 50 | 100 | — | ns |
| STATIC PERFORMANCE | | | | | | | | | | |
| Resolution | — | 12 | — | — | 12 | — | — | 12 | — | Bits |
| Integral Nonlinearity (fin = 10kHz) | — | ±0.75 | — | — | ±1.0 | — | — | ±1.5 | — | LSB |
| Differential Nonlinearity (fin = 10kHz) | — | ±0.5 | +0.75 | — | ±0.5 | ±0.95 | — | ±0.75 | +0.95 | LSB |
| Full Scale Absolute Accuracy | — | ±0.1 | ±0.5 | — | ±0.5 | ±0.75 | — | ±0.75 | ±1.5 | %FSR |
| Bipolar Zero Error (Tech Note 2) | — | ±0.1 | ±0.5 | — | ±0.5 | ±0.85 | — | ±0.85 | ±2.0 | %FSR |
| Bipolar Offset Error (Tech Note 2) | — | ±0.1 | ±0.5 | — | ±0.5 | ±1.5 | — | ±1.5 | ±2.5 | %FSR |
| Gain Error (Tech Note 2) | — | ±0.1 | ±0.5 | — | ±0.5 | ±1.0 | — | ±1.0 | ±2.5 | % |
| No Missing Codes (fin = 10kHz) | 12 | — | — | 12 | — | — | 12 | — | — | Bits |
| DYNAMIC PERFORMANCE | | | | | | | | | | |
| Peak Harmonics (-0.5dB) | | | | | | | | | | |
| dc to 500kHz | — | -76 | -71 | — | -74 | -70 | — | -72 | -66 | dB |
| 500kHz to 1MHz | — | -75 | -71 | — | -74 | -70 | — | -70 | -65 | dB |
| 1MHz to 2.5MHz | — | -69 | -69 | — | -73 | -67 | — | -66 | -60 | dB |
| Total Harmonic Distortion (-0.5dB) | | | | | | | | | | |
| dc to 500kHz | — | -72 | -68 | — | -71 | -67 | — | -70 | -65 | dB |
| 500kHz to 1MHz | — | -71 | -67 | — | -70 | -66 | — | -67 | -63 | dB |
| 1MHz to 2.5MHz | — | -70 | -66 | — | -69 | -65 | — | -66 | -60 | dB |
| Signal-to-Noise Ratio | | | | | | | | | | |
| (w/o distortion, -0.5dB) | | | | | | | | | | |
| dc to 500kHz | 67 | 69 | — | 66 | 69 | — | 64 | 67 | — | dB |
| 500kHz to 1MHz | 66 | 69 | — | 65 | 68 | — | 63 | 66 | — | dB |
| 1MHz to 2.5MHz | 66 | 69 | — | 65 | 68 | — | 63 | 66 | — | dB |
| Signal-to-Noise Ratio ④ | | | | | | | | | | |
| (& distortion, -0.5dB) | | | | | | | | | | |
| dc to 500kHz | 65 | 68 | — | 64 | 67 | — | 62 | 66 | — | dB |
| 500kHz to 1MHz | 65 | 68 | — | 64 | 67 | — | 61 | 65 | — | dB |
| 1MHz to 2.5MHz | 64 | 67 | — | 63 | 66 | — | 60 | 64 | — | dB |
| Noise | — | 195 | — | — | 195 | — | — | 195 | — | µVrms |
| Two-tone Intermodulation | | | | | | | | | | |
| Distortion (fin = 1MHz, 975kHz, fs = 5MHz, -0.5dB) | — | -74 | — | — | -74 | — | — | -74 | — | dB |
| Input Bandwidth (-3dB) | | | | | | | | | | |
| Small Signal (-20dB input) | — | 20 | — | — | 20 | — | — | 20 | — | MHz |
| Large Signal (-0.5dB input) | — | 10 | — | — | 10 | — | — | 10 | — | MHz |
| Feedthrough Rejection (fin = 2.5MHz) | — | 80 | — | — | 80 | — | — | 80 | — | dB |
| Slew Rate | — | ±400 | — | — | ±400 | — | — | ±400 | — | V/µs |
| Aperture Delay Time | — | +10 | — | — | +10 | — | — | +10 | — | ns |
| Aperture Uncertainty | — | 3 | — | — | 3 | — | — | 3 | — | ps rms |

| DYNAMIC PERFORMANCE (Cont.) | +25°C | | | 0 to +70°C | | | -55 to +125°C | | | UNITS |
|---|---------------|------|-------|------------|------|--|---------------|------|-------|---------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| S/H Acquisition Time (to ±0.001%FSR, 10V step) | — | 85 | 90 | — | 85 | 90 | — | 85 | 90 | ns |
| Overshoot Recovery Time ⑤ | — | 200 | — | — | 200 | — | — | 200 | — | ns |
| A/D Conversion Rate | 5 | — | — | 5 | — | — | 5 | — | — | MHz |
| DIGITAL OUTPUTS | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.4 | — | — | +2.4 | — | — | +2.4 | — | — | Volts |
| Logic "0" | — | — | +0.4 | — | — | +0.4 | — | — | +0.4 | Volts |
| Logic Loading "1" | — | — | -4 | — | — | -4 | — | — | -4 | mA |
| Logic Loading "0" | — | — | +4 | — | — | +4 | — | — | +4 | mA |
| Delay, Falling Edge of \overline{EOC} to Output Data Valid | — | — | 20 | — | — | 20 | — | — | 20 | MHz |
| Delay, Falling Edge of \overline{ENABLE} to Output Data Valid | — | — | 10 | — | — | 10 | — | — | 10 | MHz |
| Output Coding | Offset Binary | | | | | | | | | |
| POWER REQUIREMENTS | | | | | | | | | | |
| Power Supply Ranges ⑥ | | | | | | | | | | |
| +5V Supply | +4.75 | +5.0 | +5.25 | +4.75 | +5.0 | +5.25 | +4.9 | +5.0 | +5.25 | Volts |
| -5V Supply | -4.75 | -5.0 | -5.25 | -4.75 | -5.0 | -5.25 | -4.9 | -5.0 | -5.25 | Volts |
| Power Supply Currents | | | | | | | | | | |
| +5V Supply | — | +205 | +220 | — | +205 | +220 | — | +205 | +220 | mA |
| -5V Supply | — | -80 | -90 | — | -80 | -90 | — | -80 | -90 | mA |
| Power Dissipation | — | 1.3 | 1.5 | — | 1.3 | 1.5 | — | 1.3 | 1.5 | Watts |
| Power Supply Rejection | — | — | ±0.1 | — | — | ±0.1 | — | — | ±0.1 | %FSR/%V |
| Footnotes: | | | | | | | | | | |
| ① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time. | | | | | | ④ Effective bits is equal to: $(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}} \right]$ 6.02 | | | | |
| ② Input voltage ranges for ADS-118A is ±1.25V | | | | | | ⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range. | | | | |
| ③ A 100ns wide start convert pulse is used for all production testing. For applications requiring less than an 5MHz sampling rate, wider start convert pulses can be used. NOTE: The device only requires the rising edge of a start convert pulse to operate. | | | | | | ⑥ The minimum supply voltages of +4.9V and -4.9V for ±V _{DD} are required for -55°C operation only. The minimum limits are +4.75V and -4.75V when operating at +125°C | | | | |

TECHNICAL NOTES

- Obtaining fully specified performance from the ADS-118 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 18, and 23) directly to a large **analog** ground plane beneath the package.

Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.
- The ADS-118 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using

- the adjustment circuitry shown in Figures 2a and 2b. When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.
- To enable the three-state outputs, connect \overline{ENABLE} (pin 17) to a logic "0" (low). To disable, connect pin 17 to logic "1" (high). The three-state outputs are permanently enabled in the ADS-118A.
- Applying a start convert pulse while a conversion is in progress (EOC = logic "1") will initiate a new and inaccurate conversion cycle.

CALIBRATION PROCEDURE

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figures 2a and 2b are guaranteed to compensate for the ADS-118's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting

LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-118, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is $\pm\frac{1}{2}$ LSB ($\pm 244\mu\text{V}$ for ADS-118; $\pm 305\mu\text{V}$ for ADS-118A).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus $\frac{1}{2}$ LSB's ($+0.99927\text{V}$ for ADS-118; $+1.249085\text{V}$ for ADS-118A).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting.
2. Apply $\pm 244\mu\text{V}$ (ADS-118) or $\pm 305\mu\text{V}$ (ADS-118A) to the ANALOG INPUT (pin 19).

3. Adjust the offset potentiometer until the output bits are 1000 0000 0000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply $+0.99927\text{V}$ (ADS-118) or $+1.249085\text{V}$ (ADS-118A) to the ANALOG INPUT (pin 19).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 1.

Table 1. Output Coding for Bipolar Operation

| BIPOLAR SCALE | ADS-118 INPUT RANGE ($\pm 1\text{V}$) | OUTPUT CODING | | ADS-118A INPUT RANGE ($\pm 1.25\text{V}$) |
|---------------|---|---------------|------------|---|
| | | OFFSET MSB | BINARY LSB | |
| +FS -1 LSB | +0.99951V | 1111 | 1111 1111 | +1.2494V |
| +3/4 FS | +0.75000V | 1110 | 0000 0000 | +0.9375V |
| +1/2 FS | +0.50000V | 1100 | 0000 0000 | +0.6250V |
| 0 | 0.00000V | 1000 | 0000 0000 | 0.0000V |
| -1/2 FS | -0.50000V | 0100 | 0000 0000 | -0.6250V |
| -3/4 FS | -0.75000V | 0010 | 0000 0000 | -0.9375V |
| -FS +1 LSB | -0.99951V | 0000 | 0000 0001 | -1.2494V |
| -FS | -1.00000V | 0000 | 0000 0000 | -1.2500V |

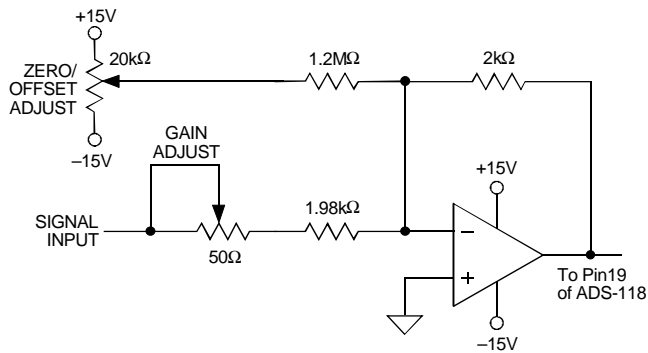


Figure 2a. Optional ADS-118 External Gain and Offset Adjust Circuits

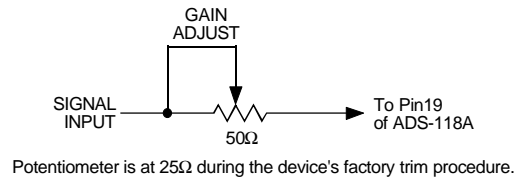
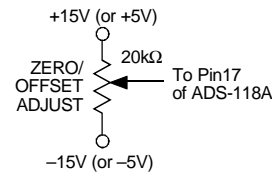
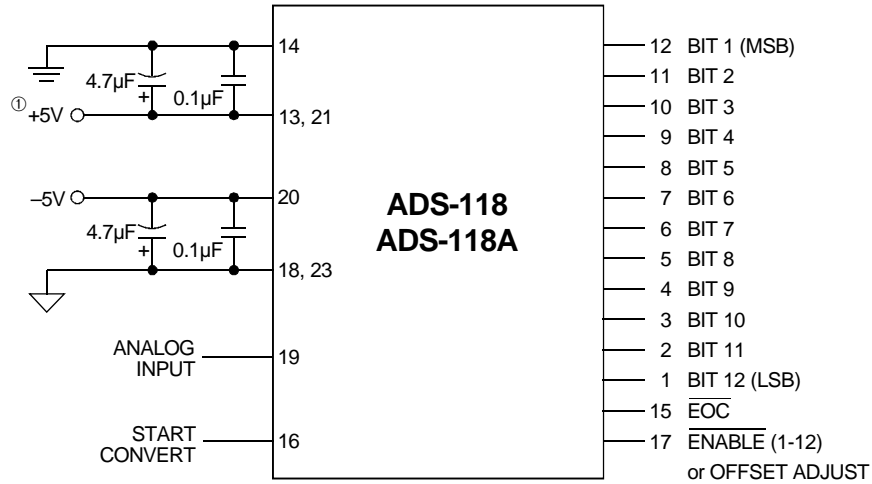


Figure 2b. Optional ADS-118A Gain and Offset Adjust Circuits





① A single +5V supply should be used for both the +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 3. Typical Connection Diagram

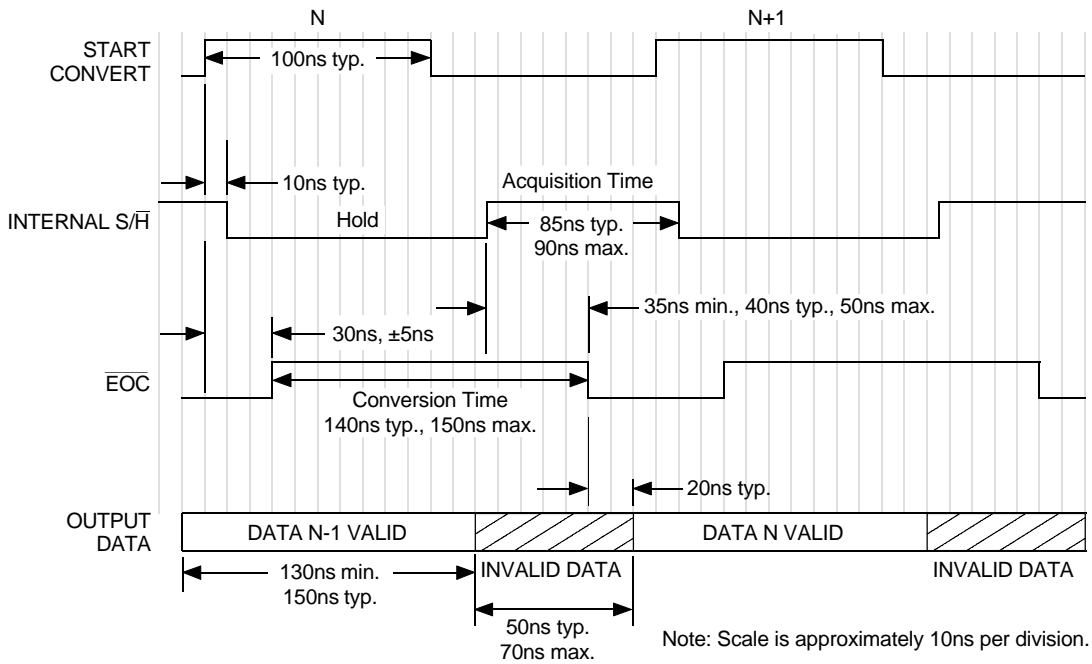


Figure 4. ADS-118/118A Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and -55 to +125°C. All room temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than socketed, and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

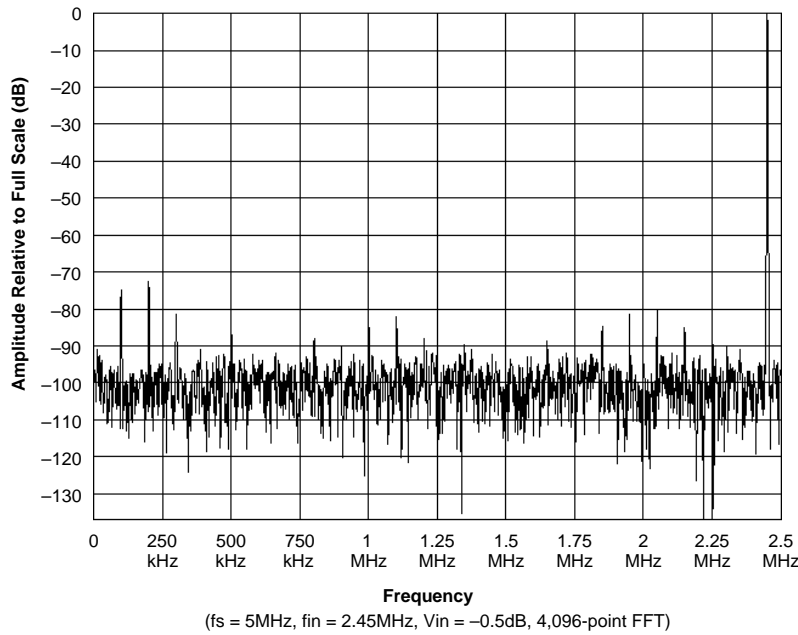


Figure 5. FFT Analysis of ADS-118

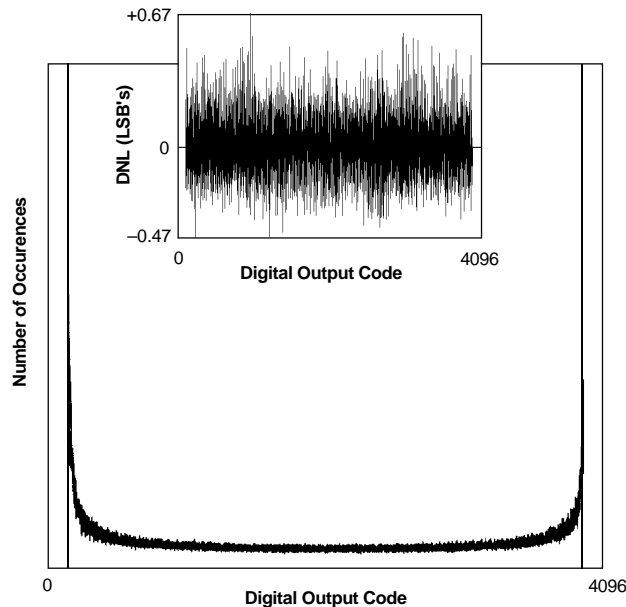


Figure 6. ADS-118 Histogram and Differential Nonlinearity

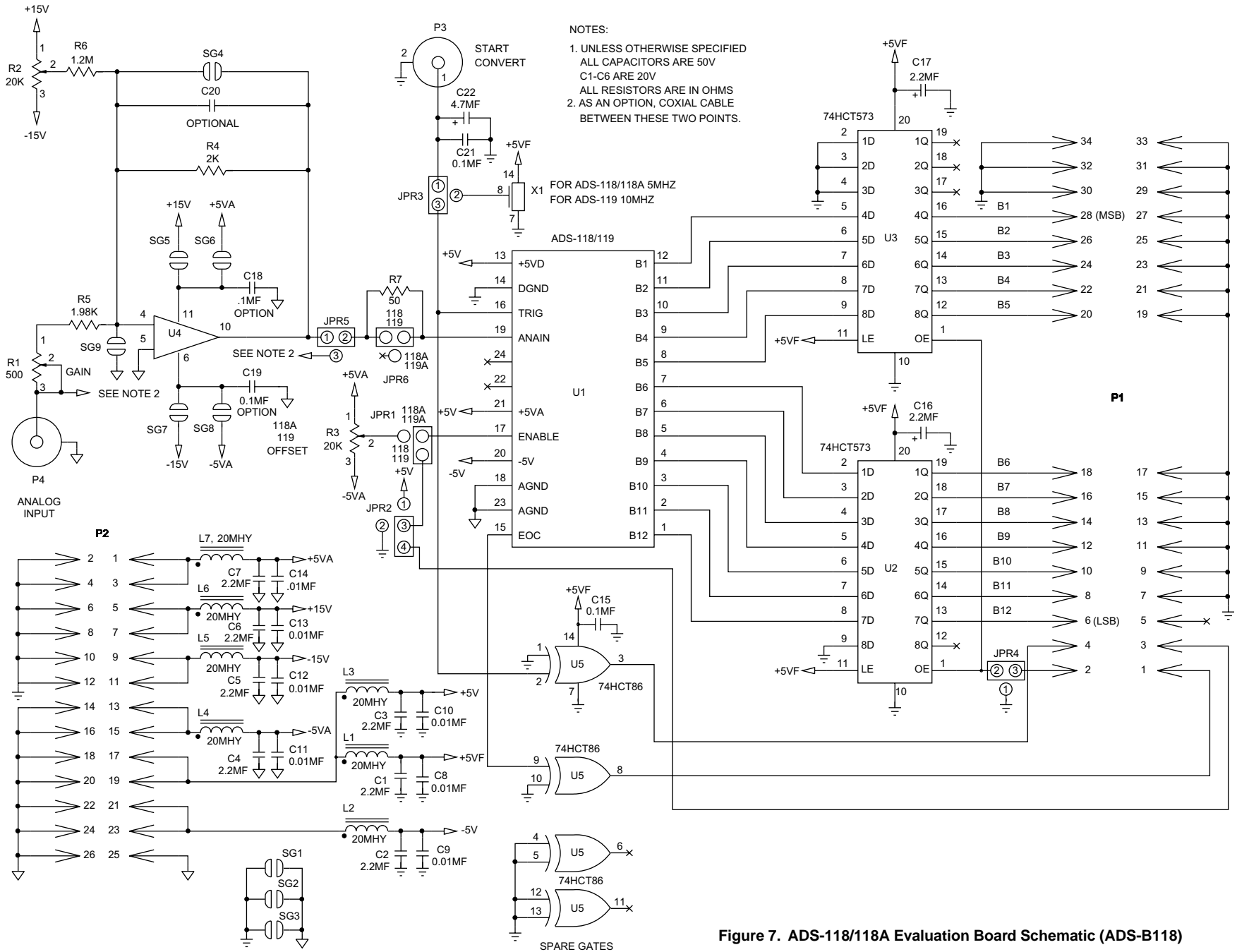
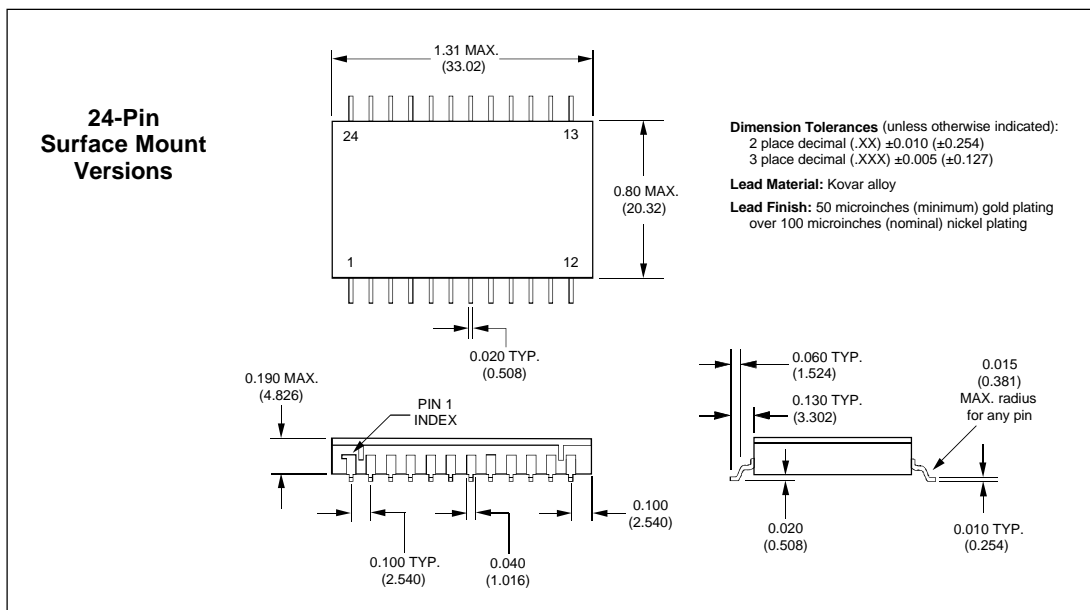
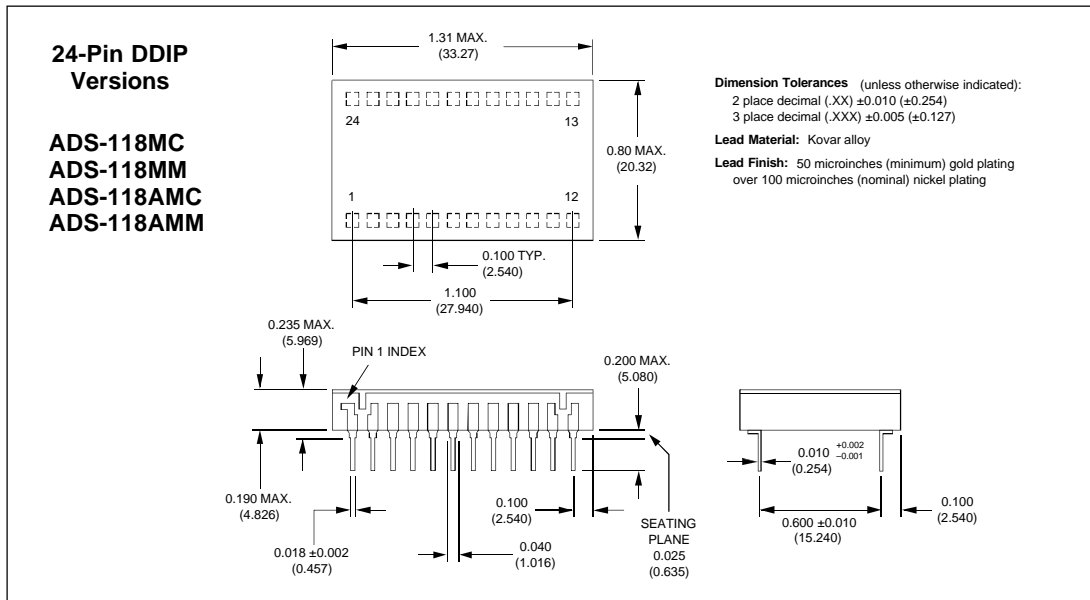


Figure 7. ADS-118/118A Evaluation Board Schematic (ADS-B118)

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

| MODEL NUMBER | OPERATING TEMP. RANGE | 24-PIN PACKAGE | ACCESSORIES |
|--------------|-----------------------|----------------|---|
| ADS-118MC | 0 to +70°C | DDIP | ADS-B118 Evaluation Board (without ADS-118) |
| ADS-118MM | -55 to +125°C | DDIP | HS-24 Heat Sink for all ADS-118 DDIP models |
| ADS-118AMC | 0 to +70°C | SMT | |
| ADS-118AMM | -55 to +125°C | SMT | |

Receptacles for PC board mounting can be ordered through AMP, Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product, or surface mount packaging, contact DATEL.