## FEATURES

- 20MHz sampling rate
- Low Power, 100 mW , max
- 100 MHz full power input bandwidth
- Integral sample-and-hold
- Single +3 V supply operation
- TTL compatible digital output
- Offset binary output coding


## GENERAL DESCRIPTION

The ADS-238Q is a monolithic, 12 -bit, 20 MHz , sampling analog-to-digital converter fabricated in a CMOS process. The converter is designed for applications where high speed, wide bandwidth and low power dissipation are essential. These characteristics are provided through the use of a fully differential pipeline A/D architecture with digital error correction logic for the eleven most significant bits.
The ADS-238Q offers excellent dynamic performance while consuming only 79 mW , typical. The power dissipation is approximately proportional to the sampling rate, thus the ADS-238Q is ideal for low power applications between 1 and 20 MHz . With low distortion and high dynamic range, this device provides the performance required for imaging, telecommunications, multimedia, and instrumentation applications.
The ADS-238Q is available in a 44 -pin (plastic) TQFP package and operates over the commercial $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ temperature range.

## INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
| :---: | :--- | :---: | :--- |
| 1 | GND | 44 | Vs |
| 2 | CLK | 43 | BIT 12 (LSB) |
| 3 | N.C. | 42 | BIT 11 |
| 4 | Vs | 41 | BIT 10 |
| 5 | Vs | 40 | BIT 9 |
| 6 | Vs | 39 | BIT 8 |
| 7 | Vs | 38 | BIT 7 |
| 8 | Vs | 37 | BIT 6 |
| 9 | Vs | 36 | BIT 5 |
| 10 | VREF- | 35 | BIT 4 |
| 11 | VREF+ | 34 | BIT 3 |
| 12 | N.C. | 33 | BIT 2 |
| 13 | N.C. | 32 | BIT 1 |
| 14 | N.C. | 31 | GND |
| 15 | GND | 30 | GND |
| 16 | BIAS1 | 29 | GND |
| 17 | BIAS2 | 28 | GND |
| 18 | VCM | 27 | GND |
| 19 | GND | 26 | GND |
| 20 | VIN+ | 25 | GND |
| 21 | VIN- | 24 | GND |
| 22 | GND | 23 | GND |

Note: Recommend that N.C. (no connect) pins be connected to analog ground.


Figure 1. ADS-238Q Functional Block Diagram

## ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
| :--- | :---: | :---: |
| Supply Voltage, Vs (Pins 4-9,44) <br> Input Voltages: | -0.5 to +6 | Volts |
| Analog Input, VIN+, Vin- |  |  |
| (Pin 20, 21) | -0.5 to (+Vs +0.5$)$ | Volts |
| VREF-, VREF+, (Pin 10, 11) | -0.5 to (+Vs +0.5$)$ | Volts |
| CLK, (Pin 2) | -0.5 to (+Vs +0.5$)$ | Volts $^{\circ}$ |
| Lead Temperature (10 seconds) | +300 | ${ }^{\circ} \mathrm{C}$ |

## FUNCTIONAL SPECIFICATIONS

(TA = Tmin to Tmax, Vs = 3.3V, Vref- = 1.15V, Vref+ $=2.15 \mathrm{~V}$, Vcm $=1.65 \mathrm{~V}$, CLK
Frequency $=20 \mathrm{MHz}, \mathrm{BIAS1}=90 \mu \mathrm{~A}, \mathrm{BIAS} 2=9.5 \mu \mathrm{~A}$, Duty Cycle $=50 \%$ and
Differential Input, unless otherwise specified.)


| DYNAMIC PERFORMANCE |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Differential Phase | - | 0.2 | - | Degrees |
| Differential Gain | - | 0.5 | - | \% |
| Aperature Uncertainty | - | 10 | - | ps rms |
| Aperture Delay Time, tAP | - | 5 | - | ns |
| Data Latency | - | 7.5 | - | Cycles |
| A/D Conversion Rate | 20 | - | - | MHz |
| DIGITAL OUTPUTS |  |  |  |  |
| Logic "1" | 80\% Vs | 95\% Vs | - | Volts |
| Logic "0" | - | 0.1 | 0.4 | Volts |
| CLK to Output Delay Time, to | 4 | 8 | 12 | ns |
| POWER REQUIREMENTS |  |  |  |  |
| Supply Voltages, VS | 2.8 | 3.3 | 3.6 | Volts |
| Supply Current, Is | - | 24 | 30 | mA |
| Power Dissipation | - | 79 | 100 | mW |
| Power Supply Rejection Ratio | - | 63 | - | dB |
| PHYSICAL/ENVIRONMENTAL |  |  |  |  |
| Operating Temp. Range, Case Storage Temperature Range Package Type Weight | 0 | - | +70 | ${ }^{\circ} \mathrm{C}$ |
|  | -65 | - | +125 | ${ }^{\circ} \mathrm{C}$ |
|  | 44-pin (leaded), plastic thin quad flat package0.2 grams |  |  |  |

## TECHNICAL NOTES

## Differential Analog Input

The analog input is a fully differential input that can be configured in various ways depending on whether a singleended or differential, AC or DC coupled input is required. An AC coupled input is most readily implemented using a transformer (1:1 with a center tap on the secondary winding) as illustrated in Figures 2, Typical Connection Diagram, and 3.1, Transformer Coupled Input. To minimize distortion, the core of the transformer must not saturate at full scale input voltage levels. To minimize kickback noise from the internal sample-hold a small capacitor should be connected across the Vin pins (pins 20 and 21).

Figure 3.2, DC Coupled Single Ended Input, illustrates a conversion circuit for a DC coupled single-ended input. Power supplies and by-pass capacitors are not shown.

## Reference Voltage Inputs

The ADS-238Q is designed to accept two external reference voltages at the Vref input pins, see Figure 2, Typical Connection Diagram. These reference voltages, applied to $\mathrm{V}_{\text {ref+ }}$ (pin 11) and $\mathrm{V}_{\text {ref- ( }}$ (pin 10), determine the analog input voltage range, which is equal to $\pm$ (Vref+ -Vref-). This voltage range will be symmetric about the common mode voltage, and for best performance should be symmetrical about the midpoint of the supply voltage.

In order to minimize overall converter noise it is recommended that the Vref pins be adequately bypassed using a $4.7 \mu \mathrm{~F}$ tantalum capacitor in parallel with a $0.01 \mu \mathrm{~F}$ ceramic capacitor. Locate the bypass capacitors as close to the unit as possible.


Figure 2. ADS-238QTypical Connection Diagram


Figure 3-1. ADS-238Q Transformer Coupled Input


Figure 3-2. ADS-238Q DC Coupled Single Ended Input

## Common Mode Voltage Reference

The ADS-238Q has an internal common mode reference voltage, $\mathrm{V}_{\text {cm }}$ (pin 18). This reference voltage is typically one half of the supply voltage and is capable of driving loads up to $20 \mu \mathrm{~A}$. This reference is used to drive the center tap in the transformer used in fully differential applications, or provide level shifting in single-ended to differential applications.

Table 1. Sample Rate Bias Current Settings

| SAMPLE RATE <br> $(\mathbf{M H z})$ | BIAS1 <br> $(\boldsymbol{\mu A})$ | BIAS2 <br> $(\boldsymbol{\mu A})$ |
| :---: | :---: | :---: |
| 1 | 20 | 3.5 |
| 5 | 50 | 6.5 |
| 10 | 80 | 8.0 |
| 20 | 90 | 9.5 |



Figure 4. Suggested Bias Current vrs Sample Rate


Figure 5. Bias Current Determination and Adjustment

## Bias Current Inputs

The bias currents shown in Table I, Sample Rate Bias Current Settings, and Figure 4, Suggested Bias Currents vrs Sample Rate, are designed to optimize performance of the ADS-238Q for a given sample rate.

Figure 5, Bias Current Determination and Adjustment, details the suggested circuits for measuring bias voltage drops to calculate the bias currents. Adjustments to the bias currents are made via the trim pots. The Bias1 voltage drop is measured across TP1A and TP1B. The Bias2 voltage drop is measured across TP2A and TP2B. Figures 6-1 and $6-2$ show the relationship between the bias currents and voltages when measured in the indicated circuit. The Bias1 and Bias2 pins should be by-passed with $0.01 \mu \mathrm{~F}$ capacitors.


Figure 6-1. Bias1 Voltage vrs Bias1 Current


Figure 6-2. Bias2 Voltage vrs Bias2 Current

## Clock

The ADS-238Q accepts a low voltage CMOS logic level at the clock input (CLK, pin 2). The clock duty cycle must be held to within $50 \%+/-3 \%$ because consecutive stages of the A-to-D are clocked in opposite phase. A duty cycle other than this will reduce the settling time available for every other stage, there by degrading dynamic performance.

For optimum performance at high input frequencies the clock must have low jitter, and rise/fall times less than 2ns. Over/undershoot should be avoided. Clock jitter causes the noise floor to increase proportional to the input frequency. To reduce crosstalk, and hence jitter, clock traces on the PC board should be kept as short as possible with transmission line practices employed.

## Digital Outputs

The digital output data is provided in offset binary format, at 3.3 V CMOS logic levels, and is available 7.5 clock cycles after the data is sampled. The output data is invalid for the first 20 clock cycles when the ADS-238Q is first powered up.

The clock to output delay is typically 8ns, but will change as a function of the supply voltage, Vs. Figure 7, Clock to Output Delay vrs Vs, shows this relationship.

A negative full scale input results in an all zeros output code (0000 00000000 ). A positive full scale input results in an all ones output code (1111 1111 1111).
The input is sampled during the high-to-low transition of the input clock. Output data should be latched during the low-to-high clock transition as shown in Figure 8, Timing Diagram.


Figure 7. Clock to Output Delay vrs Vs

## Power Supplies and Grounding

The ADS-238Q is powered from a single 3.3 V supply. The converters should be mounted on a board that provides separate low impedance paths for the analog and digital supplies and grounds. For best performance the 3.3 V supply should be clean, and linearly regulated. The power supply should be bypassed to ground with a $10 \mu \mathrm{~F}$ tantalum capacitor in parallel with a $0.01 \mu \mathrm{~F}$ ceramic capacitor. Locate the bypass capacitors as close to the converter as possible. Analog and digital grounds should be isolated with a ferrite bead. See the Typical Connection Diagram, Figure 2.


Figure 8. ADS-238Q Timing Diagram

TYPICAL PERFORMANCE CHARATERISTICS


Figure 9-1. THD, SNR, SINAD vrs Input Frequency


Figure 9-3. THD, SNR, SINAD vrs Temperature


Figure 9-2. THD, SNR, SINAD vrs Sample Rate


Figure 9-4. THD, SNR, SINAD vrs Clock Duty Cycle


Figure 9-5. Power Dissipation vrs Sample Rate

MECHANICAL DIMENSIONS INCHES (mm)


| Symbol | Inches |  | Millmeters |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Min. | Max. | Min. | Max. |
| A | 0.472 Typ. | -- | 12.00 Typ. | -- |
| B | 0.394 Typ. | -- | 10.00 Typ. | -- |
| C | 0.394 Typ. | -- | 10.00 Typ. | -- |
| D | 0.472 Typ. | -- | 12.00 Typ. | -- |
| E | 0.031 Typ. | --018 | 0.80 Typ. | -.300 |
| F | 0.012 | 0.0 | 0.45 |  |
| G | 0.053 | 0.057 | 1.35 | 1.45 |
| H | 0.002 | 0.006 | 0.05 | 0.15 |
| I | 0.018 | 0.030 | 0.450 | 0.750 |
| J | 0.039 Typ. | -- | 1.00 Typ. | -- |
| K | $0-70^{-}$ | -- | $0-7=$ | -- |

ORDERING INFORMATION

| MODEL | OPERATING TEMP. RANGE | PACKAGE |
| :--- | :--- | :--- |
| ADS-238Q | 0 to $+70^{\circ} \mathrm{C}$ | 44 -PIN PLASTIC TQFP |

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