BURR-BROWN®

ADS1252

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Resolution PLUS™ 24-Bit, 40kHz ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- 19 BITS EFFECTIVE RESOLUTION UP TO 40kHz DATA RATE
- LOW NOISE: 2.5ppm
- DIFFERENTIAL INPUTS
- INL: 0.0015% (max)
- EXTERNAL REFERENCE
- POWER-DOWN MODE
- SYNC MODE

APPLICATIONS

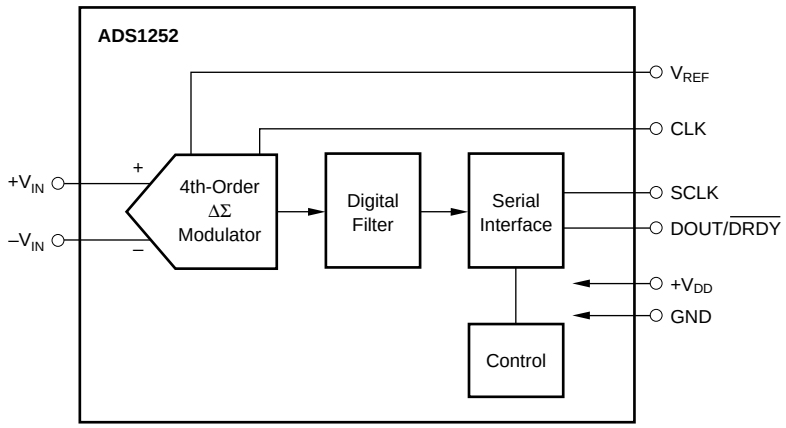
- CARDIAC DIAGNOSTICS
- DIRECT THERMOCOUPLE INTERFACE
- BLOOD ANALYSIS
- INFRARED PYROMETER
- LIQUID/GAS CHROMATOGRAPHY
- PRECISION PROCESS CONTROL

DESCRIPTION

The ADS1252 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution operating from a single +5V supply. The delta-sigma architecture is used for wide dynamic range and to guarantee 24 bits of no missing code performance. An effective resolution of 19 bits (2.5ppm of rms noise) is achieved for conversion rates up to 40kHz.

The ADS1252 is designed for high-resolution measurement applications in cardiac diagnostics, smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation. The converter includes a flexible, two-wire synchronous serial interface for low-cost isolation.

The ADS1252 is a single-channel converter and is offered in an SO-8 package.



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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

All specifications at T_{MIN} to T_{MAX}, V_{DD} = +5V, CLK = 16MHz, and V_{REF} = 4.096, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1252U MIN	ADS1252U TYP	ADS1252U MAX	UNITS
ANALOG INPUT					
Input Voltage Range(1)		0		$\pm V_{REF}$	V
Input Impedance (differential)	R = 6 ÷ (20pF • CLK)		19		kΩ
Input Capacitance			20		pF
Input Leakage	At +25°C		5	50	pA
	At T_{MIN} to T_{MAX}			1	nA
DYNAMIC CHARACTERISTICS					
Data Rate				41.7	kHz
Bandwidth	–3dB	9			kHz
Serial Clock (SCLK)				16	MHz
System Clock Input (CLK)				16	MHz
ACCURACY					
Integral Linearity Error(2)			±0.0004	±0.0015	% of FSR
THD	1kHz Input; 0.1dB below FS		97		dB
Noise			2.5	3.8	ppm of FSR, rms
Resolution			24		Bits
No Missing Codes			24		Bits
Common-Mode Rejection(3)	at DC	90	100		dB
Gain Error			0.4	1	% of FSR
Offset Error			±100	±200	ppm of FSR
Gain Sensitivity to V_{REF}	V_{REF} = 4.096V ±0.1V		1:1		
Power Supply Rejection Ratio		60	80		dB
PERFORMANCE OVER TEMPERATURE					
Offset Drift			0.07		ppm/°C
Gain Drift			13		ppm/°C
VOLTAGE REFERENCE					
V_{REF}			4.096		V
Load Current			200		µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Level: V_{IH}		+4.0		$+V_{DD}$ + 0.3	V
V_{IL}		–0.3		+0.8	V
V_{OH}	I_{OH} = –500µA	+4.5			V
V_{OL}	I_{OL} = 500µA			0.4	V
Input (SCLK, CLK) Histeresis			0.6		V
Data Format			Offset Two's Complement		
POWER SUPPLY REQUIREMENTS					
Operation		+4.75	+5	+5.25	VDC
Quiescent Current	V_{DD} = +5VDC		8	10	mA
Operating Power			40	50	mW
Power-Down Current			1	10	µA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential. If the input is single-ended ($+V_{IN}$ or $-V_{IN}$ is fixed), then the full scale range is one-half that of the differential range. (2) Applies to full-differential signals. (3) The common-mode rejection test is performed with a 100mV differential input.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	GND –0.3V to V_{DD} + 0.3V
V_{DD} to GND	–0.3V to 6V
V_{REF} Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation (any package)	500mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

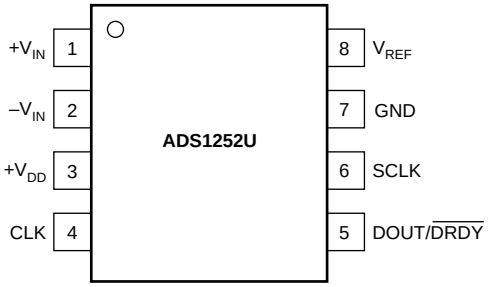
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
ADS1252U	SO-8	182	–40°C to +85°C	ADS1252U	ADS1252U	Rails
"	"	"	"	"	ADS1252U/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS1252U/2K5" will get a single 2500-piece Tape and Reel.

PIN CONFIGURATION

Top View **SO-8**



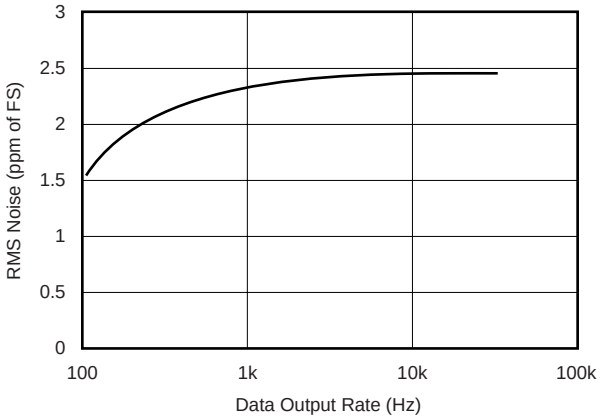
PIN DESCRIPTIONS

PIN	NAME	PIN DESCRIPTION
1	+V_{IN}	Analog Input: Positive Input of the Differential Analog Input.
2	–V_{IN}	Analog Input: Negative Input of the Differential Analog Input.
3	+V_{DD}	Input: Power Supply Voltage, +5V.
4	CLK	Digital Input: Device System Clock. The system clock is in the form of a CMOS-compatible clock. This is a Schmitt-Trigger input.
5	DOUT/$\overline{DRDY}$	Digital Output: Serial Data Output/Data Ready. A logic LOW on this output indicates that a new output word is available from the ADS1252 data output register. The serial data is clocked out of the serial data output shift register using SCLK.
6	SCLK	Digital Input: Serial Clock. The serial clock is in the form of a CMOS-compatible clock. The serial clock operates independently from the system clock, therefore, it is possible to run SCLK at a higher frequency than CLK. The normal state of SCLK is LOW. Holding SCLK HIGH will either initiate a modulator reset for synchronizing multiple converters or enter power-down mode. This is a Schmitt-Trigger input.
7	GND	Input: Ground.
8	V_{REF}	Analog Input: Reference Voltage Input.

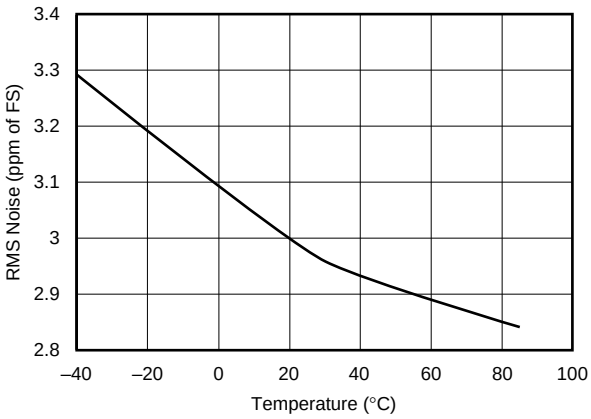
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{DD} = +5V, CLK = 14.7456MHz, and V_{REF} = 4.096, unless otherwise specified.

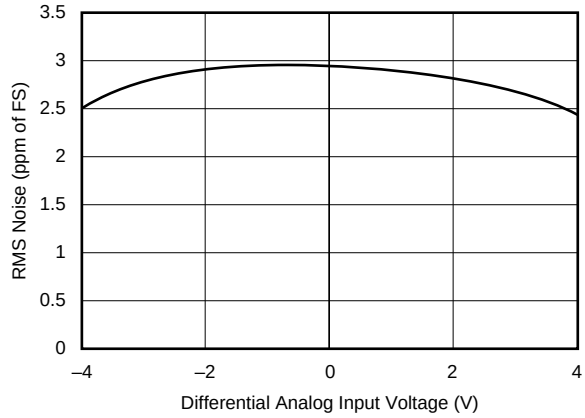
RMS NOISE vs DATA OUTPUT RATE



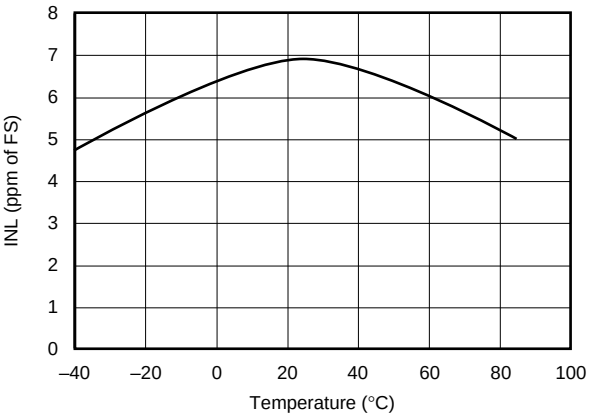
RMS NOISE vs TEMPERATURE



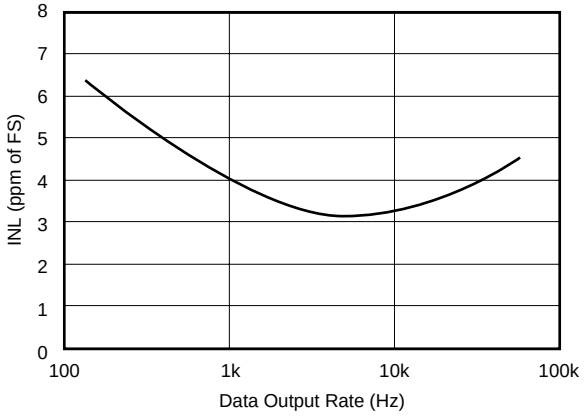
RMS NOISE vs INPUT VOLTAGE



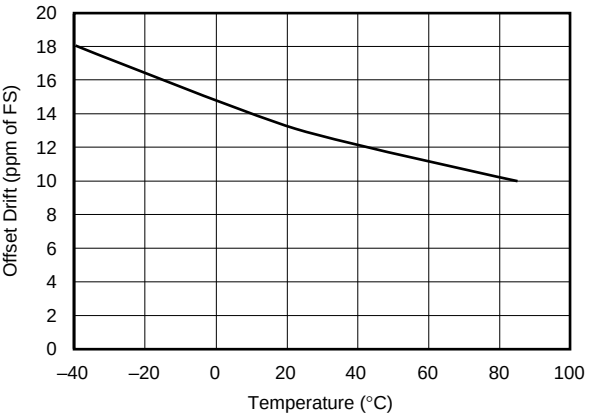
INTEGRAL NON-LINEARITY vs TEMPERATURE



INTEGRAL NON-LINEARITY vs DATA OUTPUT RATE



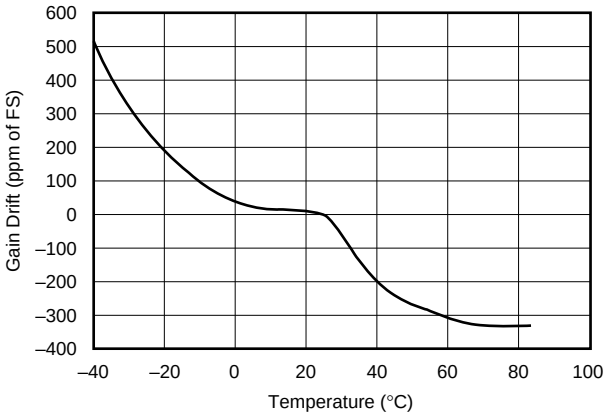
OFFSET DRIFT vs TEMPERATURE



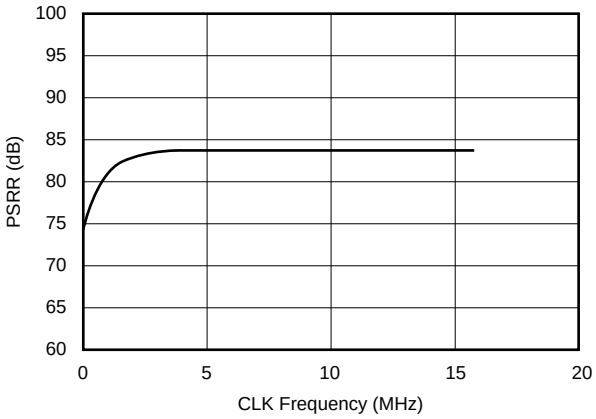
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{DD} = +5V, CLK = 14.7456MHz, and V_{REF} = 4.096, unless otherwise specified.

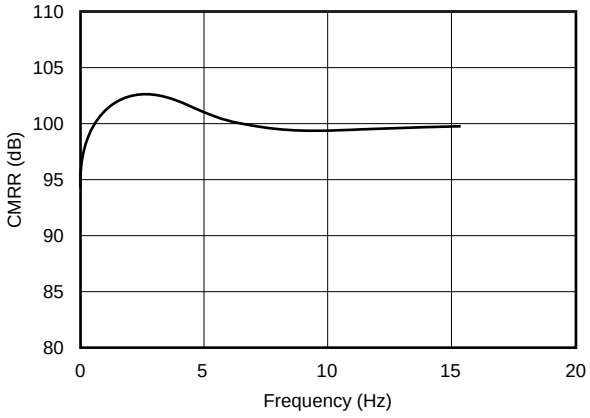
GAIN DRIFT vs TEMPERATURE



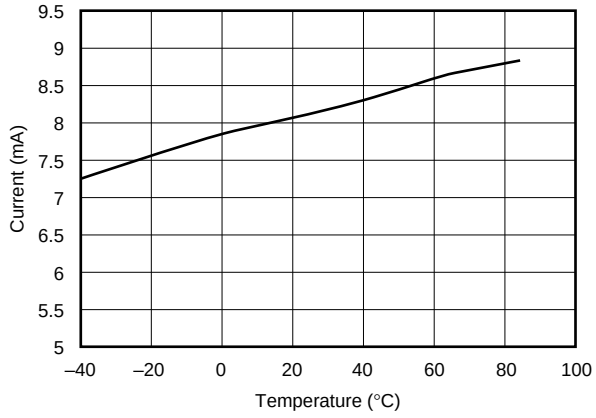
POWER SUPPLY REJECTION RATIO vs TEMPERATURE



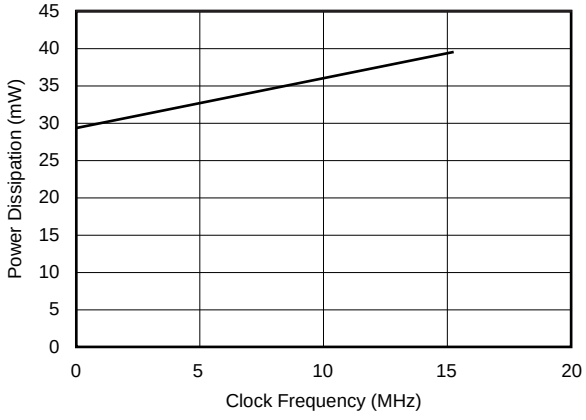
COMMON-MODE REJECTION RATIO vs FREQUENCY



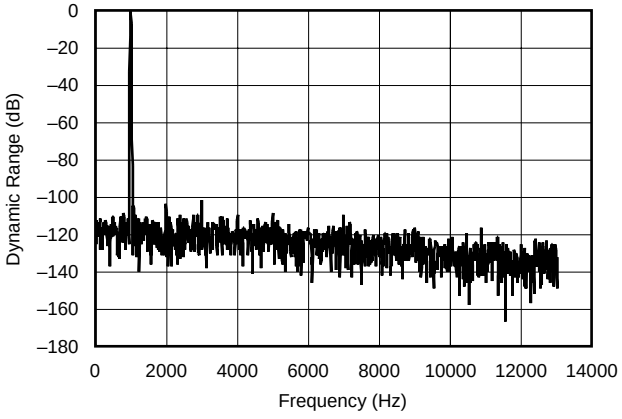
CURRENT vs FREQUENCY



POWER DISSIPATION vs CLOCK FREQUENCY



TYPICAL FFT ANALYSIS OF THE 1kHz f_S INPUT SIGNAL



THEORY OF OPERATION

The ADS1252 is a precision, high dynamic range, 24-bit, delta-sigma, A/D converter capable of achieving very high-resolution digital results at high data rates. The analog input signal is sampled at a rate determined by the frequency of the system clock (CLK). The sampled analog input is modulated by the delta-sigma A/D modulator. This is followed by a digital filter. A $sinc^5$ digital low-pass filter processes the output of the delta-sigma modulator and writes the result into the data output register. The DOUT/$\overline{DRDY}$ pin is pulled LOW indicating that new data is available to be read by the external microcontroller/microprocessor. As shown in the block diagram, the main functional blocks of the ADS1252 are the fourth-order delta-sigma modulator, a digital filter, control logic, and a serial interface. Each of these functional blocks is described below.

ANALOG INPUT

The ADS1252 contains a fully differential analog input. In order to provide low system noise, common-mode rejection of 100dB, and excellent power supply rejection, the design topology is based on a fully differential switched-capacitor architecture. The bipolar input voltage range is from –4.096 to +4.096V when the reference input voltage equals +4.096V. The bipolar range is with respect to $-V_{IN}$ and not with respect to GND.

Figure 1 shows the basic input structure of the ADS1252. The impedance is directly related to the sampling frequency of the input capacitor which is set by the CLK rate. Higher CLK rates result in lower impedance and lower CLK rates result in higher impedance.

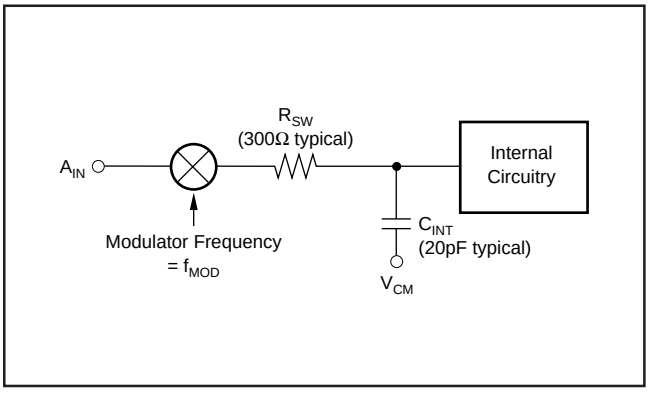


FIGURE 1. Analog Input Structure.

The input impedance of the analog input changes with ADS1252 system clock frequency (CLK). The relationship is:

$$A_{IN} \text{ Impedance } (\Omega) = (16\text{MHz/CLK}) \bullet 19{,}000$$

With regard to the analog input signal, the overall analog performance of the device is affected by three items. First, the input impedance can affect accuracy. If the source impedance of the input signal is significant, or if there is passive filtering prior to the ADS1252, a significant portion of the signal can be lost across this external impedance. The magnitude of the effect is dependent on the desired system performance.

Second, the current into or out of the analog inputs must be limited. Under no conditions should the current into or out of the analog inputs exceed 10mA.

Third, to prevent aliasing of the input signal, the bandwidth of the analog input signal must be band limited. The bandwidth is a function of the system clock frequency. With a system clock frequency of 16MHz, the data output rate is 41.667kHz, with a –3dB frequency of 9kHz. The –3dB frequency scales with the system clock frequency.

To guarantee the best linearity of the ADS1252, a fully differential signal is recommended.

DELTA-SIGMA MODULATOR

The ADS1252 operates from a nominal system clock frequency of 16MHz. The modulator frequency is fixed in relation to the system clock frequency. The system clock frequency is divided by 6 to derive the modulator frequency. Therefore, with a system clock frequency of 16MHz, the modulator frequency is 2.667MHz. Furthermore, the oversampling ratio of the modulator is fixed in relation to the modulator frequency. The oversampling ratio of the modulator is 64, and with the modulator frequency running at 2.667MHz, the data rate is 41.667kHz. Using a slower system clock frequency will result in a lower data output rate, as shown in Table I.

CLK (MHz)	DATA OUTPUT RATE (Hz)
16.000(1)	41.667
15.360(1)	40,000
15.000(1)	30,063
14.745600(1)	38,400
14.318180(1)	37,287
12.288000(1)	32,000
12.000000(1)	31,250
11.059220(1)	28,800
10.000000(1)	26,042
9.600000	25,000
7.372800(1)	19,200
6.144000(1)	16,000
6.000000(1)	15,625
4.915200(1)	12,800
3.686400(1)	9,600
3.072000(1)	8,000
2.457600(1)	6,400
1.843200(1)	4,800
0.921600	2,400
0.460800	1,200
0.384000	1,000
0.192000	500
0.038400	100
0.023040	60
0.019200	50
0.011520	30
0.009600	25
0.007680	20
0.006400	16.67
0.005760	15
0.004800	12.50
0.003840	10

NOTE: (1) Standard Clock Oscillator.

TABLE I. CLK Rate versus Data Output Rate.

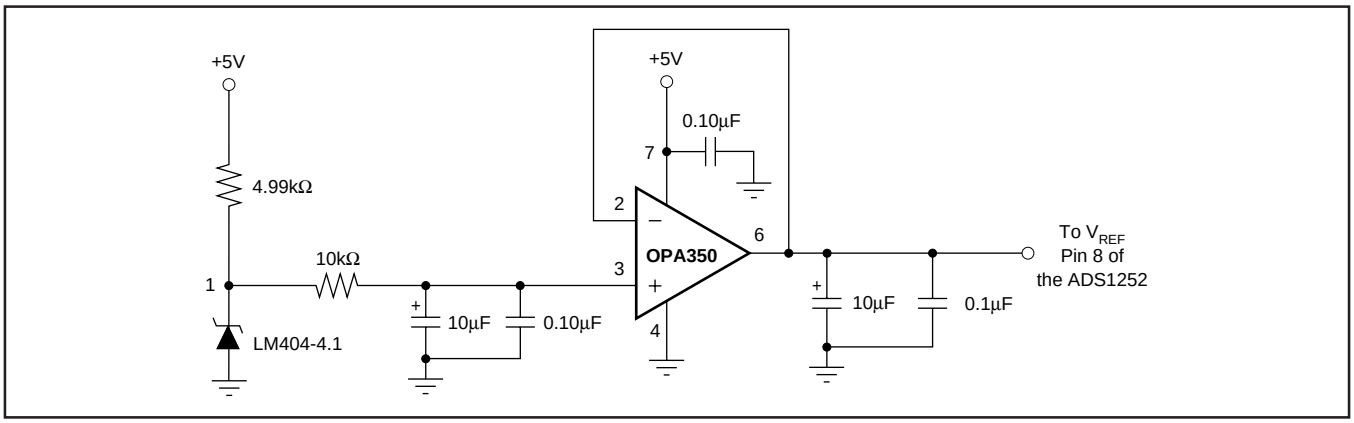


FIGURE 2. Recommended External Voltage Reference Circuit for Best Low Noise Operation with the ADS1252.

REFERENCE INPUT

Reference input takes an average current of 220µA with a 16MHz system clock. This current will be proportional to the system clock. A buffered reference is needed for ADS1252. The recommended reference circuit is shown in Figure 2.

Reference voltages higher than 4.096V will increase the full-scale range, while the absolute internal circuit noise of the converter remains the same. This will decrease the noise in terms of ppm of full scale, which increases the effective resolution.

Reference voltages lower than 4.096V will decrease the full-scale range, while the absolute internal circuit noise at the converter remains the same. This will increase the noise in terms of ppm of full scale. Therefore, the use of a lower reference voltage will reduce the effective resolution.

DIGITAL FILTER

The digital filter of the ADS1252, referred to as a $sinc^5$ filter, computes the digital result based on the most recent outputs from the delta-sigma modulator. At the most basic level, the digital filter can be thought of as simply averaging the modulator results in a weighted form and presenting this average as the digital output. The digital output rate, or data rate, scales directly with the system CLK frequency. This allows the data output rate to be changed over a very wide range (five orders of magnitude) by changing the system CLK frequency. However, it is important to note that the –3dB point of the filter is 0.216 times the data output rate, so the data output rate should allow for sufficient margin to prevent attenuation of the signal of interest.

Since the conversion result is essentially an average, the data output rate determines the location of the resulting notches in the digital filter (see Figure 3). Note that the first notch is located at the data output rate frequency, and subsequent notches are located at integer multiples of the data output rate to allow for rejection of not only the fundamental frequency, but also harmonic frequencies. In this manner, the data output rate can be used to set specific notch frequencies in the digital filter response. For example, if the rejection of power line frequencies is desired, then the data output rate can simply be set to the power line frequency. For 50Hz rejection, the system CLK frequency should be 19.200kHz, this will set the data output rate to 50Hz (see Table I and Figure 4). For 60Hz rejection, the system CLK frequency should be 20.040kHz, this will set the data output rate to 60Hz (see Table I and Figure 5). If both 50Hz and 60Hz rejection is required, then the system CLK should be 3.840kHz; this will set the data output rate to 10Hz and reject both 50Hz and 60Hz (See Table I and Figure 6).

There is an additional benefit in using a lower data output rate. It provides better rejection of signals in the frequency band of interest. For example, with a 50Hz data output rate, a significant signal at 75Hz may alias back into the passband at 25Hz. This is due to the fact that rejection at 75Hz may only be 66dB in the stopband—frequencies higher than the first notch frequency (see Figure 4). However, setting the data output rate to 10Hz will provide 135 dB rejection at 75Hz (see Figure 6). A similar benefit is gained at frequencies near the data output rate (see Figures 7, 8, 9, and 10). For example, with a 50Hz data output rate, rejection at 55Hz may only be 105dB (see Figure 7). However, with a 10Hz data output rate, rejection at 55Hz will be 122dB (see Figure 8). If a slower data output rate does not meet the system requirements, then the analog front end can be designed to provide the needed attenuation to prevent aliasing. Additionally the data output rate may be increased and additional digital filtering may be done in the processor or controller.

The digital filter is described by the following transfer function:

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi \bullet f \bullet 64}{f_{MOD}}\right)}{64 \bullet \sin\left(\frac{\pi \bullet f}{f_{MOD}}\right)} \right|^5$$

or

$$H(z) = \left(\frac{1 - z^{-64}}{64 \bullet \left(1 - z^{-1}\right)} \right)^5$$

The digital filter requires five conversions to fully settle. The modulator has an oversampling ratio of 64, therefore, it requires 5 • 64, or 320 modulator results, or clocks, to fully settle. Since the modulator clock is derived from the system

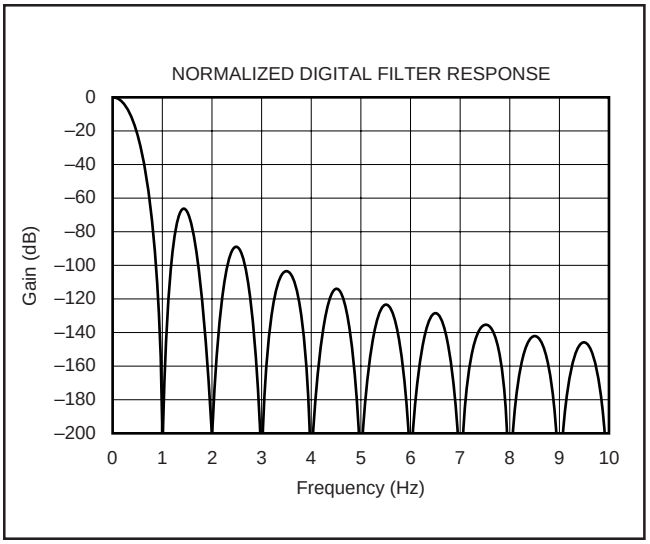


FIGURE 3. Normalized Digital Filter Response.

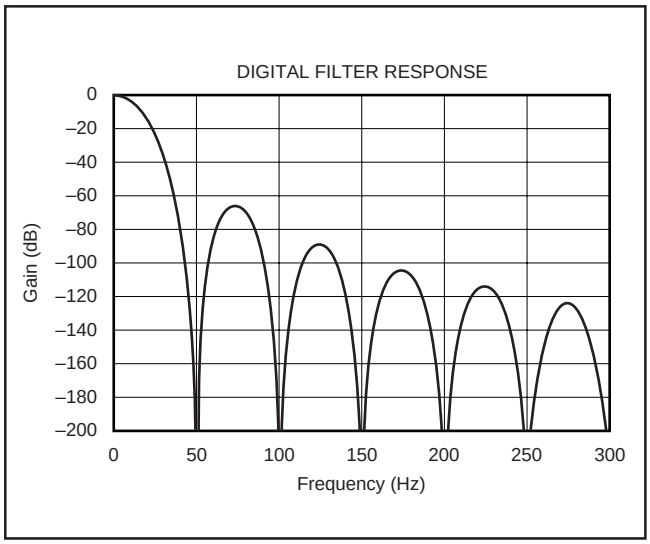


FIGURE 4. Digital Filter Response (50Hz).

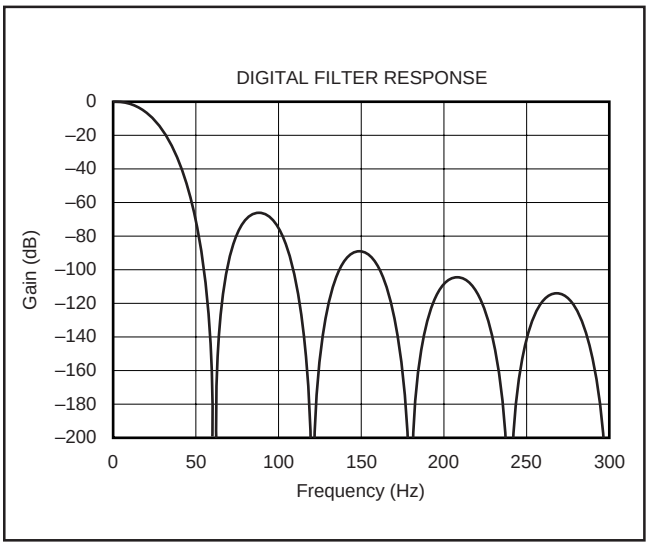


FIGURE 5. Digital Filter Response (60Hz).

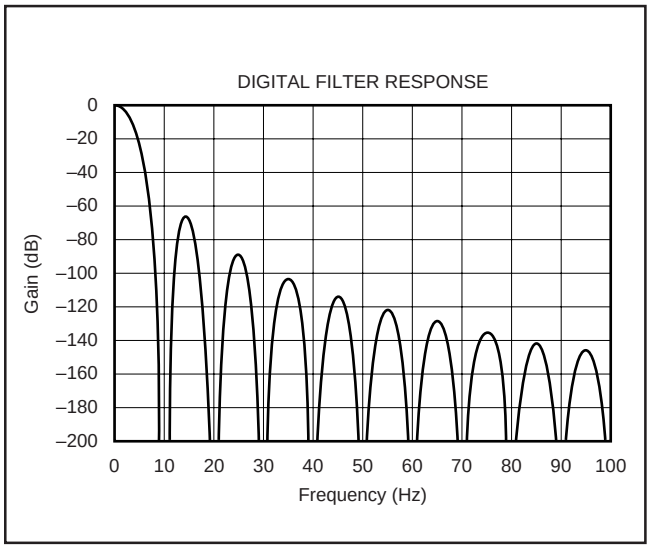


FIGURE 6. Digital Filter Response (10Hz Multiples).

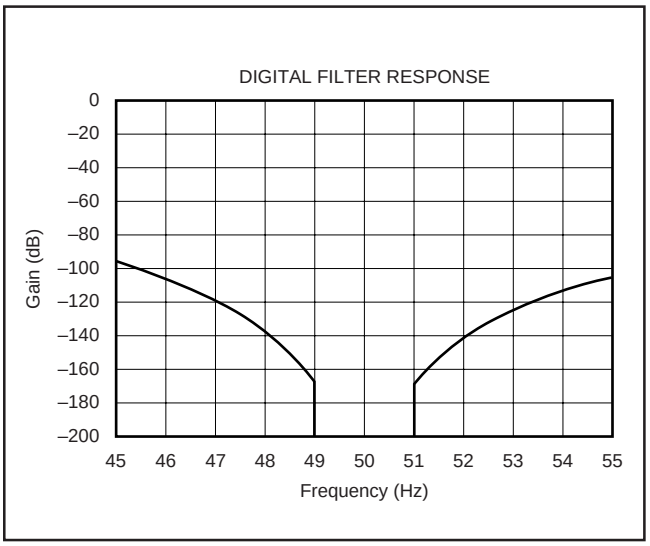


FIGURE 7. Expanded Digital Filter Response (50Hz with a 50Hz Notch).

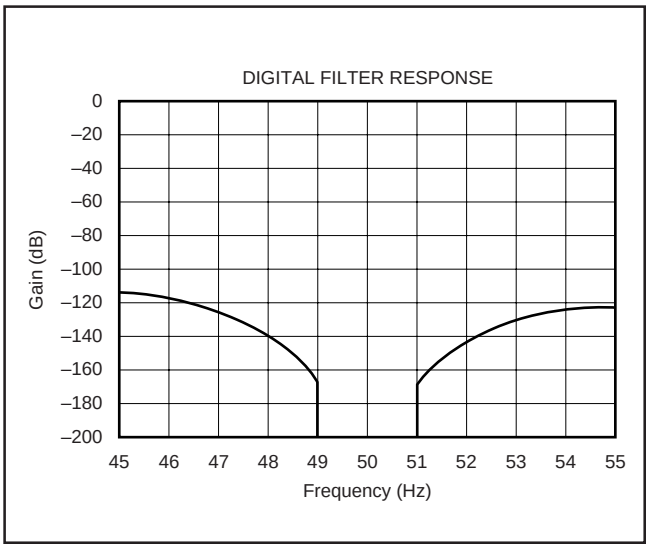


FIGURE 8. Expanded Digital Filter Response (50Hz with a 10Hz Notch).

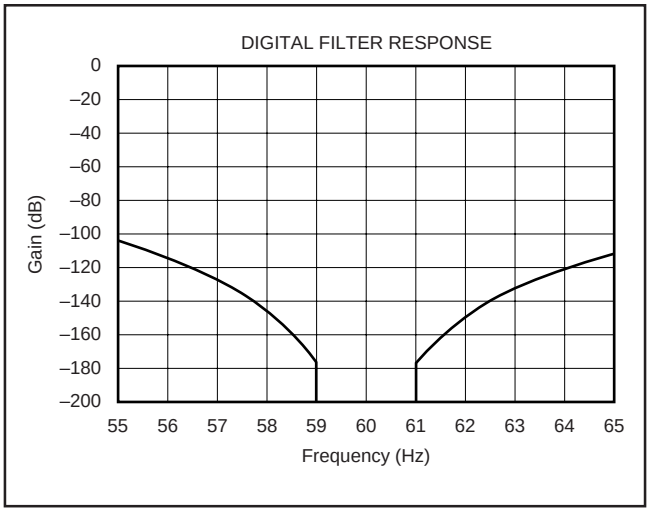


FIGURE 9. Expanded Digital Filter Response (60Hz with a 60Hz Notch).

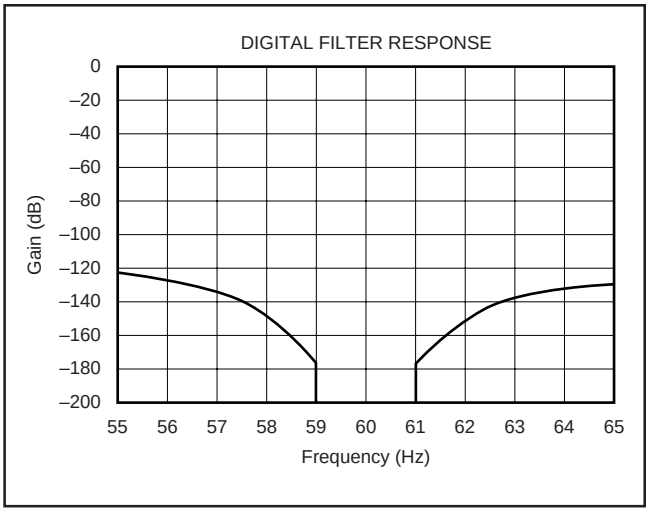


FIGURE 10. Expanded Digital Filter Response (60Hz with a 10Hz Notch).

clock (CLK) (modulator clock = CLK ÷ 6), the number of system clocks required for the digital filter to fully settle is 5 • 64 • 6, or 1920 CLKs. This means that any significant step change at the analog input requires five full conversions to settle. However, if the analog input change occurs asynchronously to the DOUT/$\overline{\text{DRDY}}$ pulse, six conversions are required to ensure full settling.

CONTROL LOGIC

The control logic is used for communications and control of the ADS1252.

Power-Up Sequence

Prior to power-up, all digital and analog input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they should never exceed $+V_D$.

Once the ADS1252 powers up, the DOUT/$\overline{\text{DRDY}}$ line will pulse LOW on the first conversion. This data will not be valid. The sixth pulse of DOUT/$\overline{\text{DRDY}}$ will be valid data from the analog input signal.

DOUT/$\overline{\text{DRDY}}$

The DOUT/$\overline{\text{DRDY}}$ output signal alternates between two modes of operation. The first mode of operation is the Data Ready mode ($\overline{\text{DRDY}}$) to indicate that new data has been loaded into the data output register and is ready to be read. The second mode of operation is the Data Output (DOUT) mode and is used to serially shift data out of the Data Output Register (DOR). The time domain partitioning of the $\overline{\text{DRDY}}$ and DOUT function is shown in Figure 11.

The basic timing for DOUT/$\overline{\text{DRDY}}$ is shown in Figure 12. During the time defined by t_2, t_3, and t_4, the DOUT/$\overline{\text{DRDY}}$ pin functions in $\overline{\text{DRDY}}$ mode. The state of the DOUT/$\overline{\text{DRDY}}$ pin would be HIGH prior to the internal transfer of new data to the DOR. The result of the A/D conversion would be written to the DOR from MSB to LSB in the time defined by t_1 (see Figures 11 and 12). The DOUT/$\overline{\text{DRDY}}$ line would then pulse LOW for the time defined by t_2, and then pulse HIGH for the time defined by t_3 to indicate that new data was available to be read. At this point, the function of the DOUT/$\overline{\text{DRDY}}$ pin would change

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DRDY}	Conversion Cycle		384 • CLK		ns
DRDY Mode	$\overline{\text{DRDY}}$ Mode		36 • CLK		ns
DOUT Mode	DOUT Mode		348 • CLK		ns
t_1	DOR Write Time		6 • CLK		ns
t_2	DOUT/$\overline{\text{DRDY}}$ LOW Time		6 • CLK		ns
t_3	DOUT/$\overline{\text{DRDY}}$ HIGH Time (Prior to Data Out)		6 • CLK		ns
t_4	DOUT/$\overline{\text{DRDY}}$ HIGH Time (Prior to Data Ready)		24 • CLK		ns
t_5	Rising Edge of CLK to Falling Edge of DOUT/$\overline{\text{DRDY}}$			30	ns
t_6	End of $\overline{\text{DRDY}}$ Mode to Rising Edge of First SCLK	30			ns
t_7	End of $\overline{\text{DRDY}}$ Mode to Data Valid (Propogation Delay)			30	ns
t_8	Falling Edge of SCLK to Data Valid (Hold Time)	5			ns
t_9	Falling Edge of SCLK to Next Data Out Valid (Propogation Delay)			30	ns
t_{10}	SCLK Setup Time for Synchronization or Power Down	30			ns
t_{11}	DOUT/$\overline{\text{DRDY}}$ Pulse for Synchronization or Power Down		3 • CLK		ns
t_{12}	Rising Edge of SCLK Until Start of Synchronization	1537 • CLK		7679 • CLK	ns
t_{13}	Synchronization Time	0.5 • CLK		6143.5 • CLK	ns
t_{14}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode		314.5 • CLK		ns
t_{15}	Rising Edge of SCLK Until Start of Power Down	7681 • CLK			ns
t_{16}	Falling Edge of CLK (After SCLK Goes Low) Until Start of $\overline{\text{DRDY}}$ Mode	591.5 • CLK		592.5 • CLK	ns
t_{17}	Falling Edge of Last DOUT/$\overline{\text{DRDY}}$ to Start of Power Down		6143.5 • CLK		ns

TABLE II. Digital Timing.

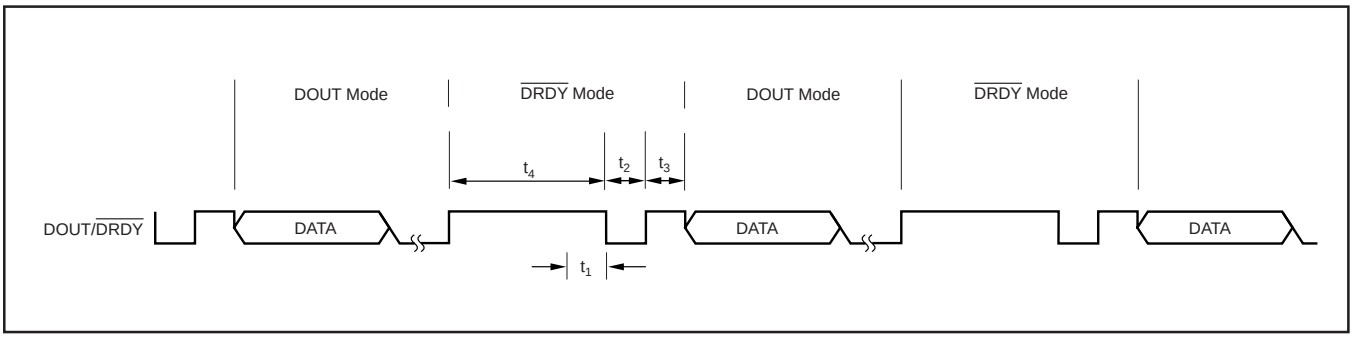


FIGURE 11. DOUT/$\overline{\text{DRDY}}$ Partitioning.

to DOUT mode. Data would be shifted out on the pin after t_7. The device communicating with the ADS1252 can provide SCLKs to the ADS1252 after the time defined by t_6. The normal mode of reading data from the ADS1252 would be for the device reading the ADS1252 to latch the data on the rising edge of SCLK (since data is shifted out of the ADS1252 on the falling edge of SCLK). In order to retrieve valid data, the entire DOR must be read before the DOUT/$\overline{\text{DRDY}}$ pin reverts back to $\overline{\text{DRDY}}$ mode.

If SCLKs were not provided to the ADS1252 during the DOUT mode, the MSB of the DOR would be present on the DOUT/$\overline{\text{DRDY}}$ line until the time defined by t_4. If an incomplete read of the ADS1252 took place while in DOUT mode (i.e., less than 24 SCLKs were provided), the state of the last bit read would be present on the DOUT/$\overline{\text{DRDY}}$ line until the time defined by t_4. If more than 24 SCLKs were provided during DOUT mode, the DOUT/$\overline{\text{DRDY}}$ line would stay LOW until the time defined by t_4.

The internal data pointer for shifting data out on DOUT/$\overline{\text{DRDY}}$ is reset on the falling edge of the time defined by t_1 and t_4. This ensures that the first bit of data shifted out of the ADS1252 after $\overline{\text{DRDY}}$ mode is always the MSB of new data.

SYNCHRONIZING MULTIPLE CONVERTERS

The normal state of SCLK is LOW. However, by holding SCLK HIGH, multiple ADS1252s can be synchronized. This is accomplished by holding SCLK HIGH for at least four, but less than twenty, consecutive DOUT/$\overline{\text{DRDY}}$ cycles (see Figure 13). After the ADS1252 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/$\overline{\text{DRDY}}$ cycles, the DOUT/$\overline{\text{DRDY}}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. The modulator will be released from reset and synchronization will occur on the falling edge of SCLK. It is important to note that prior to synchronization, the DOUT/$\overline{\text{DRDY}}$ pulse of multiple ADS1252s in the system could have a difference in timing up to one $\overline{\text{DRDY}}$ period. Therefore to ensure synchronization, the SCLK should be held HIGH for at least five $\overline{\text{DRDY}}$ cycles. The first DOUT/$\overline{\text{DRDY}}$ pulse after the falling edge of SCLK will occur at t_{14}. Valid data will not be present until the sixth DOUT/$\overline{\text{DRDY}}$ pulse.

POWER-DOWN MODE

The normal state of SCLK is LOW. However, by holding SCLK HIGH, the ADS1252 will enter power-down mode. This is accomplished by holding SCLK HIGH for at least twenty consecutive DOUT/$\overline{\text{DRDY}}$ periods (see Figure 14). After the ADS1252 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/$\overline{\text{DRDY}}$ cycles, the DOUT/$\overline{\text{DRDY}}$ pin will pulse LOW for 3 CLK cycles and then be held HIGH, and the modulator will be held in a reset state. If SCLK is held HIGH for an additional sixteen DOUT/$\overline{\text{DRDY}}$ periods, the ADS1252 will enter power-down mode. The part will be released from power-down mode on the falling edge of SCLK. It is important to note that the DOUT/$\overline{\text{DRDY}}$ pin will be held HIGH after four DOUT/$\overline{\text{DRDY}}$ cycles, but power-down mode will not be entered for an additional sixteen DOUT/$\overline{\text{DRDY}}$ periods. The first DOUT/$\overline{\text{DRDY}}$ pulse after the falling edge of SCLK will occur at t_{16}. Subsequent DOUT/$\overline{\text{DRDY}}$ pulses will occur normally. Valid data will not be present until the sixth DOUT/$\overline{\text{DRDY}}$ pulse.

SERIAL INTERFACE

The ADS1252 includes a simple serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Communications with the ADS1252 can commence on the first detection of the DOUT/$\overline{\text{DRDY}}$ pulse after power up, although data will not be valid until the sixth conversion.

It is important to note that the data from the ADS1252 is a 24-bit result transmitted MSB-first in Offset Two's Complement format, as shown in Table III.

DIFFERENTIAL VOLTAGE INPUT	DIGITAL OUTPUT (HEX)
+Fulll Scale	7FFFFFH
Zero	000000H
–Full Scale	800000H

TABLE III. ADS1252 Data Format (Offset Two's Complement).

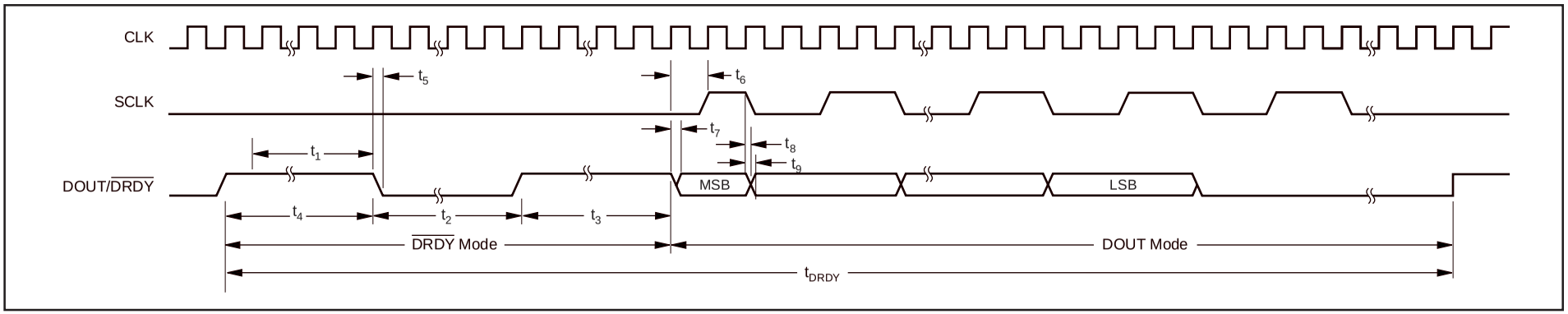


FIGURE 12. DOUT/$\overline{\text{DRDY}}$ Timing.

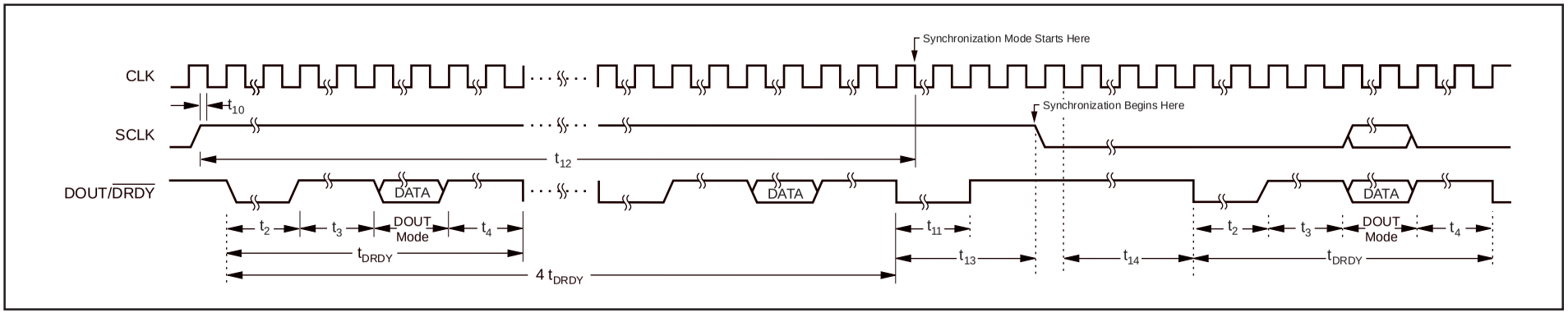


FIGURE 13. Synchronization Mode.

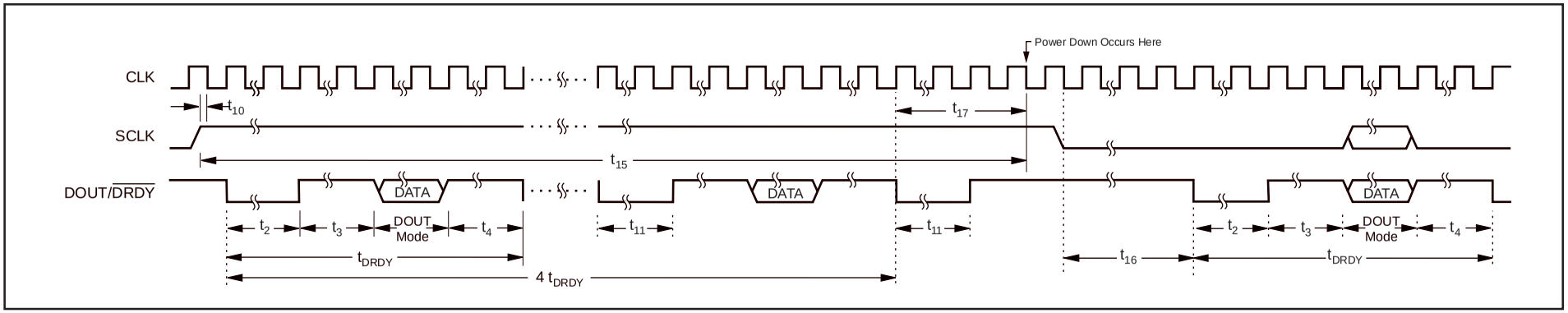


FIGURE 14. Power-Down Mode.

A simple two-wire interface is shown in Figure 15. Essentially P3.2 ($\overline{INT0}$) generates an internal interrupt when DOUT/$\overline{DRDY}$ pulses LOW. The user firmware in the 8xC51 vectors to the interupt handler and shifts the data in using P3.1 as SCLK and P3.2 as data in. The P1.0 output from 8xC51 is a free-running clock.

The data must be clocked out before the ADS1252 enters $\overline{DRDY}$ mode to ensure reception of valid data, as described in the DOUT/$\overline{DRDY}$ section of this data sheet.

ISOLATION

The serial interface of the ADS1252 provides for simple isolation methods. An example of an isolated three-wire interface is shown in Figure 16. The ISO150 is used to transmit the digital clocks over the isolation barrier. In addition, the digital output of the ADS1252 can, in some cases, drive opto-isolators directly.

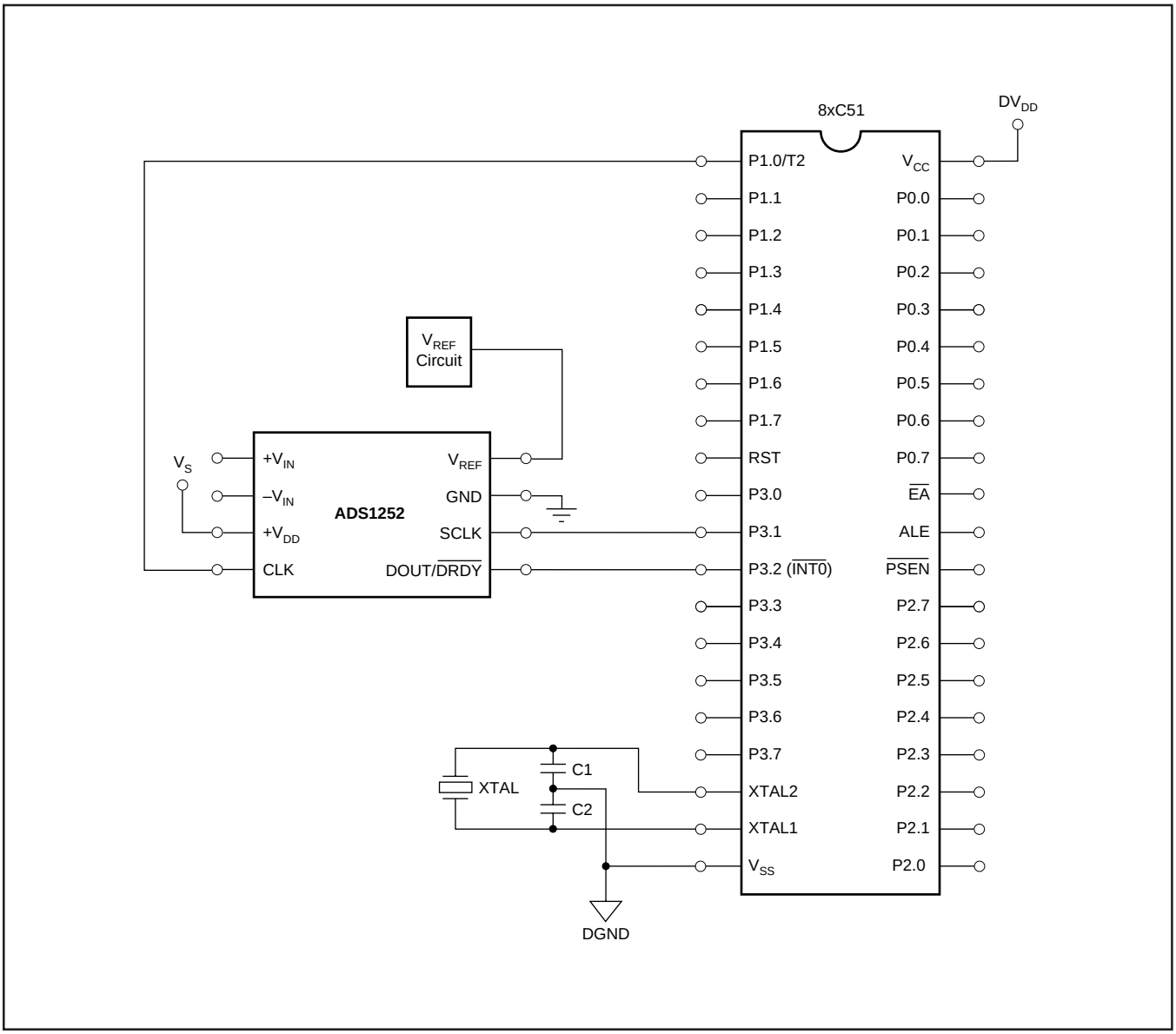


FIGURE 15. Two-Wire Interface to an 8xC51.

LAYOUT

POWER SUPPLY

The power supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1252, power supply rejection will be a concern. Avoid running digital lines under the device as they may couple noise onto the die. High frequency noise can capacitively couple into the analog portion of the device and will alias back into the passband of the digital filter, affecting the conversion result.

GROUNDING

The analog and digital sections of the system design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. GND should be connected to the analog ground plane, as well as all other analog grounds. Do not join the analog and digital ground planes on the board, but instead connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the ADS1252 and for all components in the design. All decoupling capacitors, and specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF to 10µF capacitor, in parallel with a 0.1µF ceramic capacitor, should be used to decouple V_D to GND.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. Achieving 24 bits of noise performance is a great deal more difficult than achieving 12 bits of noise performance. In general, a system can be broken up into four different stages:

- Analog Processing
- Analog Portion of the ADS1252
- Digital Portion of the ADS1252
- Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and gain), a microcontroller, and one clock source, one can achieve high resolution by powering all components by a common power supply. In addition, all components could share a common ground plane. Thus, there would be no distinctions between “analog” power and ground, and “digital” power and ground. The layout should still include a power plane, a ground plane, and careful decoupling. In a more extreme case the design could include:

- Multiple ADS1252s
- Extensive Analog Signal Processing
- One or More Microcontrollers, Digital Signal Processors, or Microprocessors
- Many Different Clock Sources
- Interconnections to Various Other Systems

High resolution will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible. For example, each ADS1252 may have its own “analog” processing front end.

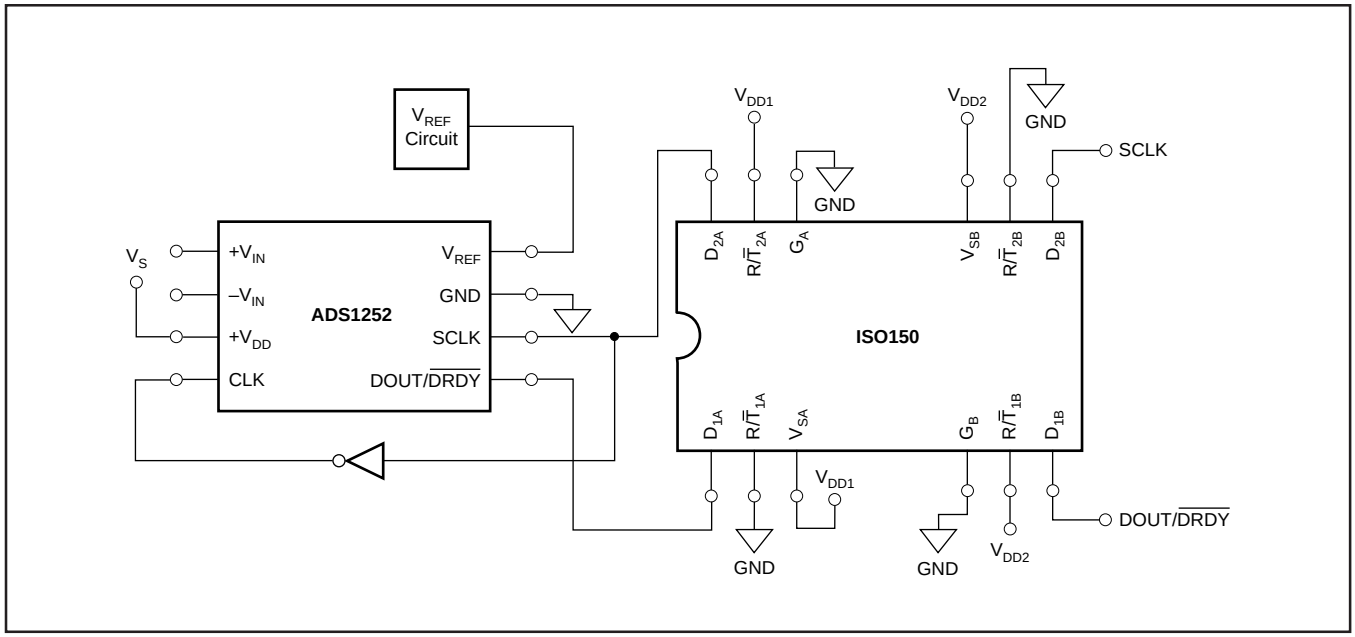


FIGURE 16. Isolated Three-Wire Interface.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Differential Voltage—for an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1252 are at 2.048V, the differential voltage is 0V. If one analog input is at 0V and the other analog input is at 4.096V, then the differential voltage magnitude is 4.096V. This is the case regardless of which input is at 0V and which is at 4.096V. The digital output result, however, is quite different. The analog input differential voltage is given by the following equation:

$$+V_{IN} - -V_{IN}$$

A positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative. For example, a positive full-scale output is produced when the converter is configured with a 4.096V reference, and the analog input differential is 4.096V. The negative full-scale output is produced when the differential voltage is –4.096V. In each case, the actual input voltages must remain within the XGND to $+V_{DD}$ range.

Actual Analog Input Voltage—the voltage at any one analog input relative to GND.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1252 is defined as the "input" which produces the positive full-scale digital output minus the "input" which produces the negative full-scale digital output. For example, when the converter is configured with a 4.096V reference, the differential full-scale range is:

[4.096V (positive full scale) – (–4.096V) (negative full scale)] = 8.192V

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full–Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

Conversion Cycle—as used here, a conversion cycle refers to the time period between DOUT/$\overline{\text{DRDY}}$ pulses.

Effective Resolution (ER)—of the ADS1252 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and µVrms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation based on a given number of results. Noise occurs randomly; the rms value represents a statistical measure which is one standard deviation. The ER in bits can be computed as follows:

$$\text{ER in bits rms} = \frac{20 \bullet \log\left(\frac{2 \bullet V_{REF}}{\text{Vrms noise}}\right)}{6.02}$$

The $2 \bullet V_{REF}$ figure in each calculation represents the full-scale range of the ADS1252. This means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared, regardless of the units.

Noise Reduction—for random noise, the ER can be improved with averaging. The result is the reduction in noise by the factor $\sqrt{N}$, where N is the number of averages, as shown in Table IV. This can be used to achieve true 24-bit performance at a lower data rate. To achieve 24 bits of resolution, more than 24 bits must be accumulated. A 36-bit accumulator is required to achieve an ER of 24 bits. The following uses V_{REF} = 4.096V. With the ADS1252 outputting data at 40kHz, a 4096 point average will take 102.4ms. The benefits of averaging will be degraded if the input signal drifts during that 100ms.

N (NUMBER OF AVERAGES)	NOISE REDUCTION FACTOR	ER IN VRMS	ER IN BITS RMS
1	1	31.3µV	18
2	1.414	22.1µV	18.5
4	2	15.6µV	19
8	2.82	11.1µV	19.5
16	4	7.82µV	20
32	5.66	5.53µV	20.5
64	8	3.91µV	21
128	11.3	2.77µV	21.5
256	16	1.96µV	22
512	22.6	1.38µV	22.5
1024	32	978nV	23
2048	45.25	692nV	23.5
4096	64	489nV	24

TABLE IV. Averaging.