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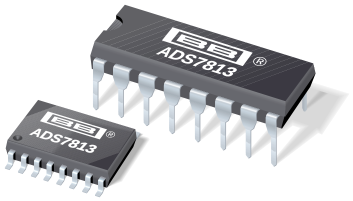


ADS7813

Low-Power, Serial 16-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **20µs max CONVERSION TIME**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 12-BIT ADS7812**
- **EASY-TO-USE SERIAL INTERFACE**
- **16-PIN 0.3" PLASTIC DIP AND SOIC**
- **±2.0LSB max INL**
- **87dB min SINAD**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **MULTIPLE INPUT RANGES**
- **35mW max POWER DISSIPATION**
- **NO MISSING CODES**
- **50µW POWER DOWN MODE**

APPLICATIONS

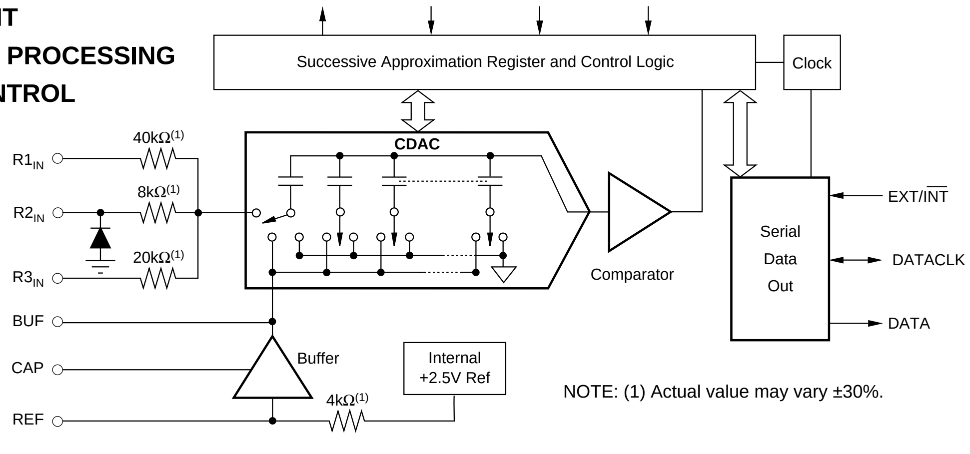
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION SYSTEMS**
- **ROBOTICS**
- **INDUSTRIAL CONTROL**
- **TEST EQUIPMENT**
- **DIGITAL SIGNAL PROCESSING**
- **DSP SERVO CONTROL**

DESCRIPTION

The ADS7813 is a low-power, single +5V supply, 16-bit sampling analog-to-digital converter. It contains a complete 16-bit capacitor-based SAR A/D with a sample/hold, clock, reference, and serial data interface.

The converter can be configured for a variety of input ranges including ±10V, ±5V, 0V to 10V, and 0.5V to 4.5V. A high impedance 0.3V to 2.8V input range is also available (input impedance > 10MΩ). For most input ranges, the input voltage can swing to +16.5V or –16.5V without damage to the converter.

A flexible SPI compatible serial interface allows data to be synchronized to an internal or external clock. The ADS7813 is specified at a 40kHz sampling rate over the –40°C to +85°C temperature range. It is available in a 16-pin 0.3" plastic DIP or a 16-lead SOIC package.



NOTE: (1) Actual value may vary ±30%.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

At T_A = –40°C to +85°C, f_S = 40kHz, V_S = +5V ±5%, using internal reference, unless otherwise specified.

		ADS7813P, U			ADS7813PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Range			See Table I			*		
Impedance			See Table I			*		
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time				20			*	µs
Complete Cycle	Acquire and Convert			25			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error				±3		*	±2	LSB(1)
Differential Linearity Error				+3, –2		*	+2, –1	LSB
No Missing Codes		15			16			Bits
Transition Noise(2)			0.6			*		LSB
Full Scale Error(3)				±0.5			±0.25	%
Full Scale Error Drift			±14			*		ppm/°C
Full Scale Error(3)	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±5			*		ppm/°C
Bipolar Zero Error	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±3			*		ppm/°C
Unipolar Zero Error	Unipolar Ranges			±6			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±3			*		ppm/°C
Recovery Time to Rated Accuracy from Power Down(4)	1.0µF Capacitor to CAP		300			*		µs
Power Supply Sensitivity	+4.75V < (V_S = +5V) < +5.25			±12			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 1kHz	90	100		96	102		dB(5)
Total Harmonic Distortion	f_{IN} = 1kHz		–98	–90		–100	–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz	85	89		87	*		dB
Signal-to-Noise	f_{IN} = 1kHz	85	89		87	*		dB
Useable Bandwidth(6)			130			*		kHz
Full Power –3dB Bandwidth			600			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Aperture Jitter			20			*		ps
Transient Response	FS Step		5			*		µs
Overvoltage Recovery(7)			750			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			100			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_S +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format			Serial					
Data Coding			Binary Two's Complement					
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_S			±1			*	µA
Output Capacitance	High-Z State			15			15	pF

SPECIFICATIONS (CONT)

At T_A = –40°C to +85°C, f_S = 40kHz, V_S = +5V ±5%, using internal reference, unless otherwise specified.

		ADS7813P, U			ADS7813PB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY								
V_S		+4.75	+5	+5.25	∗	∗	∗	V
Power Dissipation	f_S = 40kHz			35			∗	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	∗		∗	°C
Derated Performance		–55		+125	∗		∗	°C

∗ Same specification as grade to the left.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) After the ADS7813 is initially powered on and fully settles, this is the time delay after it is brought out of Power Down Mode until all internal settling occurs and the analog input is acquired to rated accuracy, and normal conversions can begin again. (5) All specifications in dB are referred to a full-scale input. (6) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±16.5V
$R2_{IN}$	GND – 0.3V to +16.5V
$R3_{IN}$	±16.5V
REF	GND – 0.3V to V_S + 0.3V
CAP	Indefinite Short to GND Momentary Short to V_S
V_S	7V
Digital Inputs	GND – 0.3V to V_S + 0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

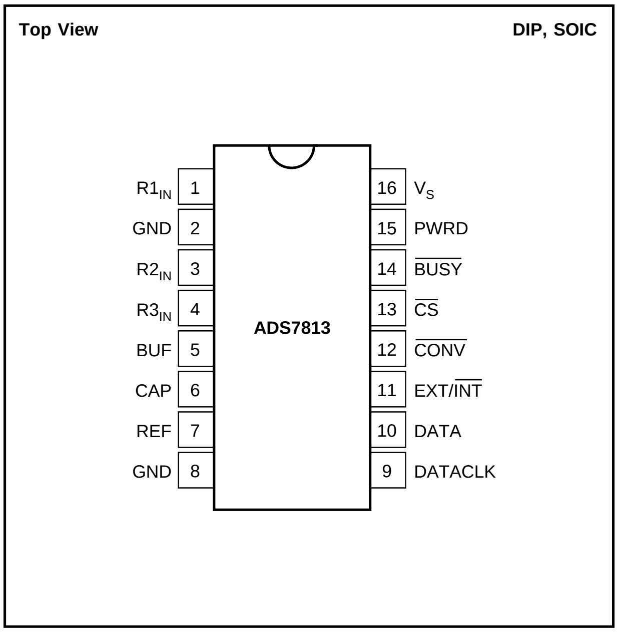
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	GUARANTEED NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7813P	±3	15	85	–40°C to +85°C	Plastic DIP	180
ADS7813PB	±2	16	87	–40°C to +85°C	Plastic DIP	180
ADS7813U	±3	15	85	–40°C to +85°C	SOIC	211
ADS7813UB	±2	16	87	–40°C to +85°C	SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATION

PIN #	NAME	DESCRIPTION
1	$R1_{IN}$	Analog Input. See Tables I and IV.
2	GND	Ground
3	$R2_{IN}$	Analog Input. See Tables I and IV.
4	$R3_{IN}$	Analog Input. See Tables I and IV.
5	BUF	Reference Buffer Output. Connect to $R1_{IN}$, $R2_{IN}$, or $R3_{IN}$, as needed.
6	CAP	Reference Buffer Compensation Node. Decouple to ground with a 1µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor.
7	REF	Reference Input/Output. Outputs internal +2.5V reference via a series 4kΩ resistor. Decouple this voltage with a 1µF to 2.2µF tantalum capacitor to ground. If an external reference voltage is applied to this pin, it will override the internal reference.
8	GND	Ground
9	DATACLK	Data Clock Pin. With EXT/$\overline{INT}$ LOW, this pin is an output and provides the synchronous clock for the serial data. The output is tri-stated when $\overline{CS}$ is HIGH. With EXT/$\overline{INT}$ HIGH, this pin is an input and the serial data clock must be provided externally.
10	DATA	Serial Data Output. The serial data is always the result of the last completed conversion and is synchronized to DATACLK. If DATACLK is from the internal clock (EXT/$\overline{INT}$ LOW), the serial data is valid on both the rising and falling edges of DATACLK. DATA is tri-stated when $\overline{CS}$ is HIGH.
11	EXT/$\overline{INT}$	External or Internal DATACLK Pin. Selects the source of the synchronous clock for serial data. If HIGH, the clock must be provided externally. If LOW, the clock is derived from the internal conversion clock. Note that the clock used to time the conversion is always internal regardless of the status of EXT/$\overline{INT}$.
12	$\overline{CONV}$	Convert Input. A falling edge on this input puts the internal sample/hold into the hold state and starts a conversion regardless of the state of $\overline{CS}$. If a conversion is already in progress, the falling edge is ignored. If EXT/$\overline{INT}$ is LOW, data from the previous conversion will be serially transmitted during the current conversion.
13	$\overline{CS}$	Chip Select. This input tri-states all outputs when HIGH and enables all outputs when LOW. This includes DATA, $\overline{BUSY}$, and DATACLK (when EXT/$\overline{INT}$ is LOW). Note that a falling edge on $\overline{CONV}$ will initiate a conversion even when $\overline{CS}$ is HIGH.
14	$\overline{BUSY}$	Busy Output. When a conversion is started, $\overline{BUSY}$ goes LOW and remains LOW throughout the conversion. If EXT/$\overline{INT}$ is LOW, data is serially transmitted while $\overline{BUSY}$ is LOW. $\overline{BUSY}$ is tri-stated when $\overline{CS}$ is HIGH.
15	PWRD	Power Down Input. When HIGH, the majority of the ADS7813 is placed in a low power mode and power consumption is significantly reduced. $\overline{CONV}$ must be taken LOW prior to PWRD going LOW in order to achieve the lowest power consumption. The time required for the ADS7813 to return to normal operation after power down depends on a number of factors. Consult the Power Down section for more information.
16	V_S	+5V Supply Input. For best performance, decouple to ground with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor.

PIN CONFIGURATION

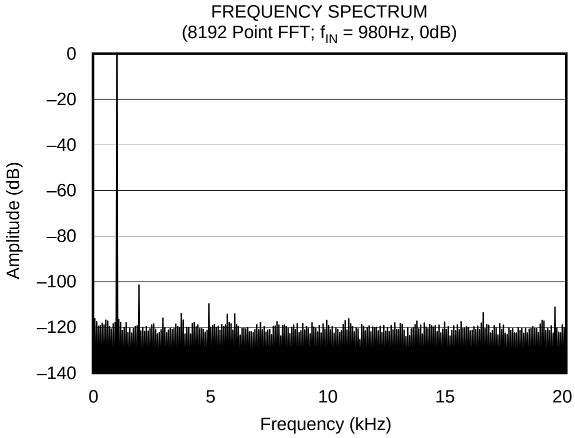


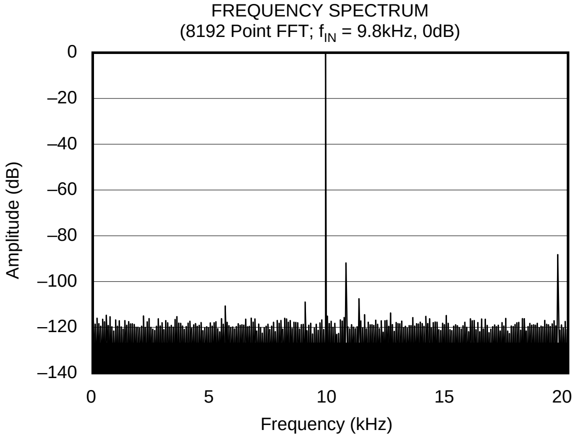
ANALOG INPUT RANGE (V)	CONNECT $R1_{IN}$ TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE (kΩ)
±10V	V_{IN}	BUF	GND	45.7
0.3125V to 2.8125V	V_{IN}	V_{IN}	V_{IN}	> 10,000
±5V	GND	BUF	V_{IN}	26.7
0V to 10V	BUF	GND	V_{IN}	26.7
0V to 4V	BUF	V_{IN}	GND	21.3
±3.33V	V_{IN}	BUF	V_{IN}	21.3
0.5V to 4.5V	GND	V_{IN}	GND	21.3

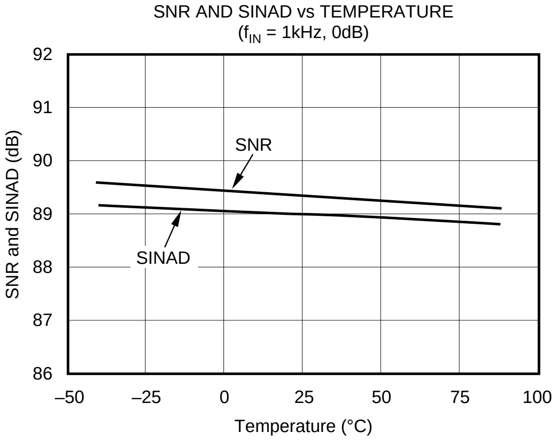
TABLE I. ADS7813 Input Ranges.

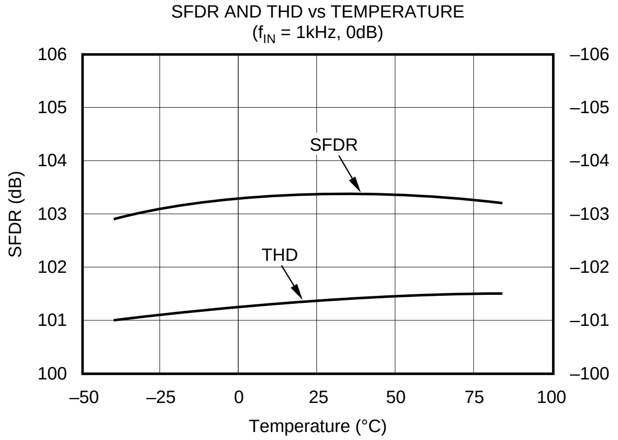
TYPICAL PERFORMANCE CURVES

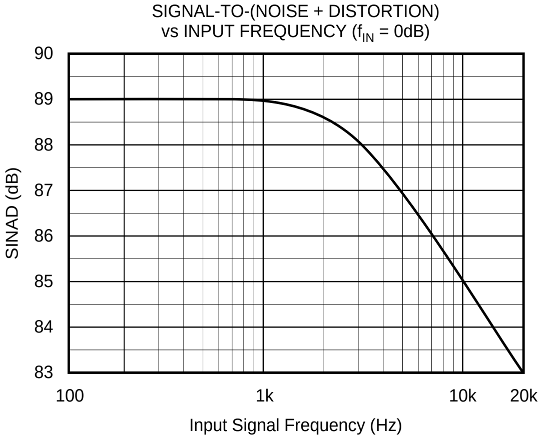
At T_A = +25°C, f_S = 40kHz, V_S = +5V, ±10V input range, using internal reference, unless otherwise noted.

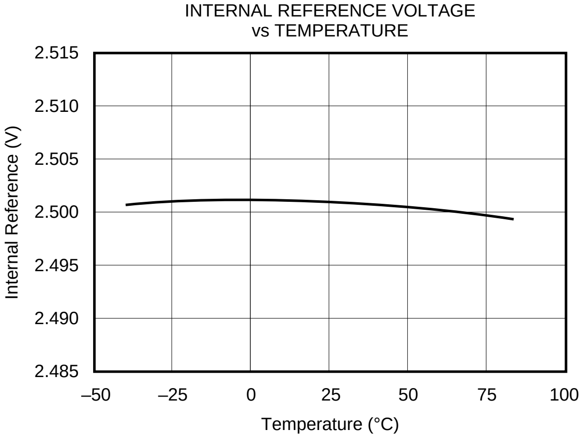






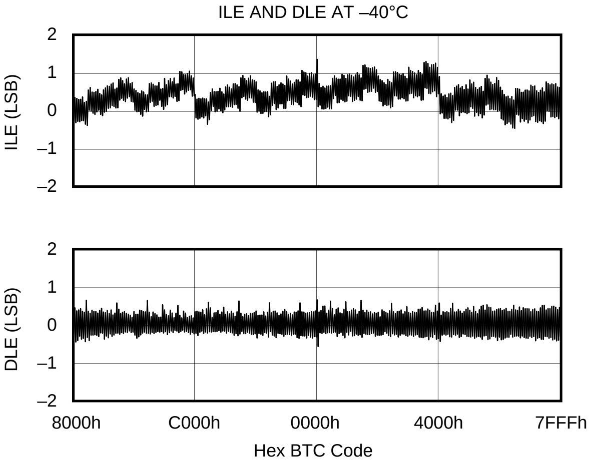


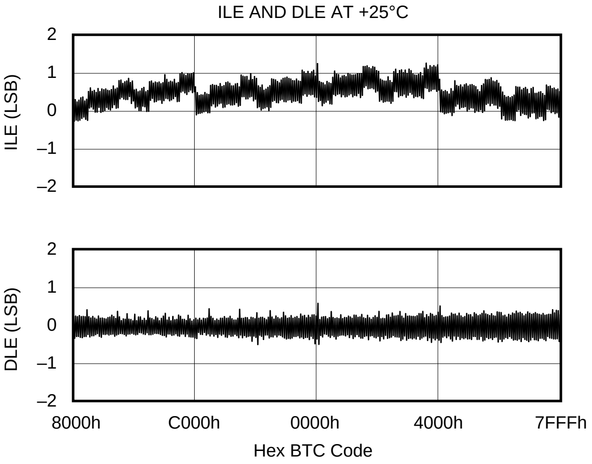


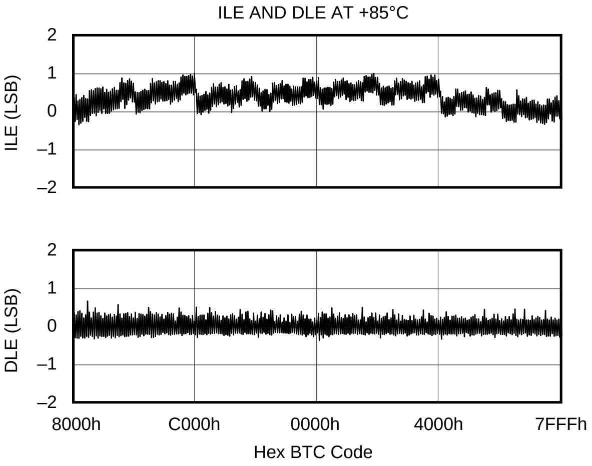


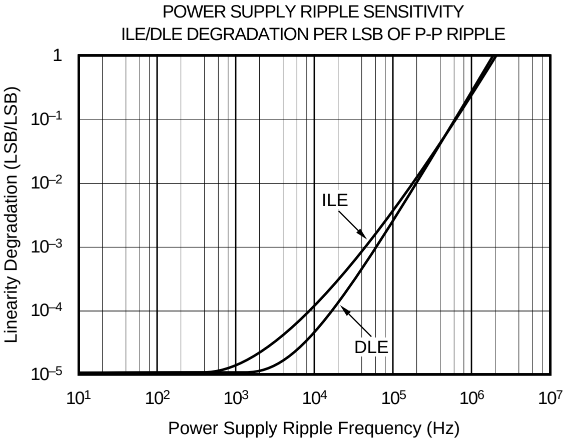
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, f_S = 40kHz, V_S = +5V, ±10V input range, using internal reference, unless otherwise noted.


ILE AND DLE AT –40°C


ILE AND DLE AT +25°C


ILE AND DLE AT +85°C


POWER SUPPLY RIPPLE SENSITIVITY
ILE/DLE DEGRADATION PER LSB OF P-P RIPPLE

BASIC OPERATION

INTERNAL DATACLK

Figure 1a shows a basic circuit to operate the ADS7813 with a ±10V input range. To begin a conversion and serial transmission of the results from the previous conversion, a falling edge must be provided to the CONV input. BUSY will go LOW indicating that a conversion has started and will stay LOW until the conversion is complete. During the conversion, the results of the previous conversion will be transmitted via DATA while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, Binary Two's Complement, and MSB first. Each data bit is valid on both the rising and falling edge of DATACLK. BUSY is LOW during the entire serial transmission and can be used as a frame synchronization signal.

EXTERNAL DATACLK

Figure 1b shows a basic circuit to operate the ADS7813 with a ±10V input range. To begin a conversion, a falling edge must be provided to the CONV input. BUSY will go LOW indicating that a conversion has started and will stay LOW until the conversion is complete. Just prior to BUSY rising near the end of the conversion, the internal working register holding the conversion result will be transferred to the internal shift register.

The internal shift register is clocked via the DATACLK input. The recommended method of reading the conversion result is to provide the serial clock after the conversion has completed. See External DATACLK under the Reading Data section of this data sheet for more information.

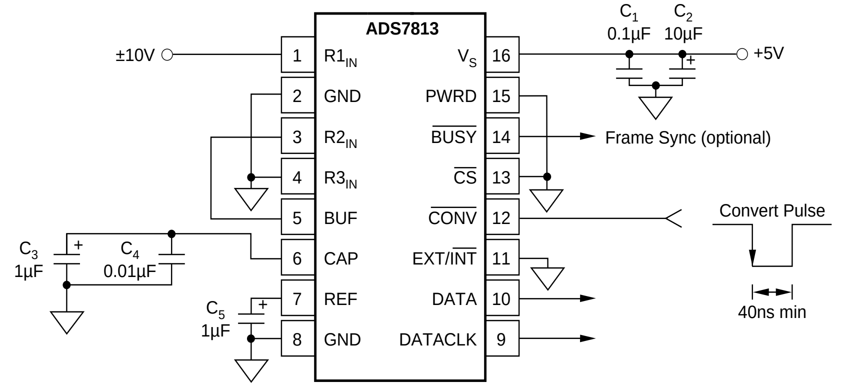
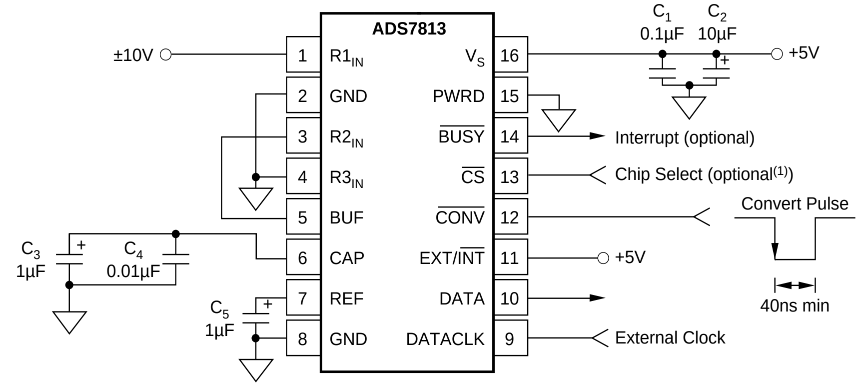


FIGURE 1a. Basic Operation, ±10V Input Range, Internal DATACLK.



NOTE: (1) Tie CS to GND if the outputs will always be active.

FIGURE 1b. Basic Operation, ±10V Input Range, External DATACLK.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Conversion Plus Acquisition Time			25	µs
t_2	$\overline{\text{CONV}}$ LOW to All Digital Inputs Stable			8	µs
t_3	$\overline{\text{CONV}}$ LOW to Initiate a Conversion	40			ns
t_4	$\overline{\text{BUSY}}$ Rising to Any Digital Input Active	0			ns
t_5	$\overline{\text{CONV}}$ HIGH Prior to Start of Conversion	2			µs
t_6	$\overline{\text{BUSY}}$ LOW		19	20	µs
t_7	$\overline{\text{CONV}}$ LOW to $\overline{\text{BUSY}}$ LOW		85	120	ns
t_8	Aperture Delay		40		ns
t_9	Conversion Time		18	20	µs
t_{10}	Conversion Complete to $\overline{\text{BUSY}}$ Rising		1.1	2	µs
t_{11}	Acquisition Time			5	µs
t_{12}	$\overline{\text{CONV}}$ LOW to Rising Edge of First DATACLK		1.4		µs
t_{13}	Internal DATACLK HIGH	250	350	500	ns
t_{14}	Internal DATACLK LOW	600	760	875	ns
t_{15}	Internal DATACLK Period		1.1		µs
t_{16}	DATA Valid to Internal DATACLK Rising	20			ns
t_{17}	Internal DATACLK Falling to DATA Not Valid	400			ns
t_{18}	Falling Edge of Last DATACLK to $\overline{\text{BUSY}}$ Rising		800		ns
t_{19}	External DATACLK Rising to DATA Not Valid	15			ns
t_{20}	External DATACLK Rising to DATA Valid		55	85	ns
t_{21}	External DATACLK HIGH	50			ns
t_{22}	External DATACLK LOW	50			ns
t_{23}	External DATACLK Period	100			ns
t_{24}	$\overline{\text{CONV}}$ LOW to External DATACLK Active	100			ns
t_{25}	External DATACLK LOW or $\overline{\text{CS}}$ HIGH to $\overline{\text{BUSY}}$ Rising	2			µs
t_{26}	$\overline{\text{CS}}$ LOW to Digital Outputs Enabled	85			ns
t_{27}	$\overline{\text{CS}}$ HIGH to Digital Outputs Disabled	85			ns

TABLE II. ADS7813 Timing. T_A = –40°C to +85°C.

STARTING A CONVERSION

If a conversion is not currently in progress, a falling edge on the $\overline{\text{CONV}}$ input places the sample and hold into the hold mode and begins a conversion, as shown in Figure 2 and with the timing given in Table II. During the conversion, the $\overline{\text{CONV}}$ input is ignored. Starting a conversion does not depend on the state of $\overline{\text{CS}}$. A conversion can be started once every 25µs (40kHz maximum conversion rate). There is no minimum conversion rate.

Even though the $\overline{\text{CONV}}$ input is ignored while a conversion is in progress, this input should be held static during the conversion period. Transitions on this digital input can easily couple into sensitive analog portions of the converter, adversely affecting the conversion results (see the Sensitivity to External Digital Signals section of this data sheet for more information).

Ideally, the $\overline{\text{CONV}}$ input should go LOW and remain LOW throughout the conversion. It should return HIGH sometime after $\overline{\text{BUSY}}$ goes HIGH. In addition, it should be HIGH prior to the start of the next conversion for a minimum time period given by t_5. This will ensure that the digital transition on the $\overline{\text{CONV}}$ input will not affect the signal that is acquired for the next conversion.

An acceptable alternative is to return the $\overline{\text{CONV}}$ input HIGH as soon after the start of the conversion as possible. For example, a negative going pulse 100ns wide would make a good $\overline{\text{CONV}}$ input signal. It is strongly recommended that from time t_2 after the start of a conversion until $\overline{\text{BUSY}}$ rises, the $\overline{\text{CONV}}$ input should be held static (either HIGH or LOW). During this time, the converter is more sensitive to external noise.

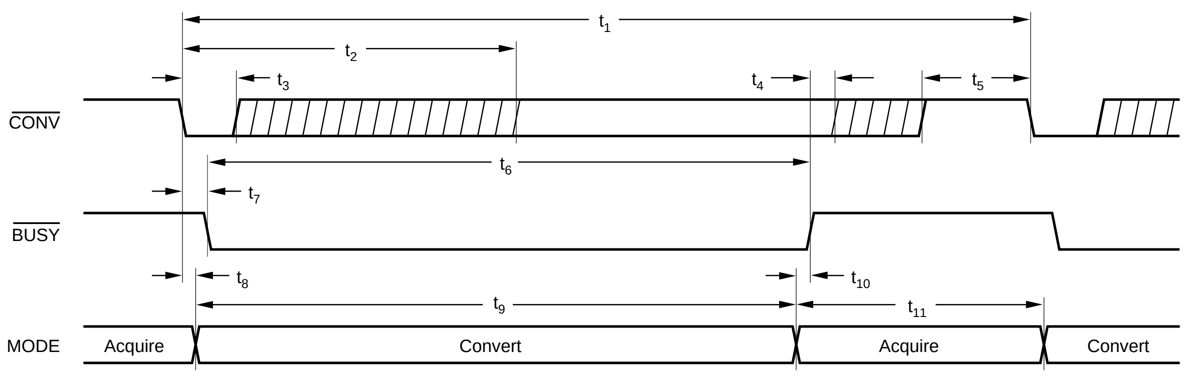
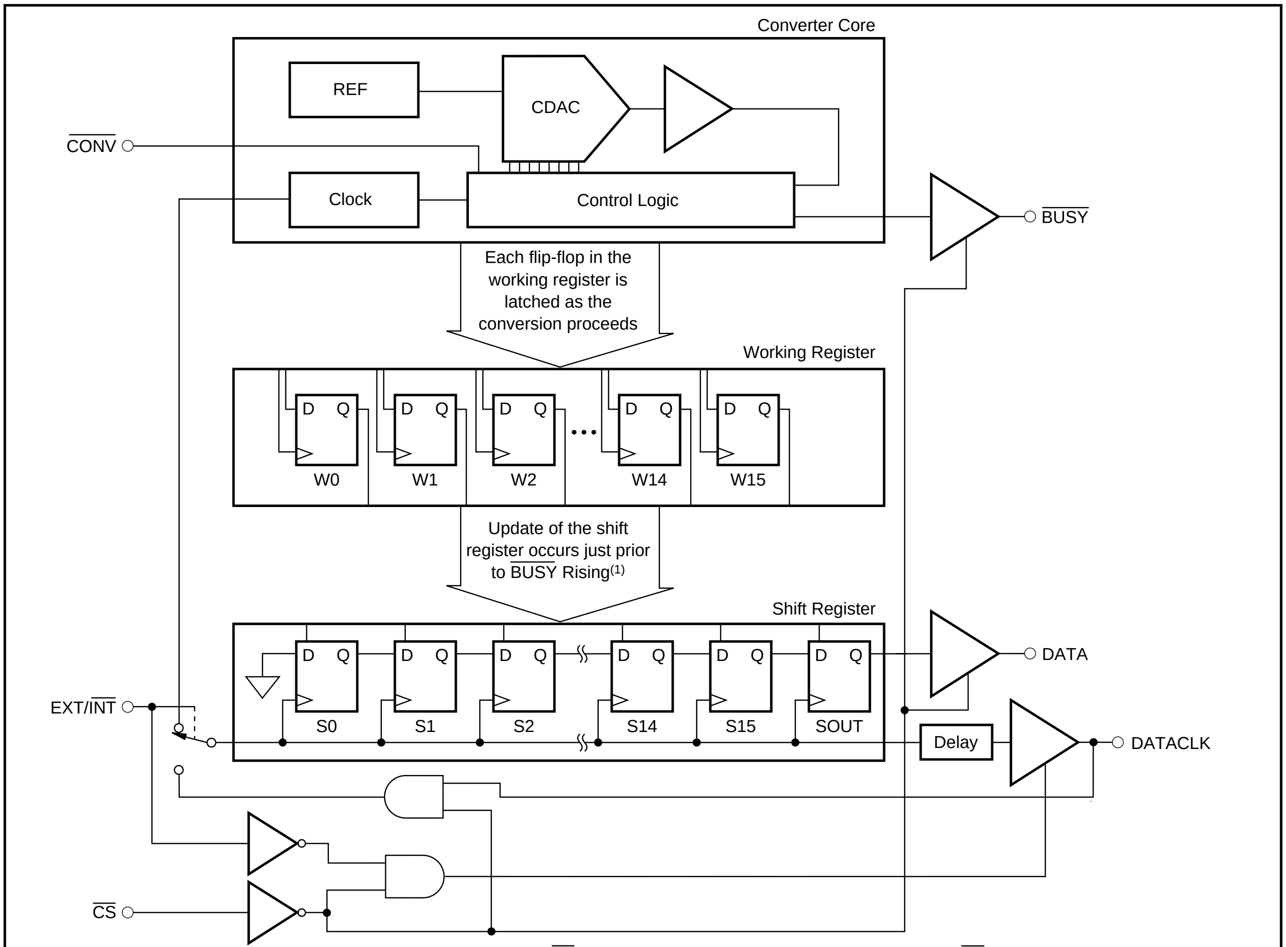


FIGURE 2. Basic Conversion Timing.

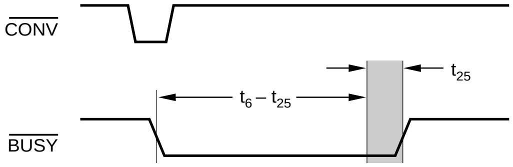
DESCRIPTION	ANALOG INPUT		DIGITAL OUTPUT	
			BINARY TWO'S COMPLEMENT	
Full-Scale Range Least Significant Bit (LSB)	±10V 305µV	0.5V to 4.5V 61µV	BINARY CODE	HEX CODE
+Full Scale –1LSB	9.999695V	4.499939V	0111 1111 1111 1111	7FFF
Midscale	0V	2.5V	0000 0000 0000 0000	0000
Midscale –1LSB	–305µV	2.499939µV	1111 1111 1111 1111	FFFF
–Full Scale	–10V	0.5V	10000 0000 0000 0000	8000

TABLE III. Ideal Input Voltage and Corresponding Digital Output for Two Common Input Ranges.



NOTE: (1) If EXT/$\overline{\text{INT}}$ is HIGH (external clock), DATACLK is HIGH, and $\overline{\text{CS}}$ is LOW during this time, the shift register will not be updated and the conversion result will be lost.

FIGURE 3. Block Diagram of the ADS7813's Digital Inputs and Outputs.



NOTE: Update of the internal shift register occurs in the shaded region. If EXT/$\overline{\text{INT}}$ is HIGH, then DATACLK must be LOW or $\overline{\text{CS}}$ must be HIGH during this time.

FIGURE 4. Timing of the Shift Register Update.

READING DATA

The ADS7813's digital output is in Binary Two's Complement (BTC) format. Table III shows the relationship between the digital output word and the analog input voltage under ideal conditions.

Figure 3 shows the relationship between the various digital inputs, digital outputs, and internal logic of the ADS7813. Figure 4 shows when the internal shift register of the ADS7813 is updated and how this relates to a single conversion cycle. Together, these two figures point out a very important aspect of the ADS7813: the conversion result is not available until after the conversion is complete. The implications of this are discussed in the following sections.

INTERNAL DATACLK

With EXT/$\overline{\text{INT}}$ tied LOW, the result from conversion ‘n’ is serially transmitted during conversion ‘n+1’, as shown in Figure 5 and with the timing given in Table II. Serial transmission of data occurs only during a conversion. When a transmission is not in progress, DATA and DATACLK are LOW.

During the conversion, the results of the previous conversion will be transmitted via DATA, while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, Binary Two’s Complement, and MSB first. Each data bit is valid on both the rising and falling edges of DATACLK. $\overline{\text{BUSY}}$ is LOW during the entire serial transmission and can be used as a frame synchronization signal.

EXTERNAL DATACLK

With EXT/$\overline{\text{INT}}$ tied HIGH, the result from conversion ‘n’ is clocked out after the conversion has completed, during the next conversion (‘n+1’), or a combination of these two. Figure 6 shows the case of reading the conversion result after the conversion is complete. Figure 7 describes reading the result during the next conversion. Figure 8 combines the important aspects of Figures 6 and 7 as to reading part of the result after the conversion is complete and the remainder during the next conversion.

The serial transmission of the conversion result is initiated by a rising edge on DATACLK. The data format is 16-bit, Binary Two’s Complement, and MSB first. Each data bit is valid on the falling edge of DATACLK. In some cases, it

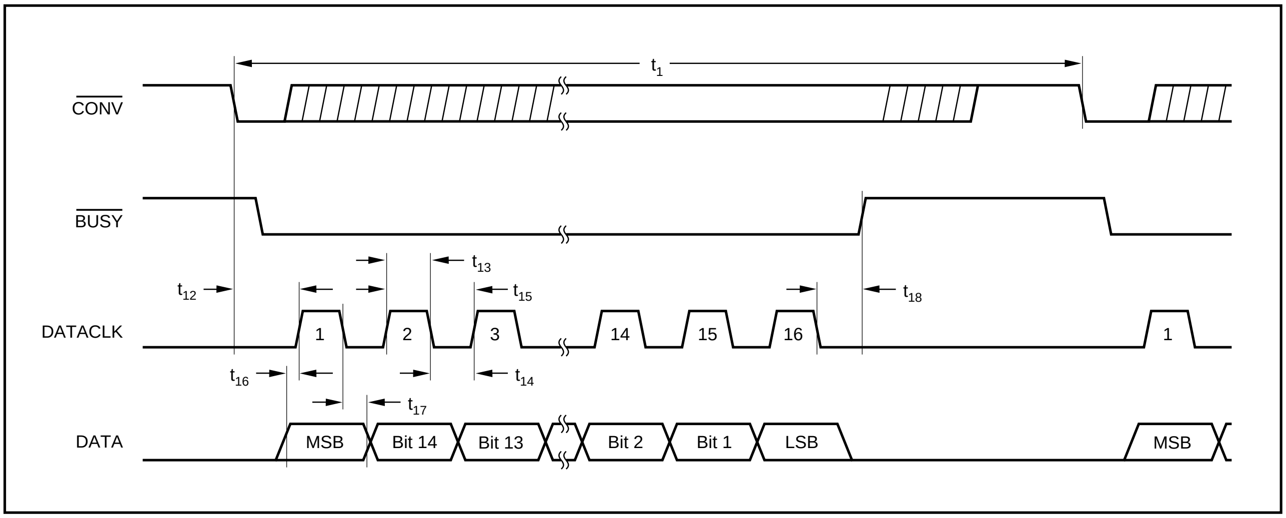


FIGURE 5. Serial Data Timing, Internal Clock (EXT/$\overline{\text{INT}}$ and $\overline{\text{CS}}$ LOW).

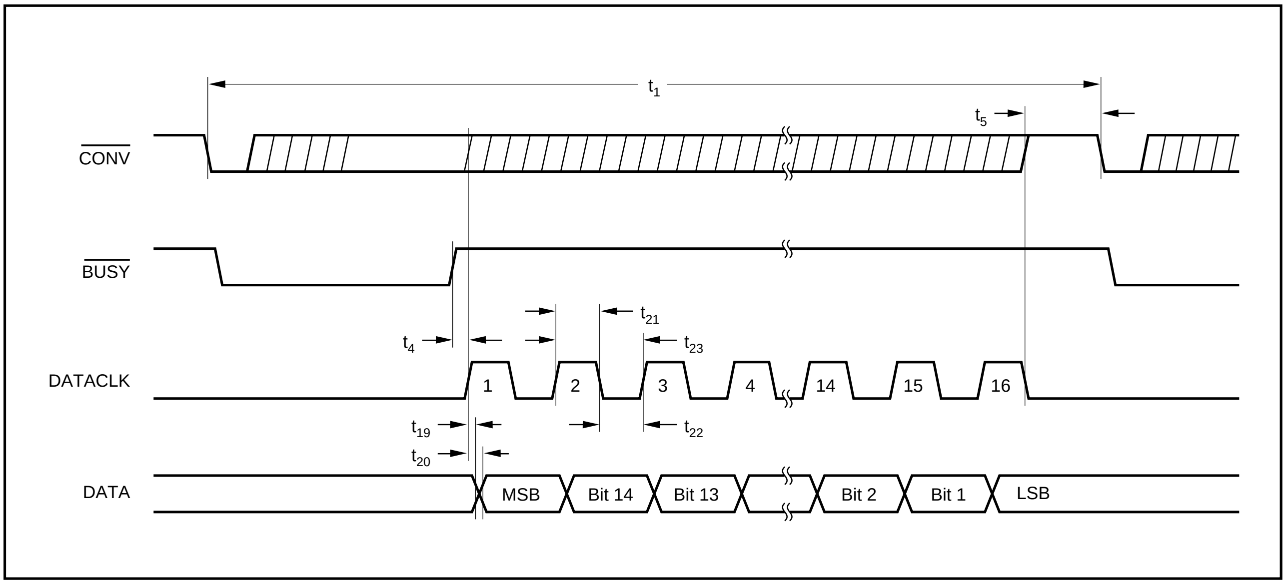


FIGURE 6. Serial Data Timing, External Clock, Clocking After the Conversion Completes (EXT/$\overline{\text{INT}}$ HIGH, $\overline{\text{CS}}$ LOW).

might be possible to use the rising edge of the DATACLK signal. However, one extra clock period (not shown in Figures 6, 7, and 8) is needed for the final bit.

The external DATACLK signal must be LOW or $\overline{CS}$ must be HIGH prior to $\overline{BUSY}$ rising (see time t_{25} in Figures 7 and 8). If this is not observed during this time, the output shift register of the ADS7813 will not be updated with the conversion result. Instead, the previous contents of the shift register will remain and the new result will be lost.

Before reading the next three paragraphs, consult the Sensitivity to External Digital Signals section of this data sheet. This will explain many of the concerns regarding how and when to apply the external DATACLK signal.

External DATACLK Active After the Conversion

The preferred method of obtaining the conversion result is to provide the DATACLK signal after the conversion has been completed and before the next conversion starts—as shown in Figure 6. Note that the DATACLK signal should be static before the start of the next conversion. If this is not observed, the DATACLK signal could affect the voltage that is acquired.

External DATACLK Active During the Next Conversion

Another method of obtaining the conversion result is shown in Figure 7. Since the output shift register is not updated until the end of the conversion, the previous result remains valid during the next conversion. If a fast clock (≥ 2MHz) can be provided to the ADS7813, the result can be read during time t_2. During this time, the noise from the DATACLK signal is less likely to affect the conversion result.

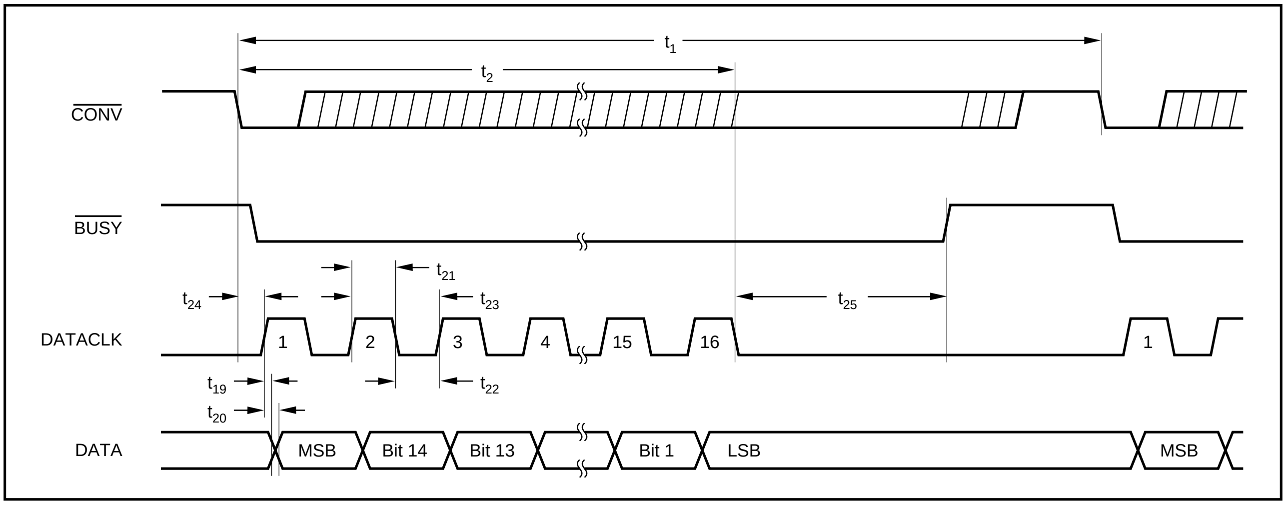


FIGURE 7. Serial Data Timing, External Clock, Clocking During the Next Conversion (EXT/$\overline{INT}$ HIGH, $\overline{CS}$ LOW).

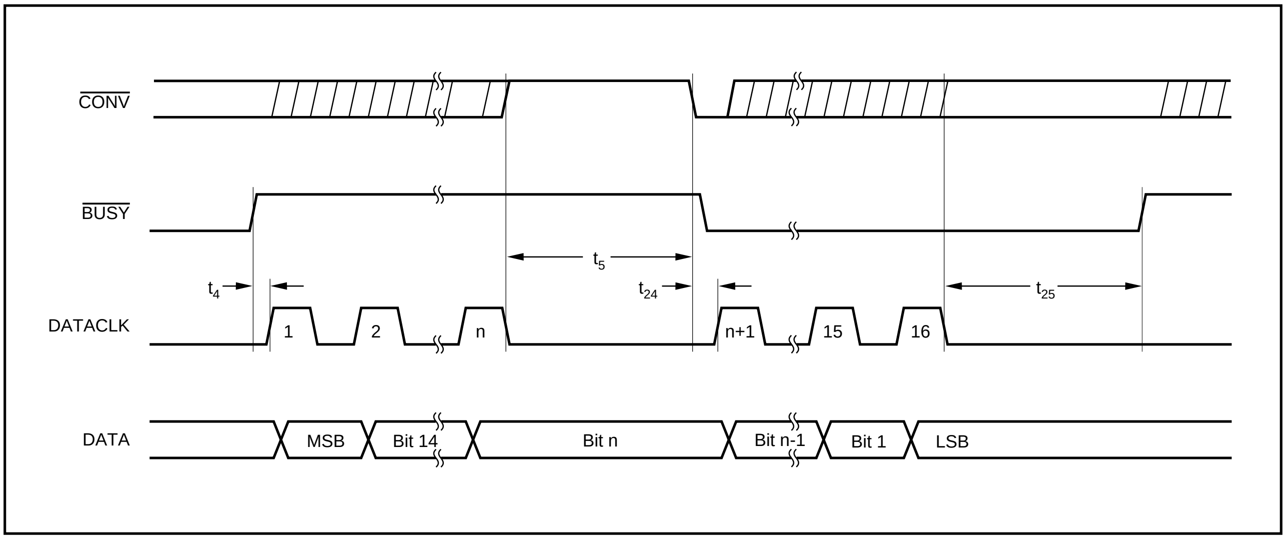


FIGURE 8. Serial Data Timing, External Clock, Clocking After the Conversion Completes and During the Next Conversion (EXT/$\overline{INT}$ HIGH, $\overline{CS}$ LOW).

External DATACLK Active After the Conversion and During the Next Conversion

Figure 8 shows a method that is a hybrid of the two previous approaches. This method works very well for microcontrollers that do serial transfers 8 bits at a time and for slower microcontrollers. For example, if the fastest serial clock that the microcontroller can produce is 1µs, the approach shown in Figure 6 would result in a diminished throughput (26kHz maximum conversion rate). The method described in Figure 7 could not be used without risk of affecting the conversion result (the clock would have to be active after time t_2). The approach in Figure 8 results in an improved throughput rate (33kHz maximum with a 1µs clock) and DATACLK is not active after time t_2.

COMPATIBILITY WITH THE ADS7812

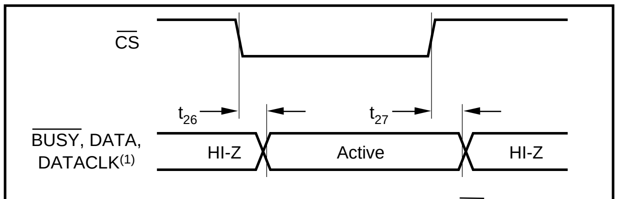
The only difference between the ADS7812 and the ADS7813 is in the internal control logic and the digital interface. Since the ADS7812 is a 12-bit converter, the internal shift register is 12 bits wide. In addition, only 12-bit decisions are made during the conversion. Thus, the ADS7812's conversion time is approximately 75% of the ADS7813's.

In the internal DATACLK mode, the ADS7812 produces 12 DATACLK periods during the conversion instead of the ADS7813's 16 (see Figure 5). In the external DATACLK mode, the ADS7812 can accept 16 clock periods on DATACLK. At the start of the 13th clock cycle, the DATA output will go LOW and remain LOW. Thus, Figures 6, 7, 8, and the associated times in Table II can also be used for the ADS7812, but the last four bits of the conversion result will be zero.

CHIP SELECT ($\overline{\mathrm{CS}}$)

The $\overline{\mathrm{CS}}$ input allows the digital outputs of the ADS7812 to be disabled and gates the external DATACLK signal when EXT/$\overline{\mathrm{INT}}$ is HIGH. See Figure 9 for the enable and disable time associated with $\overline{\mathrm{CS}}$ and Figure 3 for a block diagram of the ADS7813's logic. The digital outputs can be disabled at any time.

Note that a conversion is initiated on the falling edge of $\overline{\mathrm{CONV}}$ even if $\overline{\mathrm{CS}}$ is HIGH. If the EXT/$\overline{\mathrm{INT}}$ input is LOW (internal DATACLK) and $\overline{\mathrm{CS}}$ is HIGH during the entire conversion, the previous conversion result will be lost (the serial transmission occurs but DATA and DATACLK are disabled).



NOTE: (1) DATACLK is an output only when EXT/$\overline{\mathrm{INT}}$ is LOW.

FIGURE 9. Enable and Disable Timing for Digital Outputs.

ANALOG INPUT

The ADS7813 offers a number of input ranges. This is accomplished by connecting the three input resistors to either the analog input (V_{IN}), to ground (GND), or to the 2.5V reference buffer output (BUF). Table I shows the input ranges that are typically used in most data acquisition applications. These ranges are all guaranteed to meet the specifications given in the Specifications table. Table IV contains a complete list of ideal input ranges, associated input connections, and comments regarding the range.

ANALOG INPUT RANGE (V)	CONNECT $R1_{IN}$ TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE (kΩ)	COMMENT
0.3125 to 2.8125	V_{IN}	V_{IN}	V_{IN}	> 10,000	Guaranteed offset and gain
–0.417 to 2.916	V_{IN}	V_{IN}	BUF	26.7	V_{IN} cannot go below GND – 0.3V
0.417 to 3.750	V_{IN}	V_{IN}	GND	26.7	Offset and gain not guaranteed
±3.333	V_{IN}	BUF	V_{IN}	21.3	Guaranteed offset and gain
–15 to 5	V_{IN}	BUF	BUF	45.7	Offset and gain not guaranteed
±10	V_{IN}	BUF	GND	45.7	Guaranteed offset and gain
0.833 to 7.5	V_{IN}	GND	V_{IN}	21.3	Offset and gain not guaranteed
–2.5 to 17.5	V_{IN}	GND	BUF	45.7	Exceeds absolute maximum V_{IN}
2.5 to 22.5	V_{IN}	GND	GND	45.7	Exceeds absolute maximum V_{IN}
0 to 2.857	BUF	V_{IN}	V_{IN}	45.7	Offset and gain not guaranteed
–1 to 3	BUF	V_{IN}	BUF	21.3	V_{IN} cannot go below GND – 0.3V
0 to 4	BUF	V_{IN}	GND	21.3	Guaranteed offset and gain
–6.25 to 3.75	BUF	BUF	V_{IN}	26.7	Offset and gain not guaranteed
0 to 10	BUF	GND	V_{IN}	26.7	Guaranteed offset and gain
0.357 to 3.214	GND	V_{IN}	V_{IN}	45.7	Offset and gain not guaranteed
–0.5 to 3.5	GND	V_{IN}	BUF	21.3	V_{IN} cannot go below GND – 0.3V
0.5 to 4.5	GND	V_{IN}	GND	21.3	Guaranteed offset and gain
±5	GND	BUF	V_{IN}	26.7	Guaranteed offset and gain
1.25 to 11.25	GND	GND	V_{IN}	26.7	Offset and gain not guaranteed

TABLE IV. Complete List of Ideal Input Ranges.

The input impedance results from the various connections and the internal resistor values (refer to the block diagram on the front page of this data sheet). The internal resistor values are typical and can change by ±30%, due to process variations. However, the ratio matching of the resistors is considerably better than this. Thus, the input range will vary only a few tenths of a percent from part to part, while the input impedance can vary up to ±30%.

The Specifications table contains the maximum limits for the variation of the analog input range, but only for those ranges where the comment field shows that the offset and gain are guaranteed (this includes all the ranges listed in Table I). For the other ranges, the offset and gain are not tested and are not guaranteed.

Five of the input ranges in Table IV are not recommended for general use. The upper-end of the –2.5V to 17.5V range and 2.5V to 22.5V range exceed the absolute maximum analog input voltage. These ranges can still be used as long as the input voltage remains under the absolute maximum, but this will moderately to significantly reduce the full-scale range of the converter.

Likewise, three of the input ranges involve the connection at $R2_{IN}$ being driven below GND. This input has a reverse-biased ESD protection diode connection to ground. If $R2_{IN}$ is taken below GND – 0.3V, this diode will be forward-biased and will clamp the negative input at –0.4V to –0.7V, depending on the temperature. Since the negative full-scale value of these input ranges exceed –0.4V, they are not recommended.

Note that Table IV assumes that the voltage at the REF pin is 2.5V. This is true if the internal reference is being used or if the external reference is 2.5V. Other reference voltages will change the values in Table IV.

HIGH IMPEDANCE MODE

When $R1_{IN}$, $R2_{IN}$, and $R3_{IN}$ are connected to the analog input, the input range of the ADS7813 is 0.3125V to 2.8125V and the input impedance is greater than 10MΩ. This input range can be used to connect the ADS7813 directly to a wide variety of sensors. Figure 10 shows the impedance of the sensor versus the change in ILE and DLE of the ADS7813. The performance of the ADS7813 can be improved for higher sensor impedance by allowing more time for acquisition. For example, 10µs of acquisition time will approximately double sensor impedance for the same ILE/DLE performance.

The input impedance and capacitance of the ADS7813 are very stable with temperature. Assuming that this is true of the sensor as well, the graph shown in Figure 10 will vary less than a few percent over the guaranteed temperature range of the ADS7813. If the sensor impedance varies significantly with temperature, the worst-case impedance should be used.

DRIVING THE ADS7813 ANALOG INPUT

In general, any “reasonably fast”, high quality operational or instrumentation amplifier can be used to drive the ADS7813 input. When the converter enters the acquisition mode, there is some charge injection from the converter’s input to the amplifier’s output. This can result in inadequate settling time with slower amplifiers. Be very careful with single-supply amplifiers, particularly if their output will be required to swing very close to the supply rails.

In addition, be careful in regards to the amplifier’s linearity. The outputs of single-supply and “rail-to-rail” amplifiers can saturate as they approach the supply rails. Rather than the amplifier’s transfer function being a straight line, the curve can become severely ‘S’ shaped. Also, watch for the point where the amplifier switches from sourcing current to sinking current. For some amplifiers, the transfer function can be noticeably discontinuous at this point, causing a significant change in the output voltage for a much smaller change on the input.

Burr-Brown manufactures a wide variety of operational and instrumentation amplifiers that can be used to drive the input of the ADS7813. These include the OPA627, OPA132, and INA110.

REFERENCE

The ADS7813 can be operated with its internal 2.5V reference or an external reference. By applying an external reference voltage to the REF pin, the internal reference voltage is overdriven. The voltage at the REF input is internally buffered by a unity gain buffer. The output of this buffer is present at the BUF and CAP pins.

REF

The REF pin is the output of the internal 2.5V reference or the input for an external reference. A 1µF to 2.2µF tantulum capacitor should be connected between this pin and ground. The capacitor should be placed as close to the ADS7813 as possible.

When using the internal reference, the REF pin should not be connected to any type of significant load. An external load will cause a voltage drop across the internal 4kΩ resistor that is in series with the internal reference. Even a

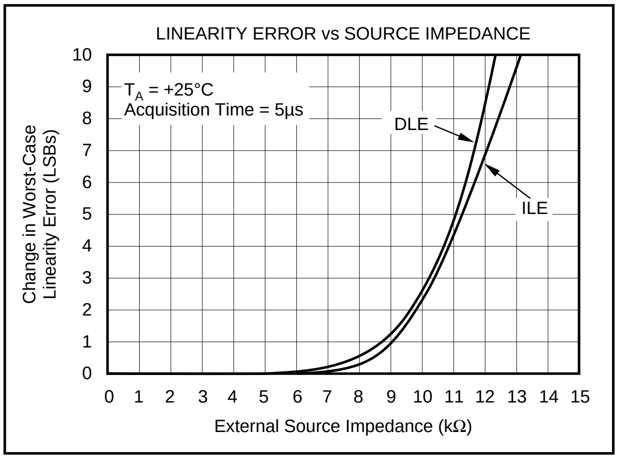


FIGURE 10. Linearity Error vs Source Impedance in the High Impedance Mode ($R1_{IN} = R2_{IN} = R3_{IN} = V_{IN}$).

40MΩ external load to ground will cause a decrease in the full-scale range of the converter by 6 LSBs.

The range for the external reference is 2.3V to 2.7V. The voltage on REF determines the full-scale range of the converter and the corresponding LSB size. Increasing the reference voltage will increase the LSB size in relation to the internal noise sources which, in turn, can improve signal-to-noise ratio. Likewise, decreasing the reference voltage will reduce the LSB size and signal-to-noise ratio.

CAP

The CAP pin is used to compensate the internal reference buffer. A 1µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor should be connected between this pin and ground, with the ceramic capacitor placed as close to the ADS7813 as possible. The total value of the capacitance on the CAP pin is critical to optimum performance of the ADS7813. A value larger than 2.0µF could overcompensate the buffer while a value lower than 0.5µF may not provide adequate compensation.

BUF

The voltage on the BUF pin is the output of the internal reference buffer. This pin is used to provide +2.5V to the analog input or inputs for the various input configurations.

The BUF output can provide up to 1mA of current to an external load. The load should be constant as a variable load could affect the conversion result by modulating the BUF voltage. Also note that the BUF output will show significant glitches as each bit decision is made during a conversion. Between conversions, the BUF output is quiet.

POWER DOWN

The ADS7813 has a power-down mode that is activated by taking $\overline{\text{CONV}}$ LOW and then PWRD HIGH. This will power down all of the analog circuitry including the reference, reducing power dissipation to under 50µW. To exit the power-down mode, $\overline{\text{CONV}}$ is taken HIGH and then PWRD is taken LOW. Note that a conversion will be initiated if PWRD is taken HIGH while $\overline{\text{CONV}}$ is LOW.

While in the power-down mode, the voltage on the capacitors connected to CAP and REF will begin to leak off. The voltage on the CAP capacitor leaks off much more rapidly than on the REF capacitor (the REF input of the ADS7813 becomes high-impedance when PWDN is HIGH—this is not true for the CAP input). When the power-down mode is exited, these capacitors must be allowed to recharge and settle to a 16-bit level. Figure 11 shows the amount of time typically required to obtain a valid 16-bit result based on the amount of time spent in power down (at room temperature). This figure assumes that the total capacitance on the CAP pin is 1.01µF.

Figure 12 provides a circuit which can significantly reduce the power up time if the power down time will be fairly brief (a few seconds or less). A low on-resistance MOSFET is used to disconnect the capacitance on the CAP pin from the leakage paths internal to the ADS7813. This allows the capacitors to retain their charge for a much longer period of time, reducing the time required to recharge them at power up. With this circuit, the power down time can be extended to tens or hundreds of milliseconds with almost instantaneous power up.

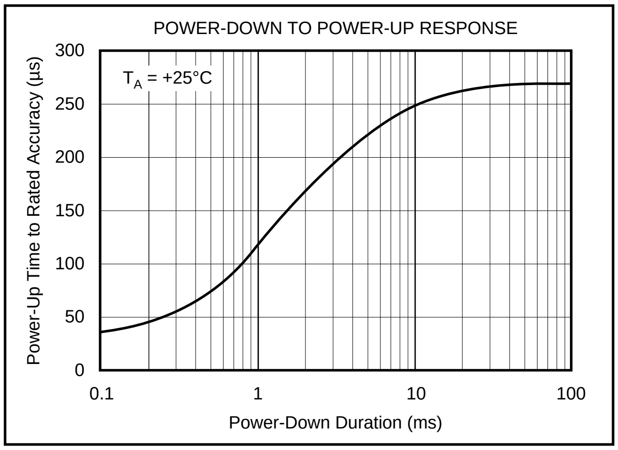


FIGURE 11. Power-Down to Power-Up Response.

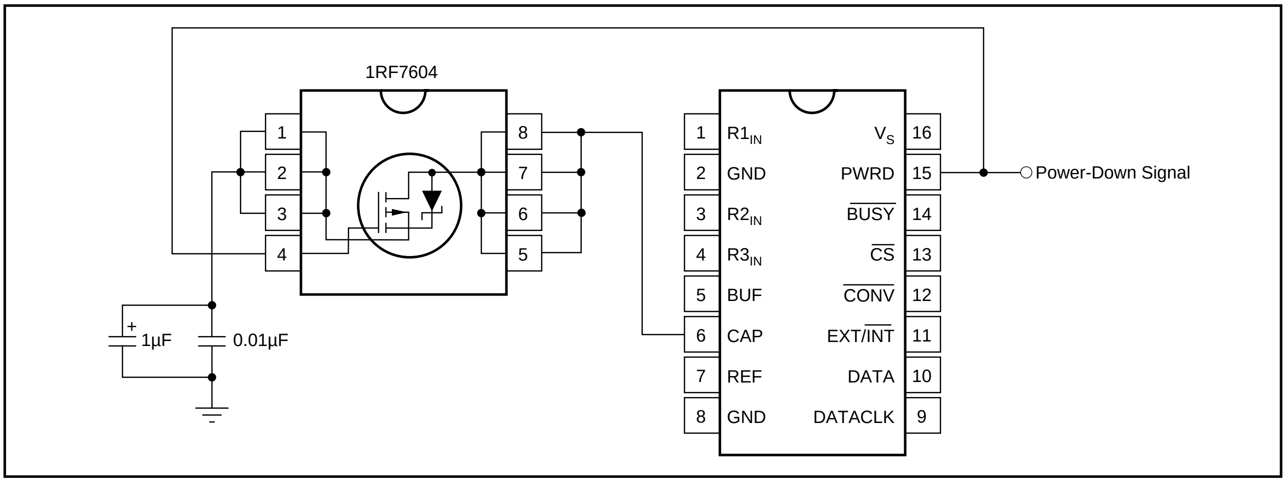


FIGURE 12. Improved Power-Up Response Circuit.

LAYOUT

The ADS7813 should be treated as a precision analog component and should reside completely on the “analog” portion of the printed circuit board. Ideally, a ground plane should extend underneath the ADS7813 and under all other analog components. This plane should be separate from the digital ground until they are joined at the power supply connection. This will help prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

The +5V power should be clean, well-regulated, and separate from the +5V power for the digital portion of the design. One possibility is to derive the +5V supply from a linear regulator located near the ADS7813. If derived from the digital +5V power, a 5Ω to 10Ω resistor should be placed in series with the power connection from the digital supply. It may also be necessary to increase the bypass capacitance near the V_S pin (an additional 100µF or greater capacitor in parallel with the 10µF and 0.1µF capacitors). For designs with a large number of digital components or very high speed digital logic, this simple power supply filtering scheme may not be adequate.

SENSITIVITY TO EXTERNAL DIGITAL SIGNALS

All successive approximation register based A/D converters are sensitive to external sources of noise. The reason for this will be explained in the following paragraphs. For the ADS7813 and similar A/D converters, this noise most often originates due to the transition of external digital signals. While digital signals that run near the converter can be the source of the noise, the biggest problem occurs with the digital inputs to the converter itself.

In many cases, the system designer may not be aware that there is a problem or a potential for a problem. For a 12-bit system, these problems typically occur at the least significant bits and only at certain places in the converter’s transfer function. For a 16-bit converter, the problem can be much easier to spot.

For example, the timing diagram in Figure 2 shows that the $\overline{\text{CONV}}$ signal should return HIGH sometime during time t_2. In fact, the $\overline{\text{CONV}}$ signal can return HIGH at any time during the conversion. However, after time t_2, the transition of the $\overline{\text{CONV}}$ signal has the potential of creating a good deal of noise on the ADS7813 die. If this transition occurs at just precisely the wrong time, the conversion results could be affected. In a similar manner, transitions on the DATACLK input could affect the conversion result.

For the ADS7813, there are 16 separate bit decisions which are made during the conversion. The most significant bit decision is made first, proceeding to the least significant bit at the end of the conversion. Each bit decision involves the assumption that the bit being tested should be set. This is combined with the result that has been achieved so far. The converter compares this combined result with the actual input voltage. If the combined result is too high, the bit is cleared. If the result is equal to or lower than the actual input voltage, the bit remains HIGH. This is why the basic architecture is referred to as “successive approximation register.”

If the result so far is getting very close to the actual input voltage, then the comparison involves two voltages which are very close together. The ADS7813 has been designed so that the internal noise sources are a minimum just prior to the comparator result being latched. However, if a external digital signal transitions at this time, a great deal of noise will be coupled into the sensitive analog section of the ADS7813. Even if this noise produces a difference between the two voltages of only 2mV, the conversion result will be off by 52 counts or least significant bits (LSBs). (The internal LSB size of the ADS7813 is 38µV regardless of the input range.)

Once a digital transition has caused the comparator to make a wrong bit decision, the decision cannot be corrected (unless some type of error correction is employed). All subsequent bit decisions will then be wrong. Figure 13 shows a successive approximation process that has gone wrong. The dashed line represents what the correct bit decisions should have been. The solid line represents the actual result of the conversion.

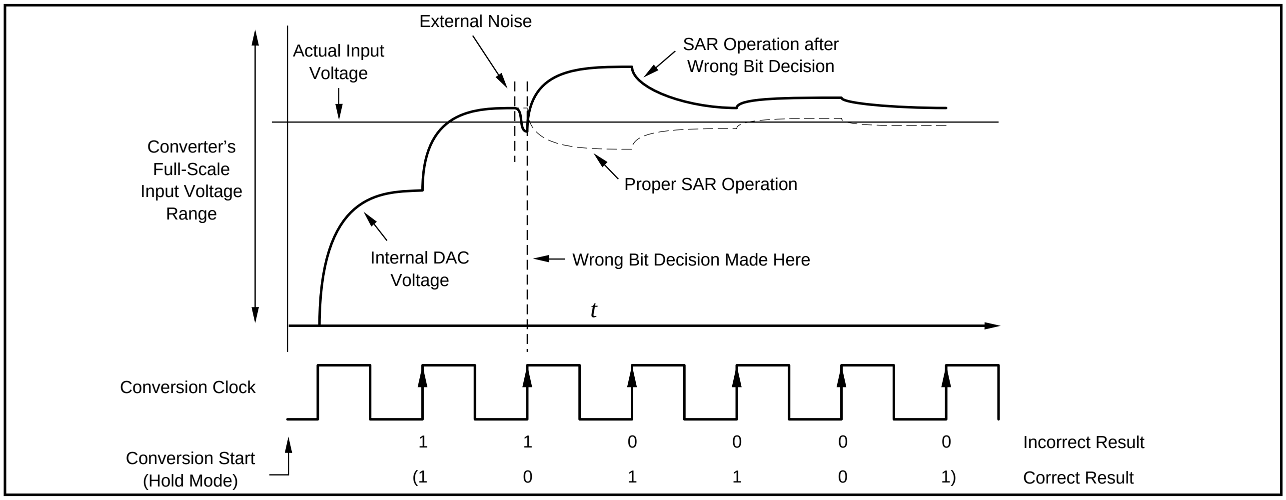


FIGURE 13. SAR Operation When External Noise Affects the Conversion.

Keep in mind that the time period when the comparator is most sensitive to noise is fairly small. Also, the peak portion of the noise "event" produced by a digital transition is fairly brief as most digital signals transition in a few nanoseconds. The subsequent noise may last for a period of time longer than this and may induce further effects which require a longer settling time. However, in general, the event is over within a few tens of nanoseconds.

For the ADS7813, error correction is done when the tenth bit is decided. During this bit decision, it is possible to correct limited errors that may have occurred during previous bit decisions. However, after the tenth bit, no such correction is possible. Note that for the timing diagrams shown in Figures 2, 5, 6, 7, and 8, all external digital signals should remain static from 8µs after the start of a conversion until $\overline{\text{BUSY}}$ rises. The tenth bit is decided approximately 10µs to 11µs into the conversion.

APPLICATIONS INFORMATION

TRANSITION NOISE

If a low-noise DC input is applied to the ADS7813 and 1,000 conversions are performed, the digital output of the converter will vary slightly in output codes. This is true for all 16-bit SAR converters. The transition noise specification found in the Specifications section is a statistical figure which represents the one sigma limit of these output codes.

Using a histogram to plot the number of occurances of each output code, the distribution should appear bell-shaped with the peak of the curve representing the nominal output code for the given input voltage. The $\pm 1\sigma$, $\pm 2\sigma$, and $\pm 3\sigma$ limits around this nominal code should contain 68.3%, 95.5%, and 99.7%, respectively, of the conversion results. As a rough approximation, multiplying transition noise by 6 ($\pm 3\sigma$) will yield the number of unique output codes which should be present in 1,000 conversions.

The ADS7813 has a transition noise figure of 0.6LSB, yielding approximately 4 different output codes for 1,000 conversions. However, since $\pm 3\sigma$ is only 99.7%, up to three conversions have some chance of being outside this range. In addition, the differential linearity error of each code and the quantization performed by the converter result in histograms which can deviate from the ideal. Figure 14 shows a histogram of 5,000 conversions from the ADS7813.

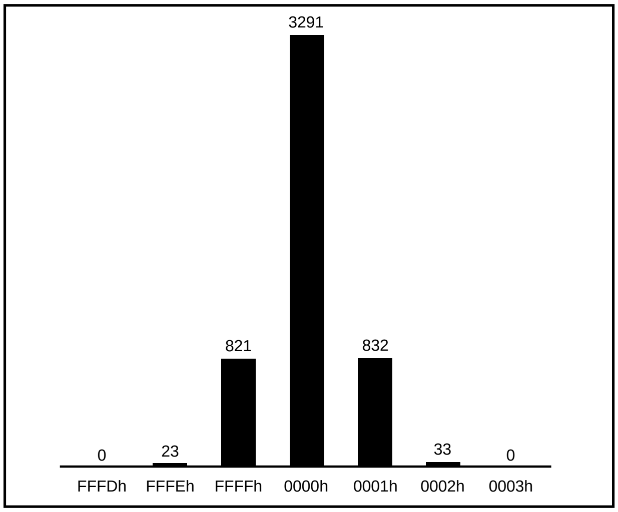


FIGURE 14. Histogram of 5,000 Conversions with Input Grounded.

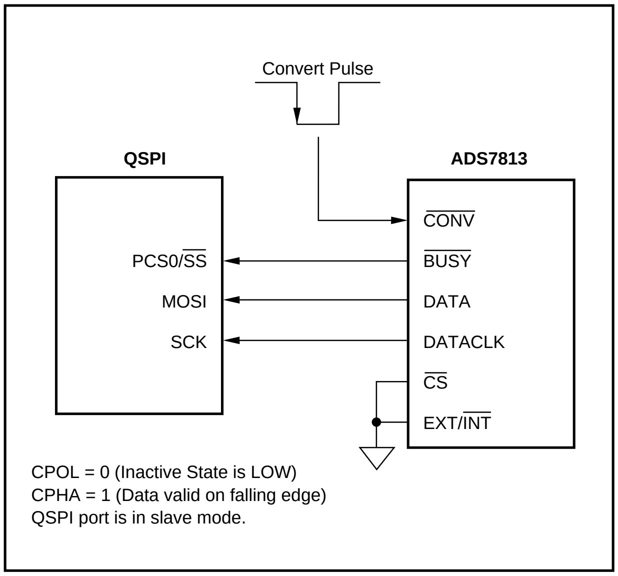
AVERAGING

The noise of the converter can be reduced by averaging conversion results. The noise will be reduced by a factor of $1/\sqrt{n}$, where 'n' is the number of averages. For example, averaging four conversions will reduce transition noise by half, to 0.3LSBs. Averaging should only be used for low-frequency signals.

For higher frequency signals, a digital filter can be used to reduce noise. This works in a similar manner to averaging: for every reduction in the signal bandwidth by two, the signal-to-noise ratio will improve by 3dB.

QSPI INTERFACING

Figure 15 shows a simple interface between the ADS7813 and any queued serial peripheral interface (QSPI) equipped microcontroller (available on several Motorola devices). This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS7813 is the only serial peripheral.



CPOL = 0 (Inactive State is LOW)
CPHA = 1 (Data valid on falling edge)
QSPI port is in slave mode.

FIGURE 15. QSPI Interface to the ADS7813.

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select ($\overline{\text{SS}}$) line. When a LOW to HIGH transition occurs (indicating the end of a conversion), the port can be enabled. If this is not done, the microcontroller and A/D converter may not be properly synchronized. (The slave select line simply enables communication—it does not indicate the start or end of a serial transfer.)

Figure 16 shows a QSPI-equipped microcontroller interfacing to three ADS7813s. There are many possible variations to this interface scheme. As shown, the QSPI port produces a common $\overline{\text{CONV}}$ signal which initiates a conversion on all three converters. After the conversions are finished, each result is transferred in turn. The QSPI port is completely programmable to handle the timing and transfers without processor intervention. If the $\overline{\text{CONV}}$ signal is generated in this way, it should be possible to make both AC and DC measurements with the ADS7813, as the $\overline{\text{CONV}}$ signal will have low jitter. Note that if the $\overline{\text{CONV}}$ signal is generated via software commands, it will have a good deal of jitter and only low frequency (DC) measurements can be made.

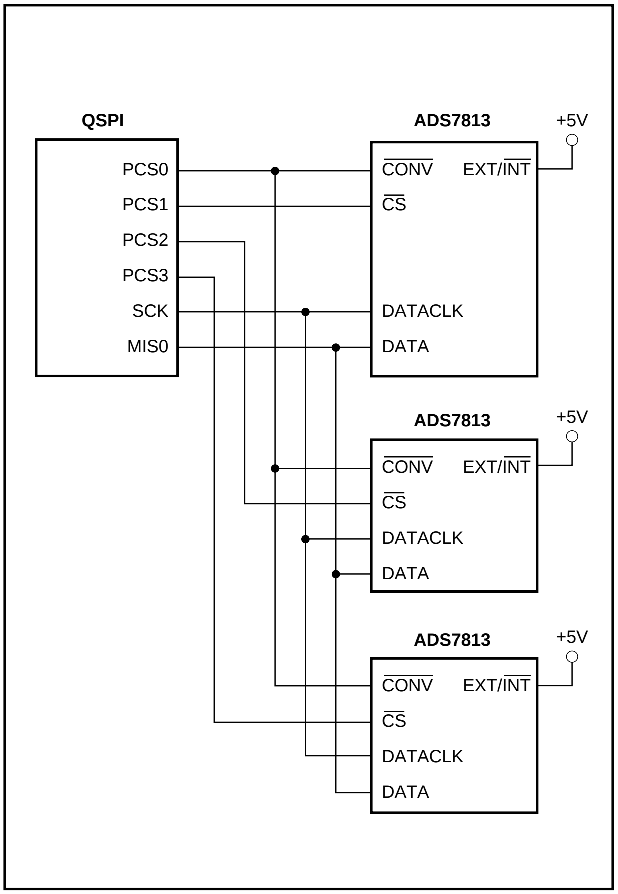


FIGURE 16. QSPI Interface to Three ADS7813s.

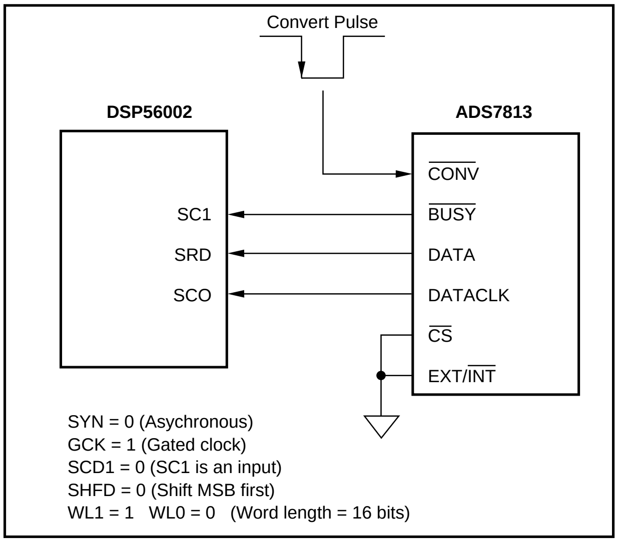
SPI INTERFACING

The serial peripheral interface (SPI) is directly related to the QSPI and both Figures 15 and 16 can be used as a guide for connecting the ADS7813 to SPI-equipped microcontrollers. For most microcontrollers, the SPI port is capable of 8-bit transfers only. In the case of Figure 15, be aware that the microcontroller may have to be capable of fetching the 8 most significant bits before they are overwritten by the 8 least significant bits.

DSP56002 INTERFACING

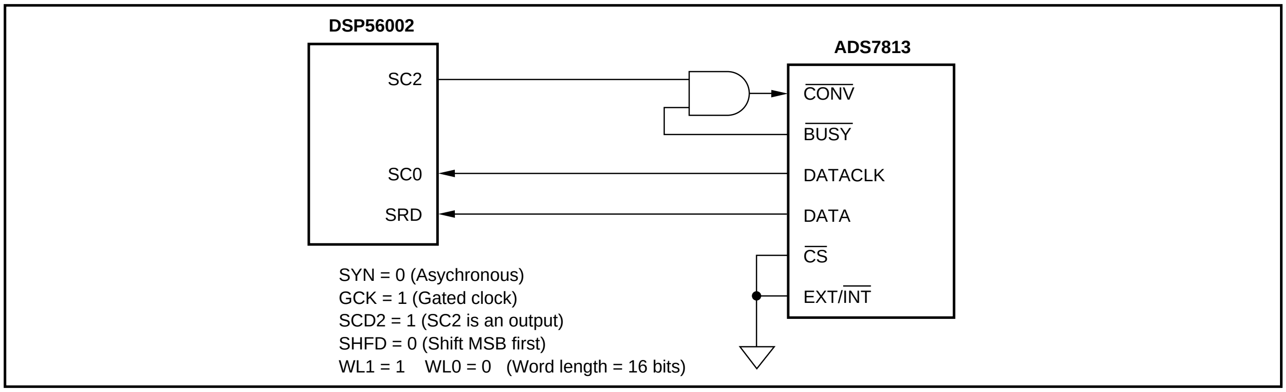
The DSP56002 serial interface has an SPI compatibility mode with some enhancements. Figure 17 shows an interface between the ADS7813 and the DSP56002. As with the QSPI interface of Figure 15, the DSP56002 must be programmed to enable the serial interface when a LOW to HIGH transition on SCI occurs.

The DSP56002 can also provide the $\overline{\text{CONV}}$ signal, as shown in Figure 18. The receive and transmit sections of the interface are decoupled (asynchronous mode) and the transmit section is set to generate a word length frame sync every other transmit frame (frame rate divider set to 2). The prescale modulus should be set to produce a transmit frame at twice the desired conversion rate.



SYN = 0 (Asychronous)
GCK = 1 (Gated clock)
SCD1 = 0 (SC1 is an input)
SHFD = 0 (Shift MSB first)
WL1 = 1 WL0 = 0 (Word length = 16 bits)

FIGURE 17. DSP56002 Interface to the ADS7813.



SYN = 0 (Asychronous)
GCK = 1 (Gated clock)
SCD2 = 1 (SC2 is an output)
SHFD = 0 (Shift MSB first)
WL1 = 1 WL0 = 0 (Word length = 16 bits)

FIGURE 18. DSP56002 Interface to the ADS7813. Processor Initiates Conversions.