



**DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED PAIR MOSFET**

**GENERAL DESCRIPTION**

The ALD1105 is a monolithic dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1116 N-channel MOSFET pair and an ALD1117 P-channel MOSFET pair in one package. The ALD1105 is a low drain current, low leakage current version of the ALD1103.

The ALD1105 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +1V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in complementary pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1105 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1105 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the field effect transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA at 25°C is  $= 3\text{mA}/30\text{pA} = 100,000,000$ .

**FEATURES**

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETs
- Low input capacitance
- Low Vos -- 10mV
- High input impedance --  $10^{13}\Omega$  typical
- Low input and output leakage currents
- Negative current ( $I_{DS}$ ) temperature coefficient
- Enhancement mode (normally off)
- DC current gain  $10^9$
- Matched N-channel pair and matched P-channel pair in one package

**ORDERING INFORMATION**

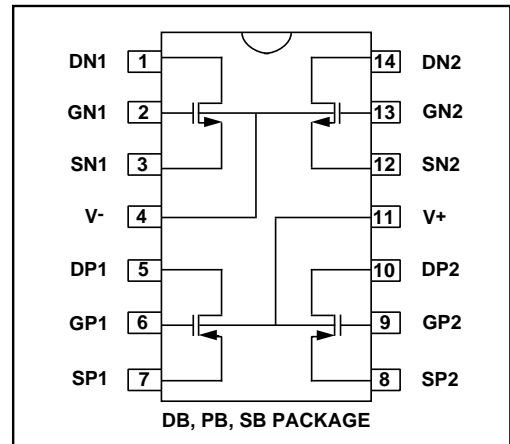
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1105 DB	ALD1105 PB	ALD1105 SB

\* Contact factory for industrial temperature range.

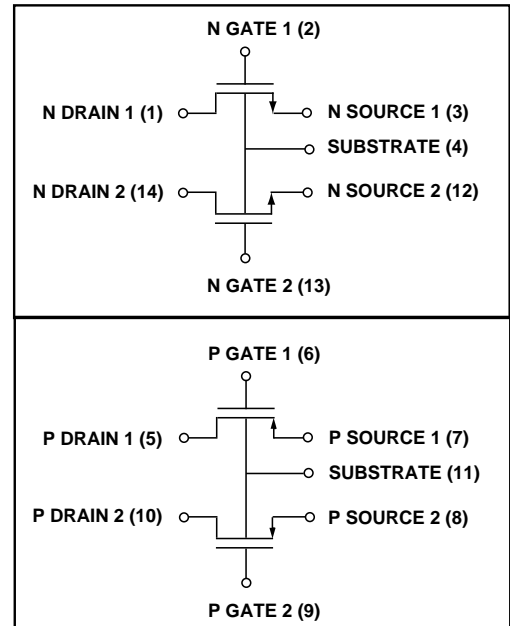
**APPLICATIONS**

- Precision current mirrors
- Complementary push-pull linear drives
- Discrete Analog switches
- Analog signal Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources

**PIN CONFIGURATION**



**BLOCK DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, $V_{DS}$	_____	13.2V
Gate-source voltage, $V_{GS}$	_____	13.2V
Power dissipation	_____	500 mW
Operating temperature range	PB, SB package _____	0°C to +70°C
	DB package _____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

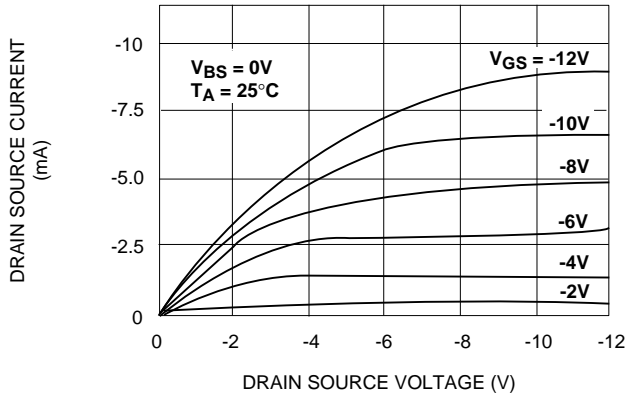
## OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise specified

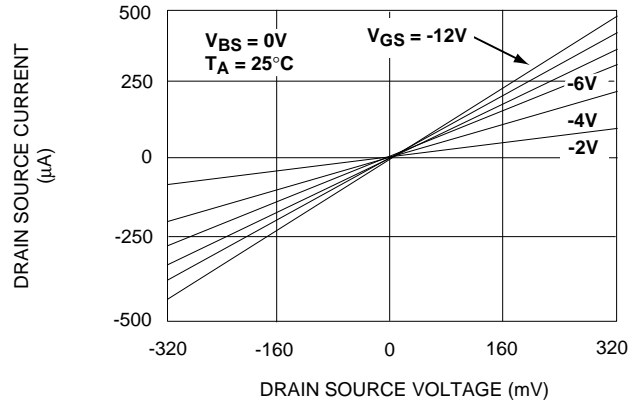
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	$V_T$	0.4	0.7	1.0	V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = V_{DS}$	-0.4	-0.7	-1.0	V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = V_{DS}$
Offset Voltage $V_{GS1} - V_{GS2}$	$V_{OS}$		2	10	mV	$I_{DS} = 10\mu\text{A}$ $V_{GS} = V_{DS}$		2	10	mV	$I_{DS} = -10\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift	$TC_{VT}$		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	3	4.8		mA	$V_{GS} = V_{DS} = 5\text{V}$	-1.3	-2		mA	$V_{GS} = V_{DS} = -5\text{V}$
Trans-conductance	$G_{fs}$	1	1.8		mmho	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$	0.25	0.67		mmho	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Mismatch	$\Delta G_{fs}$		0.5		%			0.5		%	
Output Conductance	$G_{OS}$		200		$\mu\text{mho}$	$V_{DS} = 5\text{V}$ $I_{DS} = 10\text{mA}$		40		$\mu\text{mho}$	$V_{DS} = -5\text{V}$ $I_{DS} = -10\text{mA}$
Drain Source ON Resistance	$R_{DS(ON)}$		350	500	$\Omega$	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		1200	1800	$\Omega$	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	$V_{DS} = 0.1\text{V}$ $V_{GS} = 5\text{V}$		0.5		%	$V_{DS} = -0.1\text{V}$ $V_{GS} = -5\text{V}$
Drain Source Breakdown Voltage	$BV_{DSS}$	12			V	$I_{DS} = 1\mu\text{A}$ $V_{GS} = 0\text{V}$	-12			V	$I_{DS} = -1\mu\text{A}$ $V_{GS} = 0\text{V}$
Off Drain Current	$I_{DS(OFF)}$		10	400	pA nA	$V_{DS} = 12\text{V}$ $I_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$		10	400	pA nA	$V_{DS} = -12\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	$I_{GSS}$		0.1	30	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = 12\text{V}$ $T_A = 125^\circ\text{C}$		1	30	pA nA	$V_{DS} = 0\text{V}$ $V_{GS} = -12\text{V}$ $T_A = 125^\circ\text{C}$
Input Capacitance	$C_{ISS}$		1	3	pF			1	3	pF	

# P- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

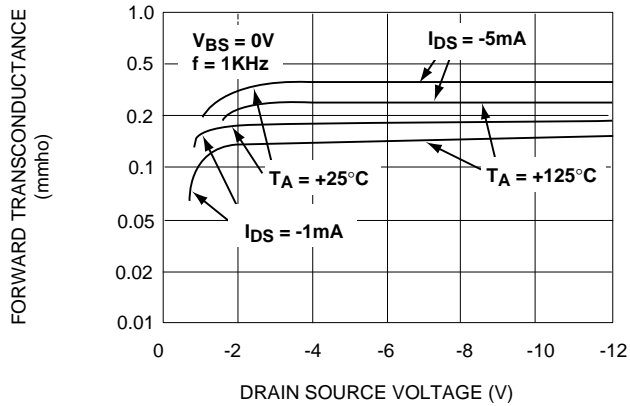
## OUTPUT CHARACTERISTICS



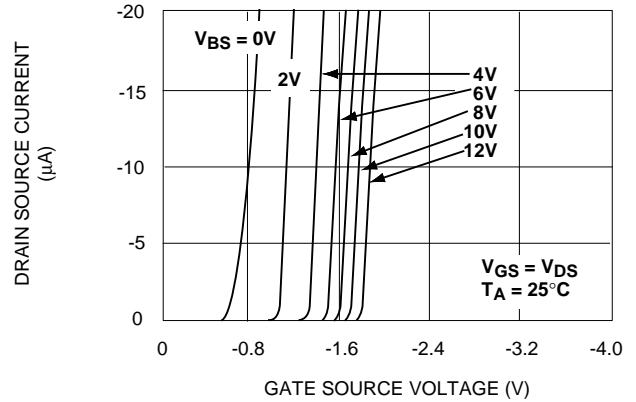
## LOW VOLTAGE OUTPUT CHARACTERISTICS



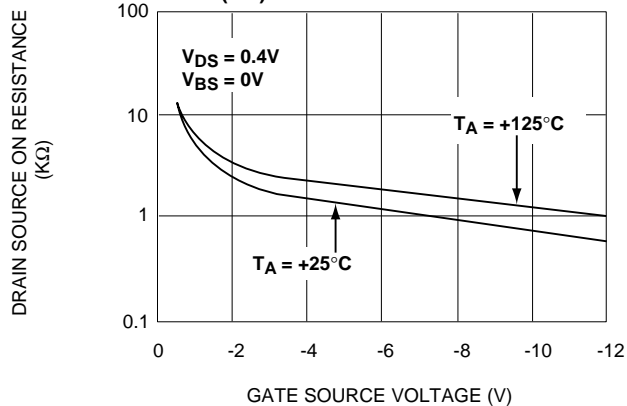
## FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



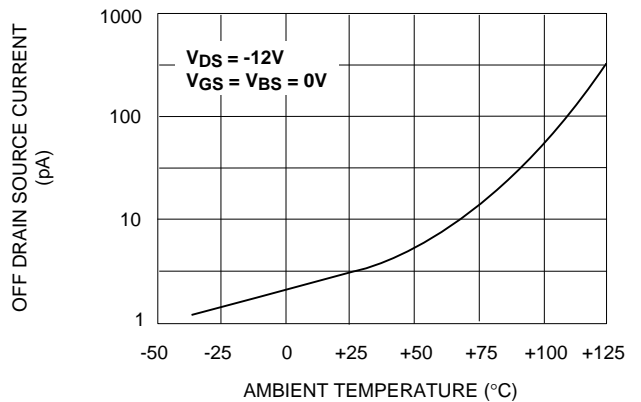
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## DRAIN SOURCE ON RESISTANCE RDS (ON) vs. GATE SOURCE VOLTAGE

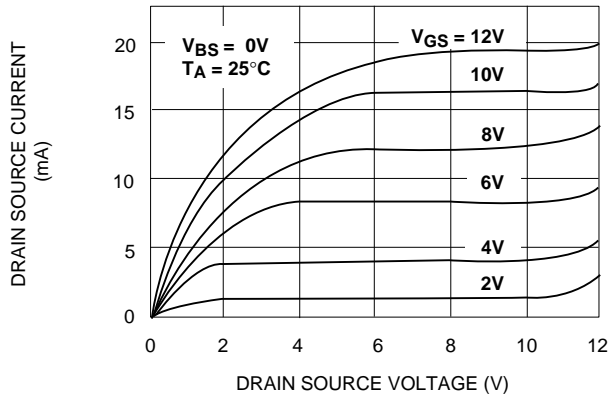


## OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

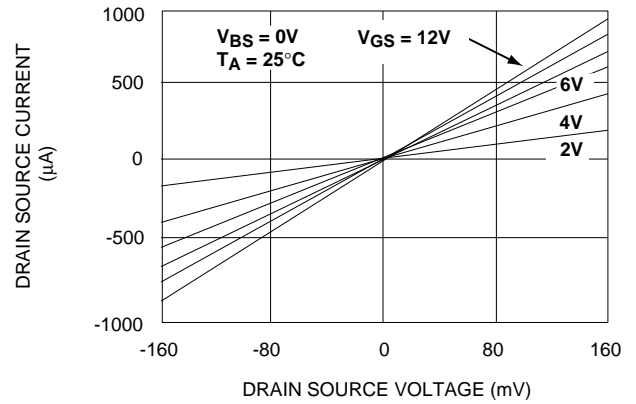


# N- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

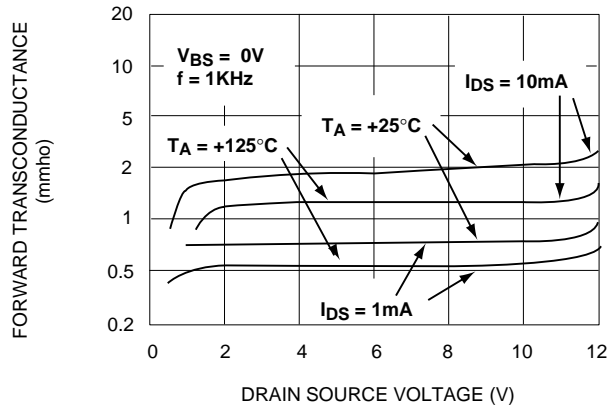
## OUTPUT CHARACTERISTICS



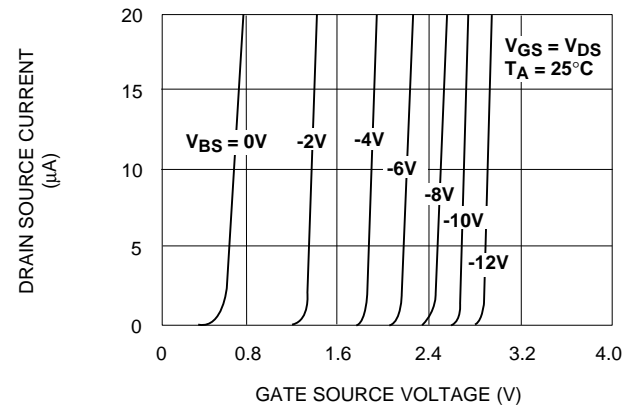
## LOW VOLTAGE OUTPUT CHARACTERISTICS



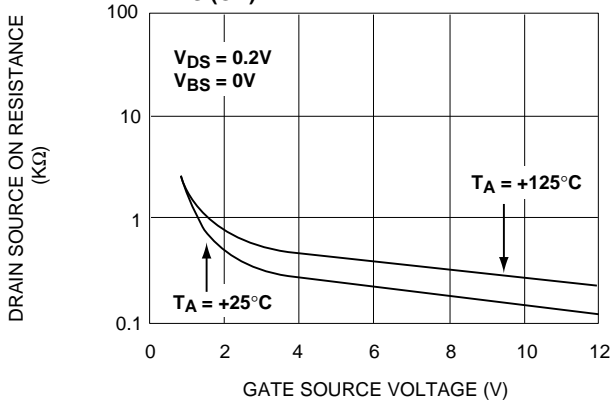
## FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



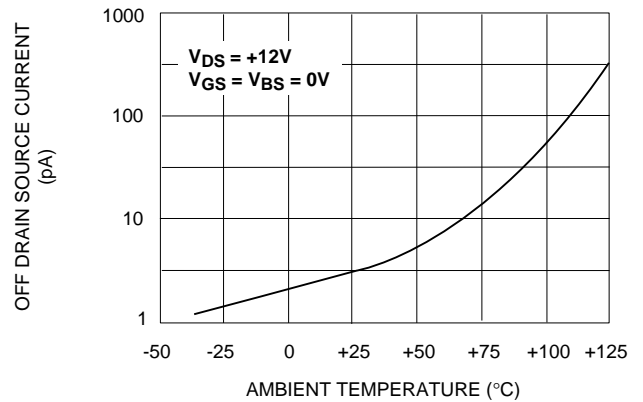
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## DRAIN SOURCE ON RESISTANCE $R_{DS(ON)}$ vs. GATE SOURCE VOLTAGE

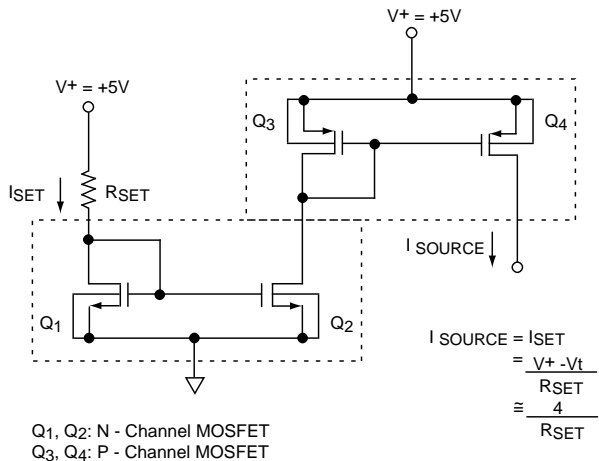


## OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

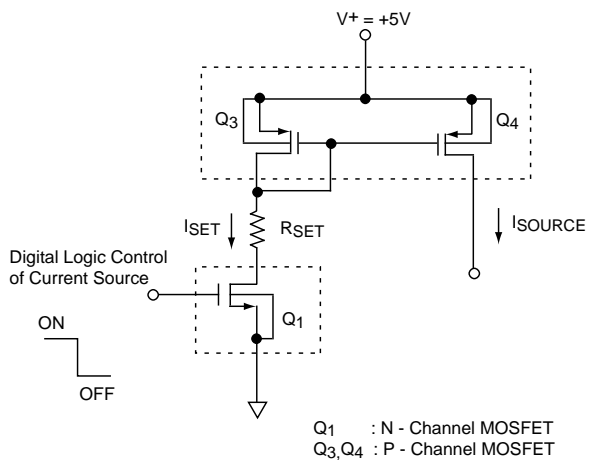


# TYPICAL APPLICATIONS

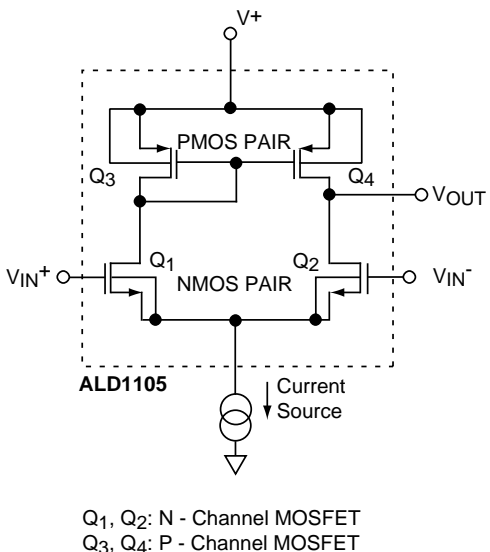
## CURRENT SOURCE MIRROR



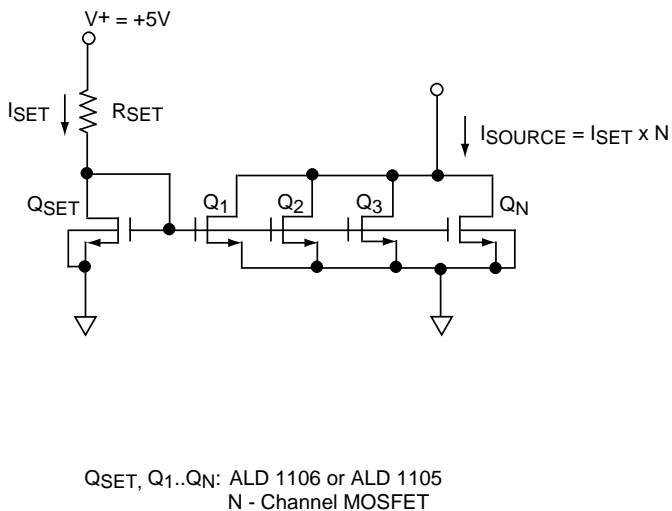
## CURRENT SOURCE WITH GATE CONTROL



## DIFFERENTIAL AMPLIFIER



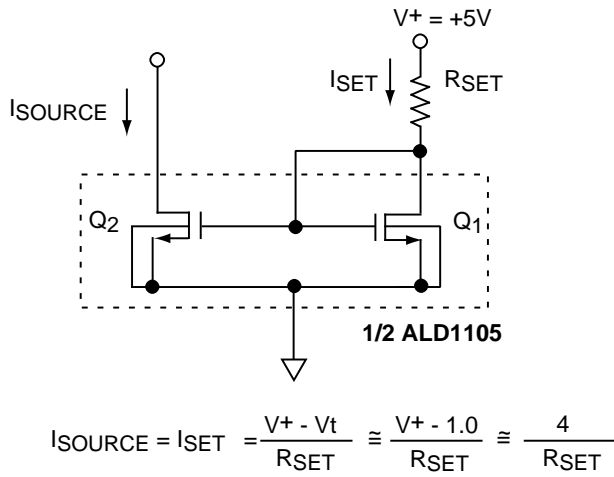
## CURRENT SOURCE MULTIPLICATION



# TYPICAL APPLICATIONS

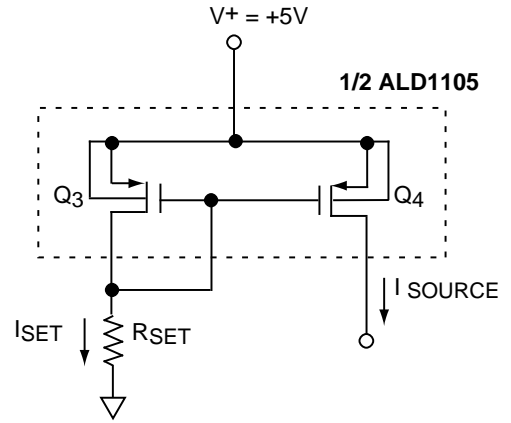
## BASIC CURRENT SOURCES

N- CHANNEL CURRENT SOURCE



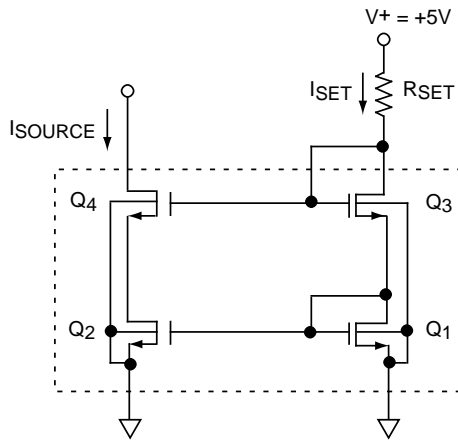
Q1, Q2 : N - Channel MOSFET

P- CHANNEL CURRENT SOURCE

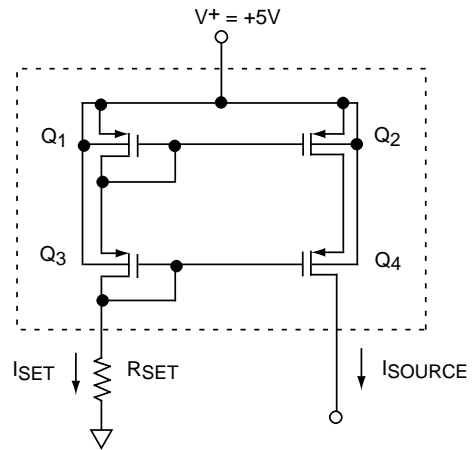


Q3, Q4: P - Channel MOSFET

## CASCODE CURRENT SOURCES



Q1, Q2, Q3, Q4: N - Channel MOSFET  
(1/2 ALD1105 + ALD1116)



$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2V_t}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET  
(1/2 ALD1105 + ALD1117)