



5V RAIL-TO-RAIL PRECISION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD1702/ALD1703 is a monolithic operational amplifier intended primarily for a wide range of analog applications in +5V single power supply and $\pm 5V$ dual power supply systems as well as +4V to +12V battery operated systems. All device characteristics are specified for +5V single supply or $\pm 2.5V$ dual supply systems. It is manufactured with Advanced Linear Devices' enhanced AC MOS silicon gate CMOS process.

The device is designed to offer a balanced trade-off of performance parameters providing a wide range of desired specifications. It offers the industry pin configuration of $\mu A741$ and ICL7611 types.

The ALD1702/ALD1703 has been developed specifically with the 5V single supply or ± 2.5 dual supply user in mind. Several important characteristics of the device make many applications easy to implement for these supply voltages. First, the operational amplifier can operate with rail to rail input and output voltages. This feature allows numerous analog serial stages to be implemented without losing operating voltage margin. Secondly, the device was designed to accommodate mixed applications where digital and analog circuits may work off the same 5V power supply. Thirdly, the output stage can drive up to 400pF capacitive and 5K Ω resistive loads in non-inverting unity gain connection and double the capacitance in the inverting unity gain mode.

These features, coupled with extremely low input currents, high voltage gain, useful bandwidth of 1.5MHz, slew rate of 2.1V/ μs , low power dissipation, low offset voltage and temperature drift, make the ALD1702/ALD1703 a truly versatile, user friendly, operational amplifier.

The ALD1702/ALD1703 is designed and fabricated with silicon gate CMOS technology, and offers 1pA typical input bias current. On-chip offset voltage trimming allows the device to be used without nulling in most applications. The device offers typical offset drift of less than 7 $\mu V/^{\circ}C$ which eliminates many trim or temperature compensation circuits. For precision applications, the ALD1702 is designed to settle to 0.01% in 8 μs .

FEATURES

- Rail-to-rail input and output voltage ranges
- All parameters specified for +5V single supply or $\pm 2.5V$ dual supply systems.
- High load capacitance capability -- 4000pF typical
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 1.0pA typical (30pA max.)
- Ideal for high source impedance applications
- Dual power supply $\pm 2.5V$ to $\pm 5.0V$ operation
- Single power supply +5V to +12V operation
- High voltage gain -- typically 85V/mV @ $\pm 2.5V$ and 250V/mV @ $\pm 5.0V$
- Drive as low as 2K Ω load with 5mA drive current
- Output short circuit protected
- Unity gain bandwidth of 1.5MHz (1.0MHz min.)
- Slew rate of 2.1V/ μs (1.4V/ μs min.)
- Low power dissipation

APPLICATIONS

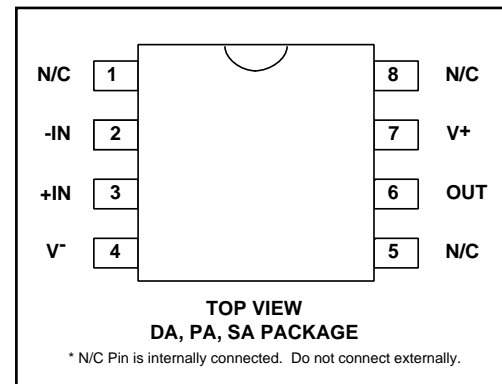
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter
- Coaxial cable driver

ORDERING INFORMATION

| Operating Temperature Range | | |
|-------------------------------------|------------------------------------|----------------------------------|
| -55 $^{\circ}C$ to +125 $^{\circ}C$ | 0 $^{\circ}C$ to +70 $^{\circ}C$ | 0 $^{\circ}C$ to +70 $^{\circ}C$ |
| 8-Pin CERDIP Package | 8-Pin Small Outline Package (SOIC) | 8-Pin Plastic Dip Package |
| ALD1702A DA | ALD1702A SA | ALD1702A PA |
| ALD1702B DA | ALD1702B SA | ALD1702B PA |
| ALD1702 DA | ALD1702 SA | ALD1702 PA |
| ALD1703 DA | ALD1703 SA | ALD1703 PA |

* Contact factory for industrial temperature range

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_+ _____ 13.2V
 Differential input voltage range _____ -0.3V to $V_+ + 0.3V$
 Power dissipation _____ 600 mW
 Operating temperature range PA, SA package _____ 0°C to $+70^\circ\text{C}$
 DA package _____ -55°C to $+125^\circ\text{C}$
 Storage temperature range _____ -65°C to $+150^\circ\text{C}$
 Lead temperature, 10 seconds _____ $+260^\circ\text{C}$

OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ $V_S = \pm 2.5V$ unless otherwise specified

| Parameter | Symbol | 1702A | | | 1702B | | | 1702 | | | 1703 | | | Unit | Test Conditions |
|------------------------------|-------------------------------|------------------|----------------|-------------------|------------------|----------------|-------------------|------------------|----------------|-------------------|------------------|----------------|-------------------|------------------------------|--|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Supply Voltage | V_S V_+ | ± 2.0 4.0 | | ± 6.0 12.0 | ± 2.0 4.0 | | ± 6.0 12.0 | ± 2.0 4.0 | | ± 6.0 12.0 | ± 2.0 4.0 | | ± 6.0 12.0 | V | Single Supply |
| Input Offset Voltage | V_{OS} | | | 0.9 1.7 | | | 2.0 2.8 | | | 4.5 5.3 | | | 10.0 11.0 | mV mV | $R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Input Offset Current | I_{OS} | | 1.0 | 25 240 | | 1.0 | 25 240 | | 1.0 | 25 240 | | 1.0 | 30 450 | pA pA | $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Input Bias Current | I_B | | 1.0 | 30 300 | | 1.0 | 30 300 | | 1.0 | 30 300 | | 1.0 | 50 600 | pA pA | $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Input Voltage Range | V_{IR} | -0.3 -2.8 | | 5.3 2.8 | -0.3 -2.8 | | 5.3 2.8 | -0.3 -2.8 | | 5.3 2.8 | 0.15 -2.35 | | 4.85 2.35 | V V | $V_+ = +5V$ $V_S = \pm 2.5V$ |
| Input Resistance | R_{IN} | | 10^{12} | | | 10^{12} | | | 10^{12} | | | 10^{12} | | Ω | |
| Input Offset Voltage Drift | TCV_{OS} | | 7 | | | 7 | | | 7 | | | 10 | | $\mu\text{V}/^\circ\text{C}$ | $R_S \leq 100K\Omega$ |
| Power Supply Rejection Ratio | PSRR | 70 70 | 80 80 | | 65 65 | 80 80 | | 65 65 | 80 80 | | 60 60 | 80 80 | | dB dB | $R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Common Mode Rejection Ratio | CMRR | 70 70 | 83 83 | | 65 65 | 83 83 | | 65 65 | 83 83 | | 60 60 | 83 83 | | dB dB | $R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Large Signal Voltage Gain | A_V | 50 20 | 85 400 | | 50 20 | 85 400 | | 50 20 | 85 400 | | 32 10 | 85 300 | | V/mV V/mV V/mV | $R_L = 10K\Omega$ $R_L \geq 1M\Omega$ $R_L = 10K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Output Voltage Range | $V_{O\ low}$ $V_{O\ high}$ | | 0.002 4.998 | 0.01 | | 0.002 4.998 | 0.01 | | 0.002 4.998 | 0.01 | | 0.002 4.998 | 0.01 | V V | $R_L = 1M\Omega$ $V_+ = 5V$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| | $V_{O\ low}$ $V_{O\ high}$ | | -2.44 2.35 | -2.35 | | -2.44 2.35 | -2.35 | | -2.44 2.35 | -2.35 | | -2.4 2.3 | -2.3 | V | $R_L = 10K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| Output Short Circuit Current | I_{SC} | | 8 | | | 8 | | | 8 | | | 8 | | mA | |
| Supply Current | I_S | | 1.1 | 2.0 | | 1.1 | 2.0 | | 1.1 | 2.0 | | 1.1 | 2.5 | mA | $V_{IN} = 0V$ No Load |
| Power Dissipation | P_D | | 5.5 | 10.0 | | 5.5 | 10.0 | | 5.5 | 10.0 | | 5.5 | 12.5 | mW | $V_S = \pm 2.5V$ |
| Input Capacitance | C_{IN} | | 1 | | | 1 | | | 1 | | | 1 | | pF | |
| Bandwidth | B_W | 1.0 | 1.5 | | 1.0 | 1.5 | | 1.0 | 1.5 | | 0.7 | 1.5 | | MHz | |
| Slew Rate | S_R | 1.4 | 2.1 | | 1.4 | 2.1 | | 1.4 | 2.1 | | 1.1 | 2.1 | | V/ μs | $A_V = +1$ $R_L = 10K\Omega$ |
| Rise time | t_r | | 0.2 | | | 0.2 | | | 0.2 | | | 0.2 | | μs | $R_L = 10K\Omega$ $C_L = 100\text{pF}$ |

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

$T_A = 25^\circ\text{C}$ $V_S = \pm 2.5\text{V}$ unless otherwise specified

| Parameter | Symbol | 1702A | | | 1702B | | | 1702 | | | 1703 | | | Unit | Test Conditions |
|--------------------------|--------|-------|-------------|-----|-------|-------------|-----|------|-------------|-----|------|-------------|-----|--------------------------------|--|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Overshoot Factor | | | 10 | | | 10 | | | 10 | | | 10 | | % | $R_L = 10\text{K}\Omega$ $C_L = 100\text{pF}$ |
| Maximum Load Capacitance | C_L | | 400 4000 | | | 400 4000 | | | 400 4000 | | | 400 4000 | | pF pF | Gain = 1 Gain = 5 |
| Input Noise Voltage | e_n | | 26 | | | 26 | | | 26 | | | 26 | | $\text{nV}/\sqrt{\text{Hz}}$ | $f = 1\text{KHz}$ |
| Input Current Noise | i_n | | 0.6 | | | 0.6 | | | 0.6 | | | 0.6 | | $\text{fA}/\sqrt{\text{Hz}}$ | $f = 10\text{Hz}$ |
| Settling Time | t_s | | 8.0 3.0 | | | 8.0 3.0 | | | 8.0 3.0 | | | 8.0 3.0 | | μs μs | 0.01% 0.1% $A_V = -1$ $R_L = 5\text{K}\Omega$ $C_L = 50\text{pF}$ |

$T_A = 25^\circ\text{C}$ $V_S = \pm 5.0\text{V}$ unless otherwise specified

| Parameter | Symbol | 1702A | | | 1702B | | | 1702 | | | 1703 | | | Unit | Test Conditions |
|------------------------------|-------------------------|-------|--------------|------|-------|--------------|------|------|--------------|------|------|--------------|------|------------------|-----------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Power Supply Rejection Ratio | PSRR | | 83 | | | 83 | | | 83 | | | 83 | | dB | $R_S \leq 100\text{K}\Omega$ |
| Common Mode Rejection Ratio | CMRR | | 83 | | | 83 | | | 83 | | | 83 | | dB | $R_S \leq 100\text{K}\Omega$ |
| Large Signal Voltage Gain | A_V | | 250 | | | 250 | | | 250 | | | 250 | | V/mV | $R_L = 10\text{K}\Omega$ |
| Output Voltage Range | V_O low V_O high | 4.8 | -4.9 4.93 | -4.8 | 4.8 | -4.9 4.93 | -4.8 | 4.8 | -4.9 4.93 | -4.8 | 4.8 | -4.9 4.93 | -4.8 | V | $R_L = 10\text{K}\Omega$ |
| Bandwidth | BW | | 1.7 | | | 1.7 | | | 1.7 | | | 1.7 | | MHz | |
| Slew Rate | S_R | | 2.8 | | | 2.8 | | | 2.8 | | | 2.8 | | V/ μs | $A_V = +1$ $C_L = 50\text{pF}$ |

$V_S = \pm 2.5\text{V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise specified

| Parameter | Symbol | 1702A DA | | | 1702B DA | | | 1702 DA | | | Unit | Test Conditions |
|------------------------------|-------------------------|----------|------------|------|----------|------------|------|---------|------------|------|------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Input Offset Voltage | V_{OS} | | | 3.0 | | | 4.0 | | | 6.5 | mV | $R_S \leq 100\text{K}\Omega$ |
| Input Offset Current | I_{OS} | | | 8.0 | | | 8.0 | | | 8.0 | nA | |
| Input Bias Current | I_B | | | 10.0 | | | 10.0 | | | 10.0 | nA | |
| Power Supply Rejection Ratio | PSRR | 60 | 75 | | 60 | 75 | | 60 | 75 | | dB | $R_S \leq 100\text{K}\Omega$ |
| Common Mode Rejection Ratio | CMRR | 60 | 83 | | 60 | 83 | | 60 | 83 | | dB | $R_S \leq 100\text{K}\Omega$ |
| Large Signal Voltage Gain | A_V | 10 | 25 | | 10 | 25 | | 7 | 25 | | V/mV | $R_L = 10\text{K}\Omega$ |
| Output Voltage Range | V_O low V_O high | 4.8 | 0.1 4.9 | 0.2 | 4.8 | 0.1 4.9 | 0.2 | 4.8 | 0.1 4.9 | 0.2 | V | $R_L = 10\text{K}\Omega$ |

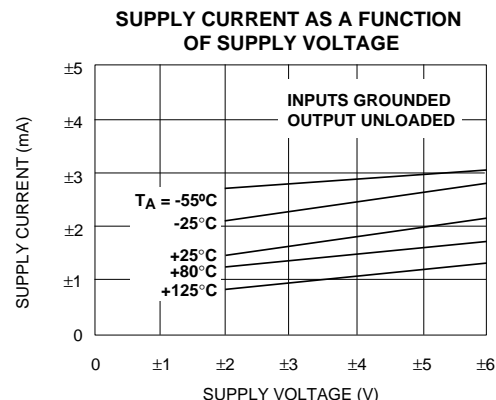
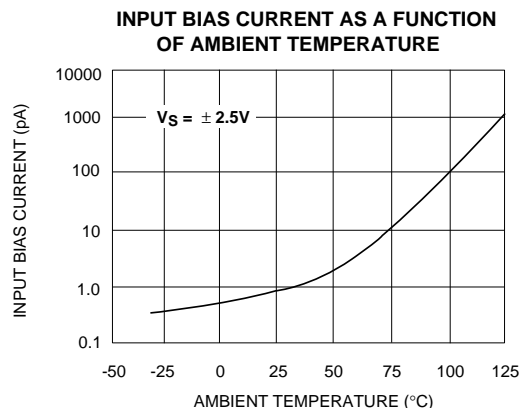
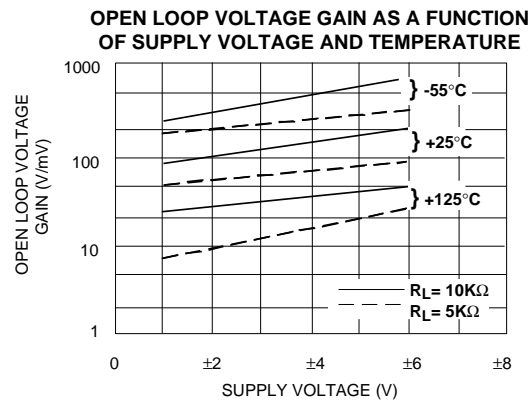
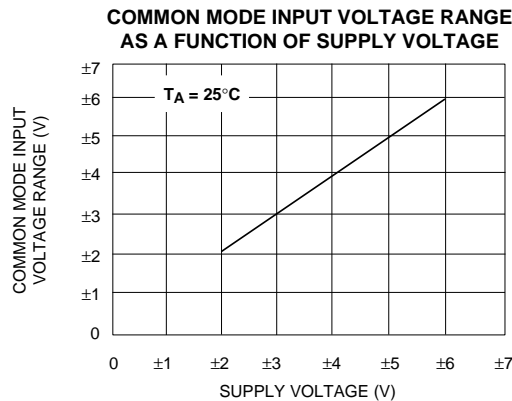
Design & Operating Notes:

1. The ALD1702/ALD1703 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1702 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD1702 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD1702 has shown itself to be more resistant to parasitic oscillations.
2. The ALD1702/ALD1703 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. Since offset voltage trimming on the ALD1702/ALD1703 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point. The user should however, be

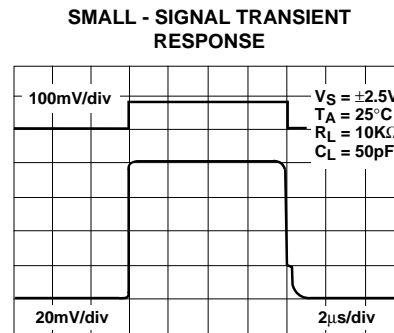
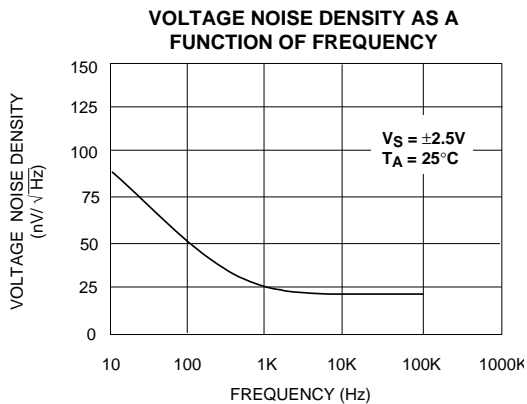
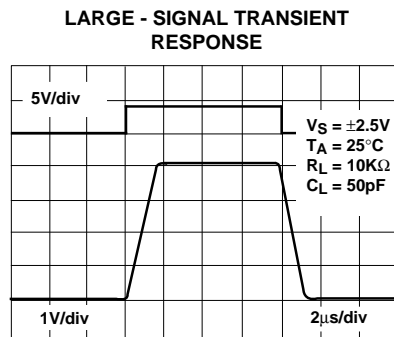
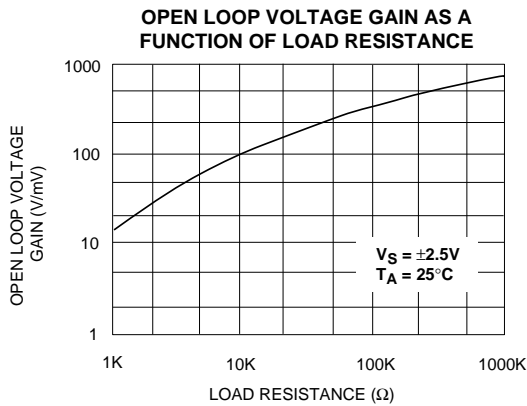
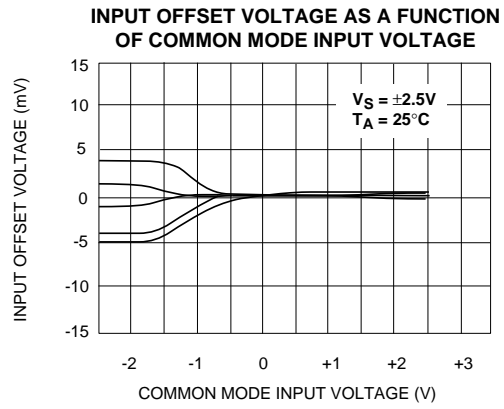
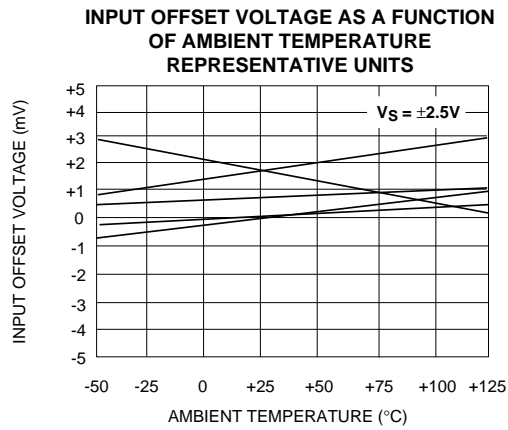
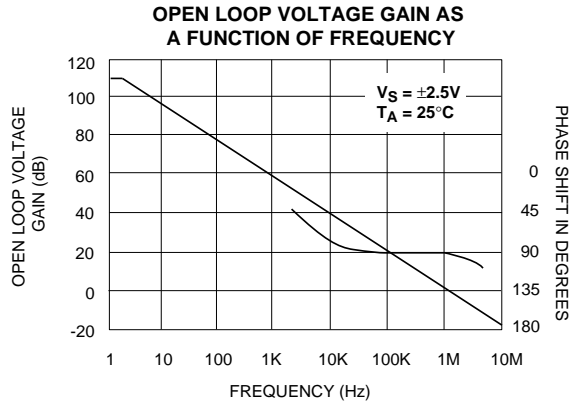
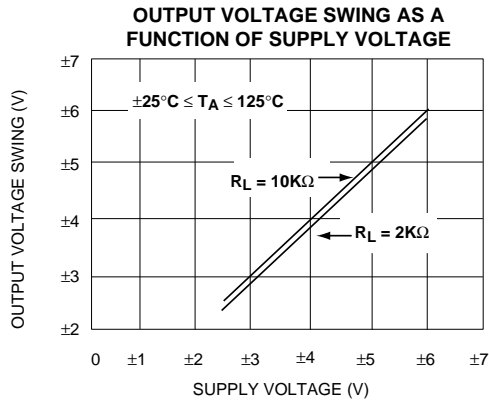
aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.

3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{12}\Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. The ALD1702/ALD1703 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

TYPICAL PERFORMANCE CHARACTERISTICS

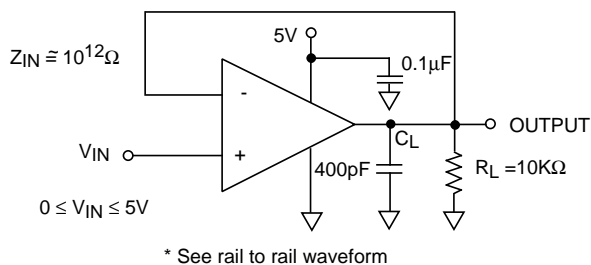


TYPICAL PERFORMANCE CHARACTERISTICS

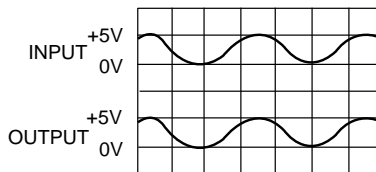


TYPICAL APPLICATIONS

RAIL TO RAIL VOLTAGE FOLLOWER/BUFFER



RAIL-TO-RAIL WAVEFORM



Performance waveforms.
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-rail voltage follower.

LOW OFFSET SUMMING AMPLIFIER

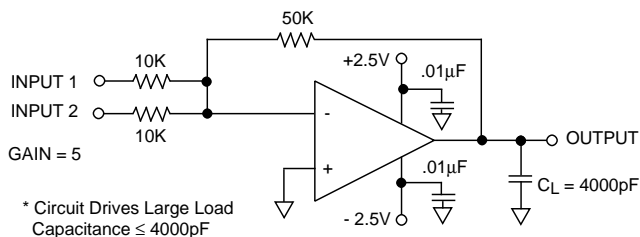
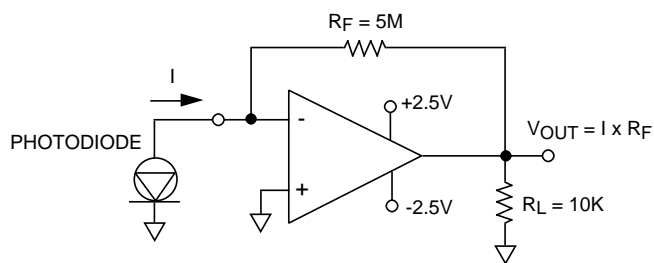
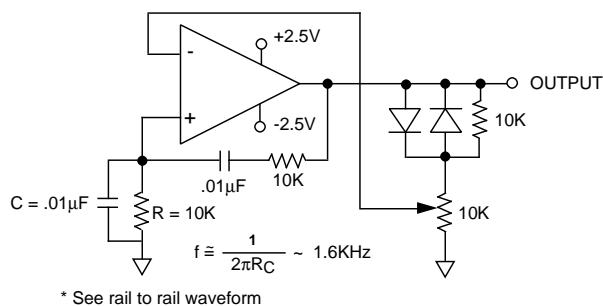


PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR



RAIL-TO-RAIL VOLTAGE COMPARATOR

