

#### **RAIL-TO-RAIL PRECISION OPERATIONAL AMPLIFIER**

#### **GENERAL DESCRIPTION**

The ALD1712 is a monolithic precision operational amplifier intended primarily for a wide range of analog applications in +5V single power supply and ±5V dual power supply systems as well as +6V to 12V battery operated systems. All device characteristics are specified for +5V single supply or ±2.5V dual supply systems. It is manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process and is available as a standard cell in ALD's ASIC "Function-Specific" library.

The device has an input stage that operates to +300mV above and -300mV below the supply voltages with no adverse effects and/or phase reversals.

The ALD1712 has been developed specifically with the 5V single supply or  $\pm 2.5 V$  dual supply user in mind. Several important characteristics of the device make many applications easy to implement for these supply voltages. First, the operational amplifier can operate with rail-to-rail input and output voltages. This feature allows numerous analog serial stages to be implemented without losing operating voltage margin. Secondly, the device was designed to accommodate mixed applications where digital and analog circuits may work off the same 5V power supply. Thirdly, the output stage can drive up to 400pF capacitive, and 1K $\Omega$  resistive loads in non-inverting unity gain connection, and up to 4000pF at a gain of 5. These features, coupled with extremely low input currents, high voltage gain, useful bandwidth of 1.5MHz, slew rate of 2.1V/ $\mu$ s, low power dissipation, low offset voltage and temperature drift, make the ALD1712 a truly versatile, user friendly, operational amplifier.

On-chip offset voltage trimming allows the device to be used without nulling in most applications. The device offers typical offset drift of less than  $5\mu\text{V/}$  °C which eliminates many trim or temperature compensation circuits. For precision applications, the 1712 is designed to settle to 0.01% in 8 $\mu\text{s}$ . The unique characteristics at input and output are modeled in an available macromodel.

#### ORDERING INFORMATION

Оре	Operating Temperature Range											
-55°C to +125°C												
8-Pin CERDIP Package	8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package										
ALD 1712A DA ALD 1712B DA ALD 1712 DA	ALD 1712 ASA ALD 1712 BSA ALD 1712 SA	ALD 1712A PA ALD 1712B PA ALD 1712 PA										

<sup>\*</sup> Contact factory for industrial temperature range

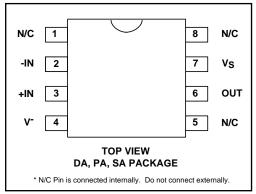
#### **FEATURES**

- Linear mode operation with input voltages 300mV beyond supply rails
- Symmetrical complementary output drive
- Output voltages to within 2mV of power supply rails
- High load capacitance capability --4000pF typical
- No frequency compensation required -unity gain stable
- Extremely low input bias currents --0.01pA typical
- Dual power supply ±2.5V to ±6.0V
- Single power supply +5V to +12V
- High voltage gain typically 85V/mV
   ±2.5V and 250V/mV @ ±5.0V
- Drive as low as 1KΩ load with 5mA drive current
- Output short circuit protected
- Unity gain bandwidth of 1.5MHz
- Slew rate of 2.1V/μs

#### **APPLICATIONS**

- Voltage amplifier
- · Voltage follower/buffer
- Charge integrator
- · Photodiode amplifier
- · Data acquisition systems
- · High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- · Current to voltage converter
- Coaxial cable driver

#### PIN CONFIGURATION



#### **ABSOLUTE MAXIMUM RATINGS**

Supply voltage, V+	13.2V
Differential input voltage range	-0.3V to V++0.3V
Power dissipation	600 mW
Operating temperature range PA,SA package	0°C to +70°C
DA package	55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature 10 seconds	+260°C

# OPERATING ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$ $V_S = \pm 2.5V$ unless otherwise specified

		1712A				1712B			1712			
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
Supply Voltage	V <sub>S</sub> V+	±2.0 4.0		±6.0 12.0	±2.0 4.0		±6.0 12.0	±2.0 4.0		±6.0 12.0	٧	Single Supply
Input Offset Voltage	Vos		0.05	0.15 0.35		0.1	0.25 0.55		0.25	0.5 1.0	mV mV	$R_S \le 100K\Omega$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Input Offset Current	los		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	$T_A = 25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Input Bias Current	IB		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	$T_A = 25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Input Voltage Range	V <sub>IR</sub>	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	$V^{+}$ = +5; notes 2,5 $V_{S}$ = ±2.5V
Input Resistance	R <sub>IN</sub>		10 <sup>13</sup>			10 <sup>13</sup>			10 <sup>13</sup>		Ω	
Input Offset Voltage Drift	TCVos		5			5			5		μV/°C	R <sub>S</sub> ≤ 100KΩ
Power Supply Rejection Ratio	PSRR	65 65	85 85		65 65	85 85		63 63	85 85		dB dB	$R_S \le 100 K\Omega$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Common Mode Rejection Ratio	CMRR	65 65	83 83		65 65	83 83		63 63	83 83		dB dB	$R_S \le 100 K\Omega$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Large Signal Voltage Gain	Av	50 20	85 400		50 20	85 400		50 20	85 400		V/mV V/mV V/mV	$R_L = 10K\Omega$ $R_L \ge 1M\Omega$ $R_L = 10K\Omega$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Output Voltage	V <sub>O</sub> low V <sub>O</sub> high	4.99	0.002 4.998	0.01	4.99	0.002 4.998	0.01	4.99	0.002 4.998	0.01	V V	$R_L = 1M\Omega V^+ = +5V$ $0^{\circ}C \le T_A \le +70^{\circ}C$
Range	V <sub>O</sub> low V <sub>O</sub> high	2.35	-2.44 2.44	-2.35	2.35	-2.44 2.44	-2.35	2.35	-2.44 2.44	-2.35	V V	$R_{L} = 10K\Omega$ $0^{\circ}C \le T_{A} \le +70^{\circ}C$
Output Short Circuit Current	Isc		8			8			8		mA	
Supply Current	IS		0.8	1.5		0.8	1.5		0.8	1.5	mA	V <sub>IN</sub> = 0V No Load
Power Dissipation	PD		4.0	7.5		4.0	7.5		4.0	7.5	mW	V <sub>S</sub> = ±2.5V
Input Capacitance	CIN		1			1			1		pF	
Bandwidth	B <sub>W</sub>	1.0	1.5		1.0	1.5		1.0	1.5		MHz	
Slew Rate	S <sub>R</sub>	1.4	2.1		1.4	2.1		1.4	2.1		V/μs	$A_V = +1$ $R_L = 10K\Omega$
Rise time	t <sub>r</sub>		0.2			0.2			0.2		μs	R <sub>L</sub> = 10KΩ
Overshoot Factor			10			10			10		%	$R_L = 10K\Omega$ $C_L = 100pF$

# OPERATING ELECTRICAL CHARACTERISTICS (cont'd) $T_A=25^{\circ}C~V_S=\pm2.5V~$ unless otherwise specified

			1712A			1712B		1712				
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
Maximum Load Capacitance	CL		400 4000			400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Input Noise Voltage	e <sub>n</sub>		26			26			26		nV/√ <del>H</del> z	f =1KHz
Input Current Noise	i <sub>n</sub>		0.6			0.6			0.6		fA/√ <del>Hz</del>	f =10Hz
Settling Time	t <sub>s</sub>		8.0 3.0			8.0 3.0			8.0 3.0		ns hs	0.01% 0.1% Av = -1 R <sub>L</sub> = 5KΩ C <sub>L</sub> = 50pF

### $T_A = 25^{\circ}C$ $V_S = \pm 5.0V$ unless otherwise specified

			1712A			1712B		1712				
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
Power Supply Rejection Ratio	PSRR		83			83			83		dB	$R_S \le 100 K\Omega$
Common Mode Rejection Ratio	CMRR		83			83			83		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	A <sub>V</sub>		250			250			250		V/mV	R <sub>L</sub> = 10KΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	4.80	-4.90 4.93	-4.80	4.80	-4.90 4.93	-4.80	4.80	-4.90 4.93	-4.80	>	R <sub>L</sub> = 10KΩ
Bandwidth	B <sub>W</sub>		1.7			1.7			1.7		MHz	
Slew Rate	S <sub>R</sub>		2.8			2.8			2.8		V/µs	A <sub>V</sub> =+1 C <sub>L</sub> =50pF

#### $V_S = \pm 2.5V - 55^{\circ}C \le T_A \le +125^{\circ}C$ unless otherwise specified

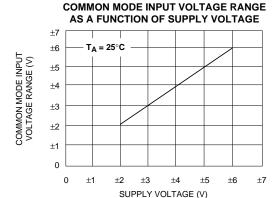
			1712A I	DA		1712B	DA		1712 DA			
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
Input Offset Voltage	Vos		0.5	1.0		0.8	1.5		1.2	2.5	mV	R <sub>S</sub> ≤ 100KΩ
Input Offset Current	Ios			4.0			4.0			4.0	nA	
Input Bias Current	I <sub>B</sub>			4.0			4.0			4.0	nA	
Power Supply Rejection Ratio	PSRR	60	83		60	83		60	83		dB	$R_S \le 100 K\Omega$
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	AV	10	25		10	25		10	25		V/mV	R <sub>L</sub> = 10KΩ
Output Voltage Range	VO low VO high	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	V	$\begin{aligned} R_L &\leq 10 K \Omega \\ R_L &\leq 10 K \Omega \end{aligned}$

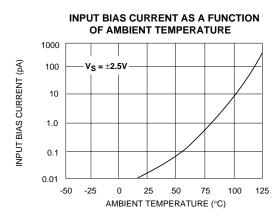
#### **Design & Operating Notes:**

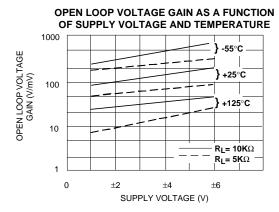
- 1. The ALD1712 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1712 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD1712 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD1712 has shown itself to be more resistant to parasitic oscilla-
- 2. The ALD1712 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. Since offset voltage trimming on the 1712 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point. The user should however, be aware that this

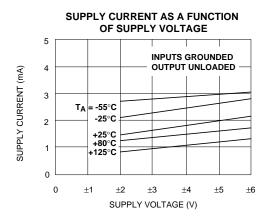
- switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.
- 3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than 10<sup>12</sup>Ω would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.
- 4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
- 5. The ALD1712 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

#### TYPICAL PERFORMANCE CHARACTERISTICS

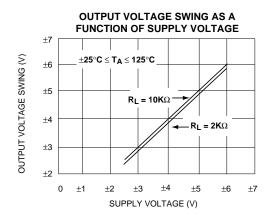


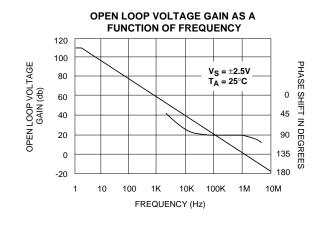




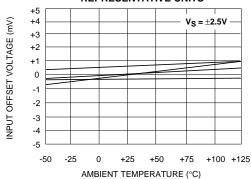


#### TYPICAL PERFORMANCE CHARACTERISTICS

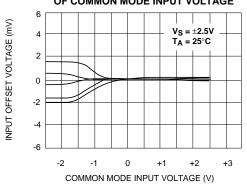




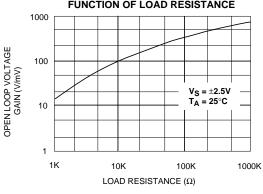




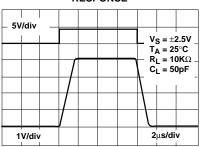




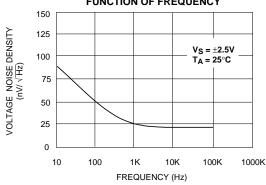
# OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



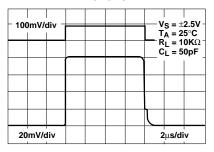
LARGE - SIGNAL TRANSIENT RESPONSE



## VOLTAGE NOISE DENSITY AS A FUNCTION OF FREQUENCY



SMALL - SIGNAL TRANSIENT RESPONSE



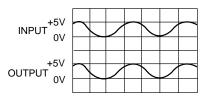
#### TYPICAL APPLICATIONS

#### **RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER**

#### \_\_0.1μFι <del>\</del> 5V 9 $Z_{\text{IN}} \approx 10^{12} \Omega$ OUTPUT VIN o $R_L = 10 K\Omega$ 400pF $0 \le V_{IN} \le 5V$

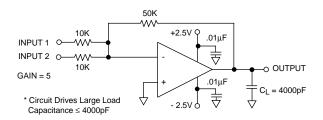
\* See rail to rail waveform

#### **RAIL-TO-RAIL WAVEFORM**

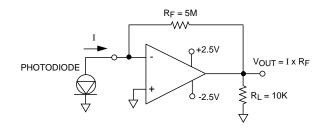


Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Railto-Rail voltage follower.

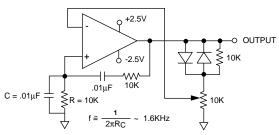
#### **LOW OFFSET SUMMING AMPLIFIER**



#### PHOTO DETECTOR CURRENT TO **VOLTAGE CONVERTER**

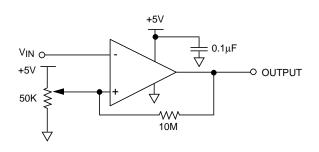


#### WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE **WAVE GENERATOR**

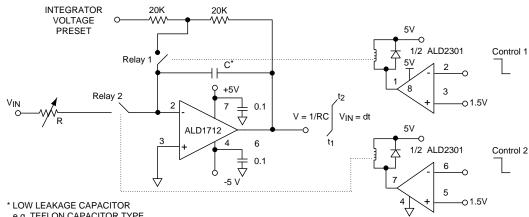


\* See rail to rail waveform

#### **RAIL-TO-RAIL VOLTAGE COMPARATOR**



#### **ULTRA LONG TIME CONSTANT INTEGRATOR**



- e.g. TEFLON CAPACITOR TYPE
- K11B104KSW Component
- Research Inc.
- All capacitance values are in μF unless otherwise specified.
- RELAYS 1 & 2 are of type 4705, Gordos Corporation.