



PRODUCT SPECIFICATION

Product Description

The aMC8500 is a full featured monolithic brushless DC motor controller containing all the required functions to implement fan speed control. This device features a selectable slope pulse width modulator (PWM) for efficient speed control with analog and digital control signal compatibility, programmable minimum speed setting, Hall amplifier with propriety noise immunity circuitry for proper drive sequencing, fixed non-overlapping commutation delay for reduced supply current spiking, dual on-chip 0.5 Ω power MOSFETs with thermal protection for direct motor drive, programmable cycle-by-cycle current limiting, internal fault timer with auto start retry, motor kick start timer to insure start up, combined frequency generator / rotor lock output, uncommitted op amp with reference for thermal sensor voltage scaling, and a selectable automatic low current power down mode for power sensitive applications.

Features

- Analog and digital speed control signal compatibility
- Programmable minimum speed setting
- Selectable PWM speed control slope
- Latching PWM for enhanced noise immunity
- Integrated fault timer with auto start retry
- Motor kick start timer
- Combined frequency generator / rotor lock output
- Differential unbuffered and digital Hall compatibility
- Hall amplifier with propriety noise immunity circuitry
- Pinned out reference
- Uncommitted op amp for thermal sensor voltage scaling
- Fixed non-overlapping commutation delay
- Dual on-chip 0.5 Ω MOSFET motor drives
- Programmable cycle-by-cycle current limit protection
- Thermal shutdown protection
- Under voltage lockout protection
- Selectable automatic low current power down mode

Applications

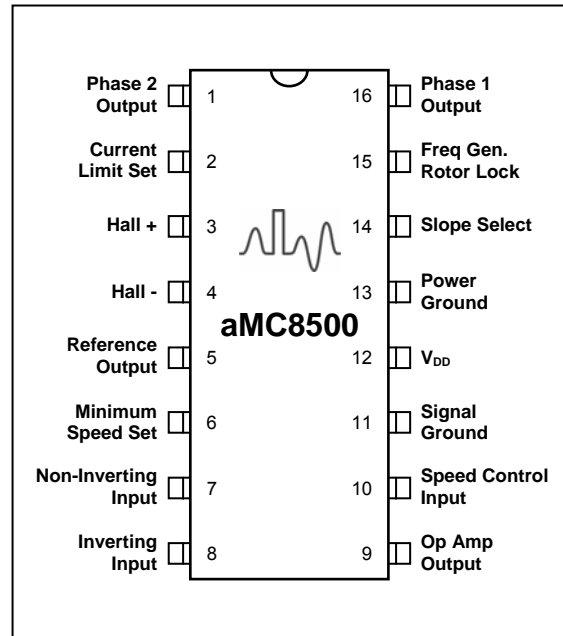
- Personal computer fans
- Workstation and mainframe fans
- LAN server blowers
- Industrial control system fans
- Telcom system fans
- Instrumentation test and measurement fans
- Card rack fans

Ordering Information

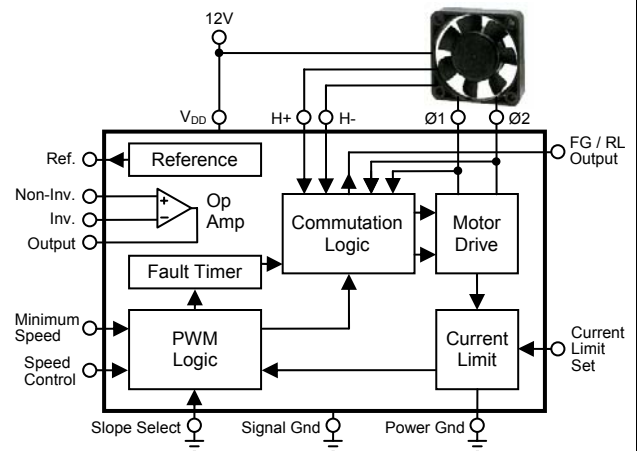
Part Number	Package	Operating Junction Temperature Range	Marking
aMC8500DE16	SOIC 16 Lead Exposed Pad	-40°C to 125°C	aMC8500 Ayww
aMC8500QS16	QSOP 16 Lead		

Ayww – Assembly site year workweek

Pin Configuration



Application Diagram



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**Absolute Maximum Ratings** (Note 1)

Parameter	Symbol	Rating	Unit
Power Supply Voltage (Pin 12)	$V_{DD}$	-0.3 to 18	V
Hall Input Voltage Range (Pin 3, 4)	$V_{IR(Hall)}$	-0.3 to $V_{DD}$	V
Speed Control Input Voltage Range (Pin 10)	$V_{IR(S)}$	-0.3 to $V_{DD}$	V
Minimum Speed Set Input Voltage Range (Pin 6)	$V_{IR(MSS)}$	-0.3 to $V_{DD}$	V
Reference Output Load Current (Pin 5)	$I_{O(Ref)}$	Internally Limited	mA
Op Amp Input Voltage Range (Pin 7, 8)	$V_{IR(OA)}$	-0.3 to $V_{DD}$	V
Op Amp Output (Pin 9, Note 4)			
Voltage Range	$V_{OR(OA)}$	-0.3 to $V_{DD}$	V
Source or Sink Current	$I_{O(OA)}$	30	mA
Slope Select Input Voltage Range (Pin 14)	$V_{IR(LS)}$	-0.3 to $V_{REF}$	V
Current Limit Set Input Voltage Range (Pin 2)	$V_{IR(ILim)}$	-0.3 to $V_{REF}$	V
Frequency Generator / Rotor Lock Output (Pin 15)			
Voltage Range	$V_{OR(FG/RL)}$	-0.3 to 18	V
Sink Current	$I_{Sink(FG/RL)}$	20	mA
Drive Outputs (Pin 1, 16, Note 4)			
Voltage Range	$V_{D(\emptyset1/\emptyset2)}$	-0.3V to 36	V
Sink Current	$I_{Sink(\emptyset1/\emptyset2)}$	1.5	A
Source Current	$I_{Source(\emptyset1/\emptyset2)}$	-1.5	A
Thermal Characteristics			$^{\circ}C/W$
SOP-16 Exposed Pad Package			
Thermal Resistance, Junction to Air	$R_{\emptyset JA}$	92	
Thermal Resistance, Junction to Pad	$R_{\emptyset JC}$	15	
QSOP-16 Package			
Thermal Resistance, Junction to Air	$R_{\emptyset JA}$	136	
Operating Junction Temperature Range	$T_{J(max)}$	-40 $^{\circ}C$ to 125	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	-60 $^{\circ}C$ to 150	$^{\circ}C$
IR Reflow Peak Temperature	$T_{reflow}$	260	$^{\circ}C$
Lead Soldering Temperature (10 sec)	$T_{lead}$	300	$^{\circ}C$
Electrostatic Discharge (Note 2)	ESD		V
Human Body Model		2000	
Machine Model		250	

**Notes:**

- Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only. Functional operation at or above these limits is not implied.
- Human Body Model: 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor into each pin.  
Machine Model: 200 pF capacitor discharged directly into each pin.
- These specifications are guaranteed only for the test conditions listed.
- Maximum package power dissipation limits must be observed.

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**Electrical Characteristics**

( $V_{DD} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted. Specifications subject to change without notice [Note 3].)

Parameter	Symbol	Min	Typ	Max	Units
<b>SPEED CONTROL (Pin 10) and MINIMUM SPEED SET (Pin 6)</b>					
Input Threshold Voltage Pin 14 = Gnd 0% Drive Conduction 100% Drive Conduction Pin 14 = Open 0% Drive Conduction 100% Drive Conduction	$V_{th(0\%)}$ $V_{th(100\%)}$ $V_{th(0\%)}$ $V_{th(100\%)}$	0.95 2.85 2.85 0.95	1.0 3.0 3.0 1.0	1.05 3.15 3.15 1.05	V
Speed Control Input Threshold Voltage for Power Down ( $I_{O(ref)} \leq 1.0\text{ mA}$ ) Input Voltage Below 0% Drive Conduction, $V_{th(0\%)}$ , Pin 14 = Gnd Input Voltage Above 0% Drive Conduction, $V_{th(0\%)}$ , Pin 14 = Open	$V_{th(PD)}$	- -	20 20	- -	mV
Speed Control Input PWM Signal Transition Time Maximum allowable rise or fall time for digital control	$t_r/t_f$	-	-	50	$\mu\text{s}$
Input Bias Current, ( $V_{in} = 3.5\text{ V}$ )	$I_{IB}$	-	1.0	-	$\mu\text{A}$
Modulation Frequency	$f_{PWM}$	-	30	-	kHz
<b>SLOPE SELECT (Pin 14)</b>					
Input Threshold Voltage Low State Increasing voltage at Pin 6, 10 causes increase in drive conduction High State Increasing voltage at Pin 6, 10 causes decrease in drive conduction	$V_{IL(S)}$ $V_{IH(S)}$	- 2.8	- -	1.0 -	V
Low State Input Pull-Up Current ( $V_{IL(S)} = 0\text{ V}$ )	$I_{I(S)}$	-	10	-	$\mu\text{A}$
<b>HALL AMPLIFIER (Pin 3, 4)</b>					
Input Differential Voltage Sensitivity Required signal level to enable drive commutation	$V_{ID(Hall)}$	-	20	40	mVpp
Input Hysteresis Voltage ( $V_{in} = 3.5\text{ V}$ )	$V_{IH(Hall)}$	-	10	-	mV
Input Resistance	$R_{IN(Hall)}$	-	3.0	-	M $\Omega$
Input Common Mode Voltage Range	$V_{ICM(Hall)}$	0 to $V_{DD}$	-0.3 to $V_{DD}$ +0.3	-	V
<b>OP AMP (Pin 7, 8, 9)</b>					
Input Offset Voltage ( $V_{in} = 3.5\text{ V}$ )	$V_{IO}$	-	2.0	-	mV
Input Bias Current ( $V_{in} = \text{Gnd}$ )	$I_{IB}$	-	50	-	nA
Input Common Mode Voltage Range	$V_{ICM(OA)}$	-	0 to 4.2	-	V
Open Loop Voltage Gain	$A_{VOL}$	80	100	-	dB
Gain Bandwidth Product ( $f = 10\text{ kHz}$ )	GBW	-	70	-	kHz
Output Voltage Swing High State ( $I_{source} = 5.0\text{ mA to Gnd}$ ) Low State ( $I_{sink} = 5.0\text{ mA to }V_{DD}$ )	$V_{OH(OA)}$ $V_{OL(OA)}$	- -	-1.5 0.5	- -	V

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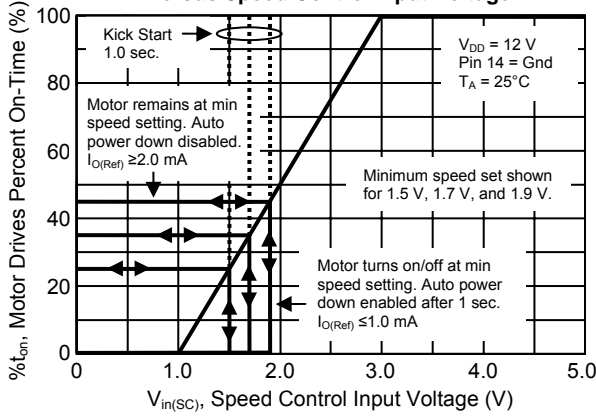


<b>REFERENCE (Pin 5)</b>					
Output Voltage ( $I_o = 5.0 \text{ mA}$ )	$V_{ref}$	3.325	3.5	3.675	V
Line Regulation ( $V_{DD} = 6.0 \text{ V to } 15 \text{ V}$ , $I_o = 5.0 \text{ mA}$ )	$Ref_{line}$	-	2.0	30	mV
Load Regulation ( $V_{DD} = 6.0 \text{ V}$ , $I_o = 1.0 \text{ mA to } 10 \text{ mA}$ )	$Ref_{load}$	-	11	30	mV
Short Circuit Current (Note 4)	$I_{SC}$	-	50	-	mA
Reference Output Load Current For Automatic Power Down Feature (Pin 10 = 500 mV, Pin 14 = Gnd, $t > 2.0\text{s}$ ) (Pin 10 = 3.5 V, Pin 14 = Open, $t > 2.0\text{s}$ )	$I_{O(PD)}$				mA
Enabled		-	1.4	1.0	
Disabled		2.0	1.6	-	
<b>FAULT TIMER</b>					
Drive Enabled Time During A Fault Condition	$t_{on(Fit)}$	-	0.25	-	s
Drive Disabled Time Before Restart	$t_{off(Fit)}$	-	2.0	-	s
<b>KICK START TIMER</b>					
Motor Kick Start Time (100% duty cycle applied)	$t_{on(KS)}$	-	1.0	-	s
<b>FREQUENCY GENERATOR / ROTOR LOCK (Pin 15)</b>					
Low State Output Sink Voltage ( $I_{sink} = 1.0 \text{ mA}$ )	$V_{OL(FG/RL)}$	-	0.13	0.25	V
Off-State Leakage Current ( $V_{off} = 12 \text{ V}$ )	$I_{off(Tach)}$	-	0.1	1.0	$\mu\text{A}$
Minimum Hall Frequency For Rotor Lock Output High State	$f_{RL(min)}$	-	4.0	-	Hz
<b>MOTOR DRIVES (Pin 1, 16)</b>					
Low State Output Voltage ( $I_{sink} = 500 \text{ mA}$ )	$V_{OL(Drv)}$	-	250	300	mV
Off-State Leakage Current ( $V_{off} = 30 \text{ V}$ )	$I_{off(Drv)}$	-	-	5.0	$\mu\text{A}$
Current Limit Threshold (Pin 2 open, Note 4)	$I_{Lim}$	900	1100	1300	mA
Non-Overlapping Commutation Delay	$t_{dly(Com)}$	-	40	-	$\mu\text{s}$
<b>TOTAL DEVICE (Pin 12)</b>					
Power Supply Threshold Voltage					
Start-Up ( $V_{DD}$ increasing)	$V_{th(on)}$	-	4.7	-	V
Hysteresis ( $V_{DD}$ decreasing after turn-on)	$V_H$	-	500	-	mV
Power Supply Current					
Operating	$I_S$	-	1.6	2.0	mA
Power Down (Pin 10 = 0.5 V, $I_{O(ref)} \leq 1.0 \text{ mA}$ , $t > 2.0\text{s}$ , Pin 14 = Gnd)	$I_{S(PwrDn)}$	-	130	200	$\mu\text{A}$

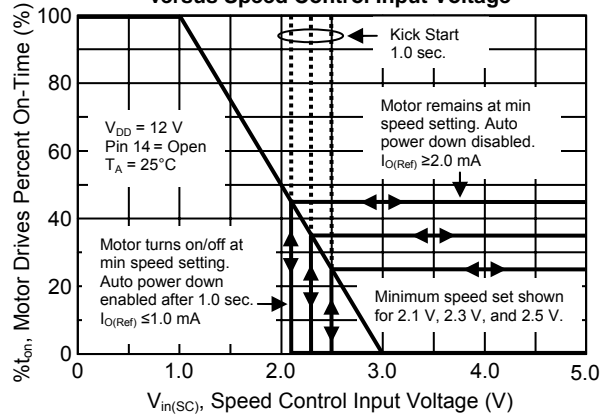
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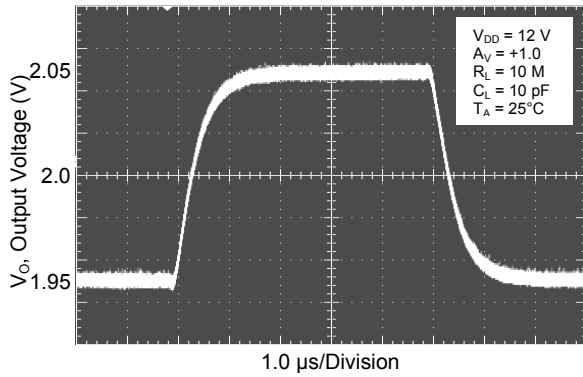
**Figure 1- Motor Drives Percent On-Time versus Speed Control Input Voltage**



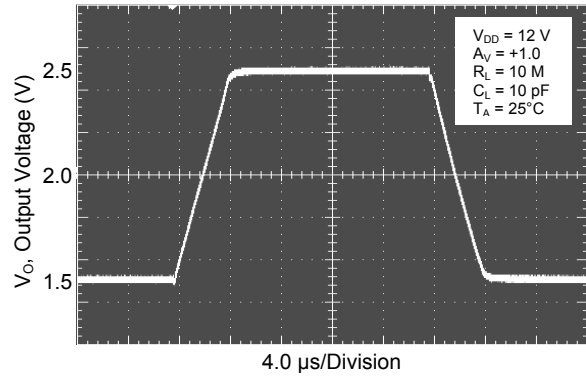
**Figure 2- Motor Drives Percent On-Time versus Speed Control Input Voltage**



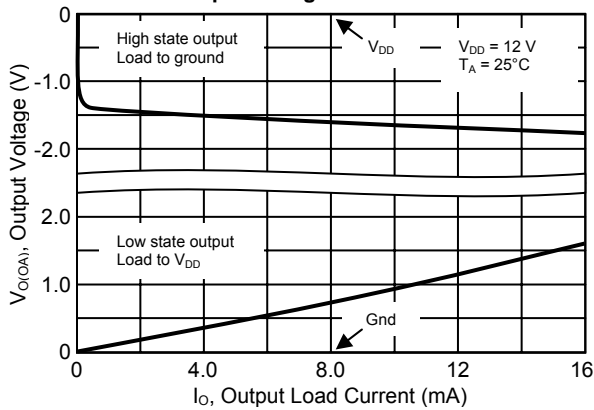
**Figure 3- Op Amp Small Signal Transient Response**



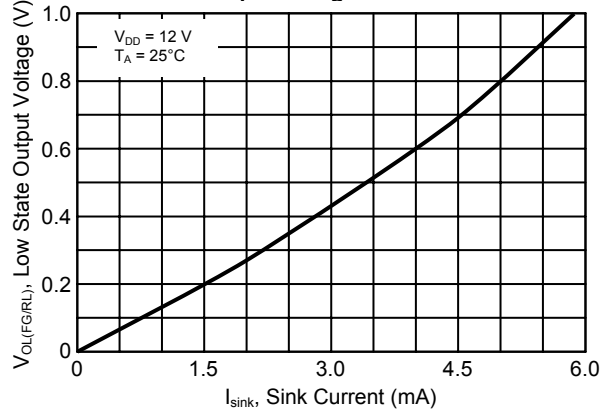
**Figure 4- Op Amp Large Signal Transient Response**



**Figure 5- Op Amp Source and Sink Output Voltage versus Current**



**Figure 6- Frequency Generator / Rotor Lock Low State Output Voltage versus Sink Current**



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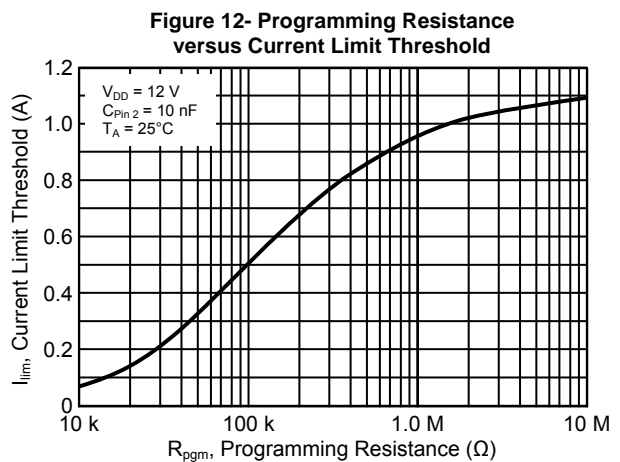
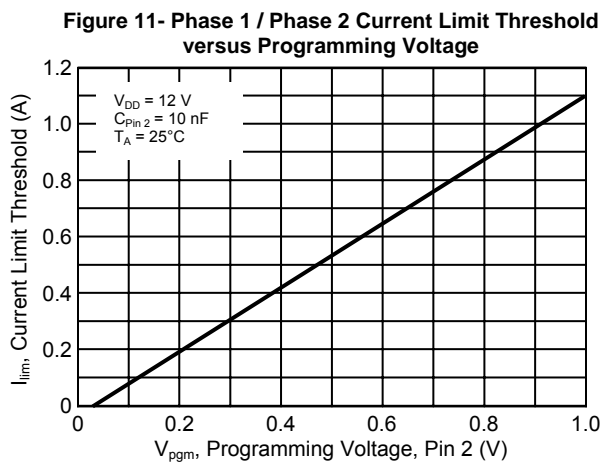
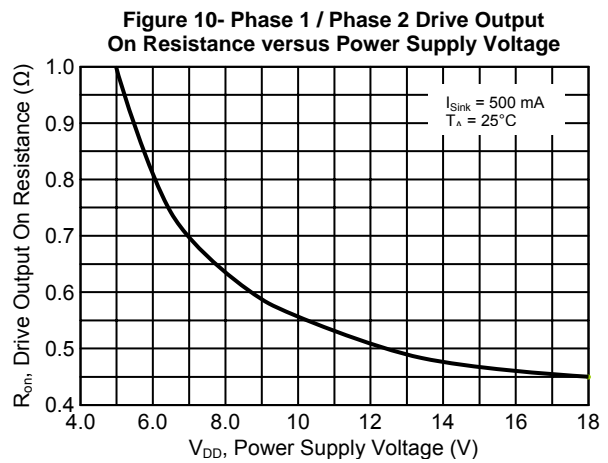
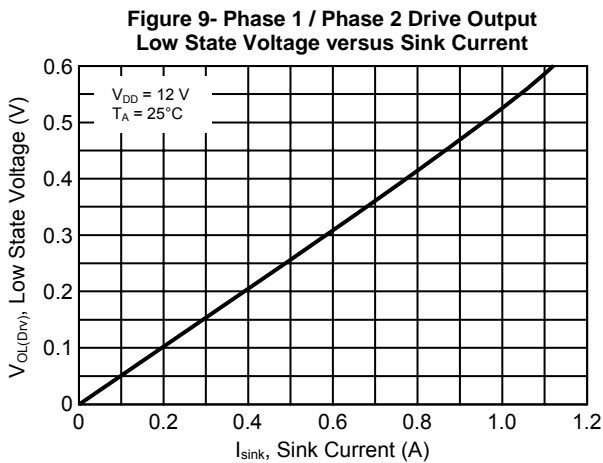
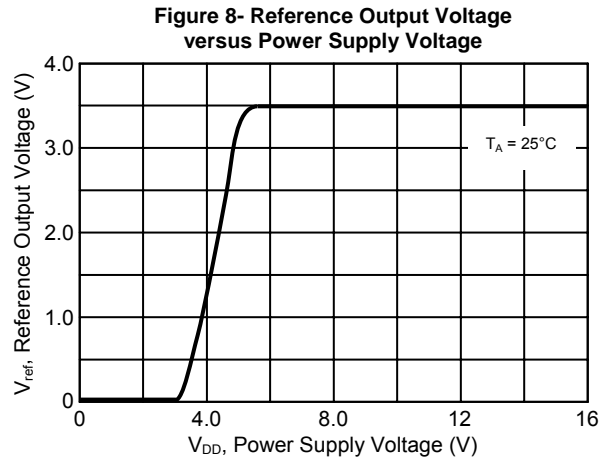
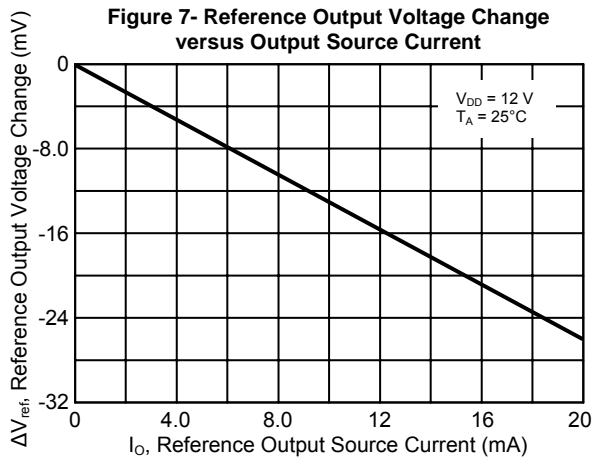
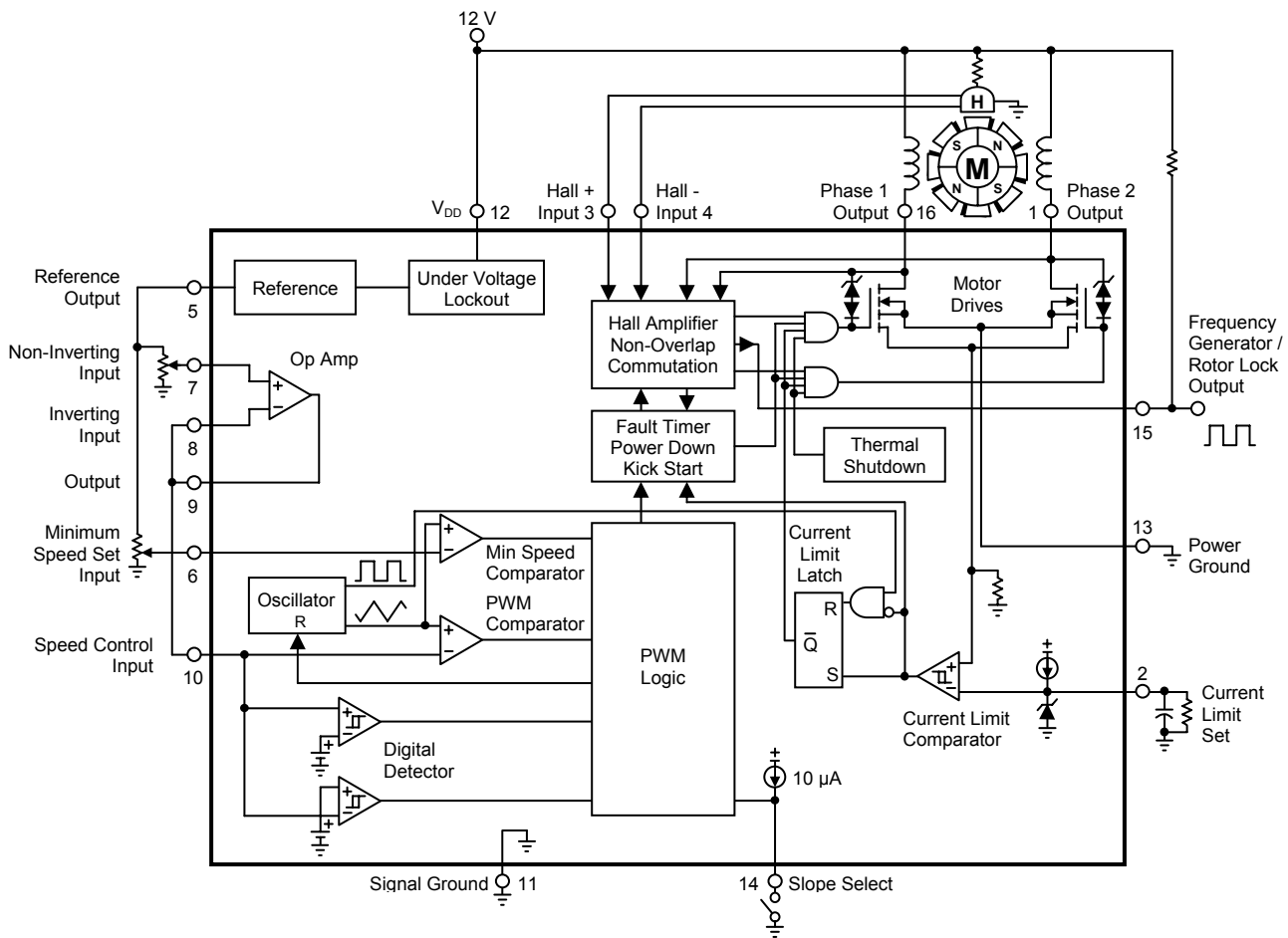


Figure 13- Representative Block Diagram



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## INTRODUCTION

The aMC8500 is a full featured two phase half wave variable speed brushless motor controller containing all the required functions for implementing a fan control system. Motor control features consists of a selectable slope pulse width modulator (PWM) with double pulse suppression for efficient speed control that is compatible with an analog voltage or a varying duty cycle digital pulse train, a programmable minimum speed set input, and an uncommitted op amp with a pinned out reference for speed control signal scaling, Hall sensor amplifier with propriety noise immunity circuitry for proper drive sequencing, non-overlapping commutation drive for reduced supply current spiking, on-chip 0.5  $\Omega$  power MOSFETs for direct coil drive. Protective and diagnostic features include an internal fault timer with auto start retry, motor kick start timer to insure proper start up, programmable cycle-by-cycle current limiting, power supply under voltage lockout, and over temperature thermal shutdown, and a combined frequency generator / rotor lock output for status reporting. Also included is a selectable automatic low current power down mode aimed at power sensitive applications.

The aMC8500 is designed for use in thermal open or closed loop systems. It can be controlled by simple NTC or PTC thermistors, Simistor™ silicon temperature sensors, or by complex digital or microcontroller based temperature monitors.

## FUNCTIONAL DESCRIPTION

A representative block diagram is shown in Figure 13 and a detailed discussion on each of the functional blocks and features are given in the following sections. A complete list of the pin functions with a brief description is shown in Figure 33.



**Speed Control**

Motor speed is efficiently controlled with the use of pulse width modulation, PWM. The voltage applied to the Speed Control Input, Pin 10, provides control of motor speed by varying the drive percent on-time or conduction time of the Phase 1 and Phase 2 outputs during the commutation cycle. The control signal can be in the form of an analog voltage ranging from 1.0 V to 3.0 V, or a variable duty cycle digital pulse train having a low state maximum of 0.98 V, a high state minimum of 3.02 V, with maximum transition times 50  $\mu$ s. The control signal to PWM transfer slope or Speed Control Input voltage to drive percent on-time, is controlled by the Slope Select input, Pin 14. When connected to ground, an increase in control voltage or a digital high state results in an increase in drive output on-time. When unconnected, an increase in control voltage or a digital high state results in a decrease in drive output on-time.

A Minimum Speed Set Input is made available at Pin 6 and it has a control transfer and slope that is identical to that of Pin 10. It is designed to be programmed from an analog voltage that ranges from 1.0 V to 3.0 V, which can be derived from the Reference. The minimum speed programmed at this input will take control of the motor speed if it is greater than the speed being requested at the Speed Control input. When directly controlling motor speed from a variable duty cycle digital pulse train, the minimum speed set feature is not available and the comparator input must be disabled. A method for preserving this feature is shown in Figure 40.

Figure 1 shows the Motor Drives percent on-time versus the Speed Control input voltage with Pin 14 connected to ground for positive slope control. Notice that there are two defined outcomes when the Speed Control input voltage falls below that of the Minimum Speed Set. The first is that the motor continuously runs at the programmed minimum speed setting and this is selected by loading the Reference with 2.0 mA or more to disable auto Power Down. The second outcome is that the motor turns off after 1.0 second and this is selected by loading the Reference with 1.0 mA or less to enable auto Power Down. This gives the fan designer a choice between letting the motor run at a minimum speed or to stop running when Speed Control falls below the programmed minimum speed setting.

Figure 2 shows the Motor Drives percent on-time versus the Speed Control input voltage with Pin 14 unconnected for negative slope control. The minimum speed operating characteristics are selected in the same manner as above but with the defined outcomes now occurring when the Speed Control input voltage rises above that of the Minimum Speed Set. The speed control and minimum speed operations are shown in table form in Figure 14. Compatibility with both analog and digital control signals combined with the ability to select both the transfer slope and automatic power down, allows this device to interface into a vast array applications.

**Figure 14- Speed Control and Minimum Speed Set Operation**

Speed Control Input Pin 10		Minimum Speed Set Input Pin 6 (V)	Controlling Input	Slope Select Pin 14	Motor Drive (% Low)	Comments
Signal	(V)					
Voltage	0 to 1.0	Gnd (Disabled)	Speed Control	Gnd	0	Zero speed, power down mode if $I_{O(ref)} \leq 1.0$ mA, $t > 1.0$ s.
	>1.0 to <3.0				0 to 100	$\%t_{on} = (V_{SC} - 1.0) / 0.02$
	3.0 to 5.0				100	Maximum speed.
	0 to <1.7	1.7	Minimum Speed Set		35	Speed control voltage is less than minimum speed set.
	>1.7 to 3.0		Speed Control		35 to 100	Speed control voltage is greater than minimum speed set.
	>3.0 to 5.0		Speed Control		100	Maximum speed.
Positive Pulse	Pulse <0.98 to >3.02	Gnd (Disabled)	Speed Control		Duty Cycle	Positive pulse width duty cycle controlled from Pin 10.
Voltage	5.0 to 3.0	Tied to Pin 14 (Disabled)	Speed Control	Open	0	Zero speed, power down mode if $I_{O(ref)} \leq 1.0$ mA, $t > 1.0$ s.
	<3.0 to >1.0				0 to 100	$\%t_{on} = 100 - (V_{SC} - 1.0) / 0.02$
	1.0 to 0				100	Maximum speed.
	3.0 to >2.3	2.3	Minimum Speed Set		35	Speed control voltage is greater than minimum speed set.
	<2.3 to 1.0		Speed Control		35 to 100	Speed control voltage is less than minimum speed set.
	<1.0 to 0		Speed Control		100	Maximum speed.
Negative Pulse	Pulse >3.02 to <0.98	Tied to Pin 14 (Disabled)	Speed Control		Duty Cycle	Negative pulse width duty cycle controlled from Pin 10.

Note that if the end application does not require a programmed minimum speed or is to be controlled by a variable duty cycle digital pulse train, the Minimum Speed Set comparator must be disabled as shown in Figure 28. For applications that do not require speed control, the device can be configured to provide commutation only, yielding maximum motor speed without requiring any additional components. This is accomplished by directly grounding Pins 6 and 10, while leaving Pin 14 open.

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**Hall Inputs**

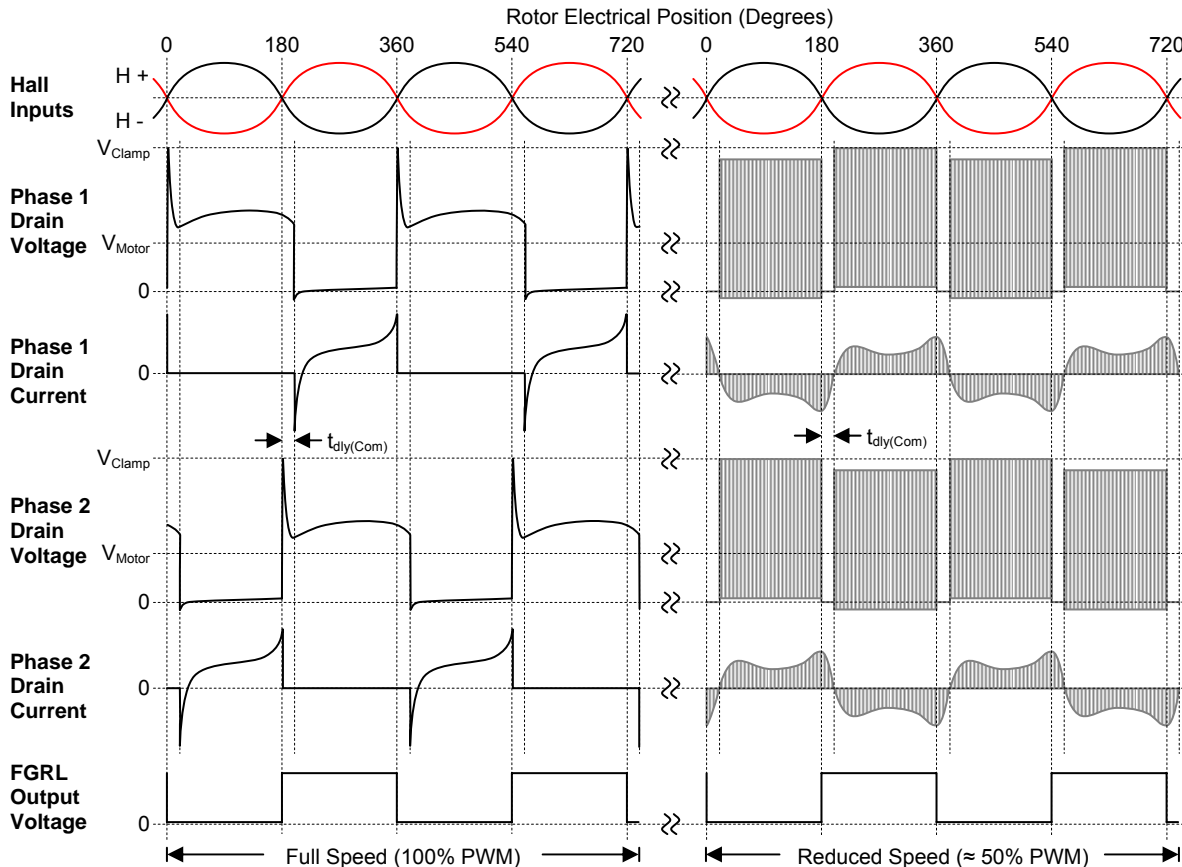
Rotor position is detected by a single Hall sensor to enable proper motor drive commutation. The H+ and H- Amplifier inputs are designed to interface with a wide variety of economical 4 pin unbuffered 'naked' or 3 pin buffered 'digital' Hall sensor types. The unbuffered sensors provide a low level differential output signal that is directly proportional to the rotors applied magnetic field. The sensor outputs connect directly to the H+ and H- inputs. The Amplifier has a differential input sensitivity of 20 mV with a common mode voltage range that extends from V<sub>DD</sub> to ground. By extending the input range to include ground, the need for offsetting the Hall output voltage with a series ground resistor is eliminated. Figures 20 through 22 show three methods of biasing unbuffered Hall sensors. The aMC8500 Hall Amplifier features enhanced noise rejection by combining a small level of input hysteresis with a propriety zero crossing detector and a timed lockout.

The buffered Hall sensors provide a high level digital output signal that changes state in direct response the rotor magnetic pole transitions. This output signal is single ended and can be applied to either the H+ or H- input while biasing the unused input to a level that is within the output voltage swing of the sensors. Economical buffered Hall sensors typically contain an NPN open collector sink only output which requires a pull-up resistor. Figures 23 and 24 show two methods for biasing buffered Hall sensors.

**Commutation**

The aMC8500 features a non-overlapping commutation delay circuit that prevents simultaneous drive conduction for reduced power supply current spikes and radio frequency interference (RFI). The non-overlap delay time (t<sub>dly</sub>) is internally set to 40 μs. The commutation waveforms and truth table are shown below in Figures 15 and 16.

**Figure 15- Two Phase, Two Step, Half Wave Commutation Waveforms**



**Figure 16- Commutation Truth Table**

Hall Inputs		System Fault	Drive Outputs		FGRL Output (Pin 15)
+(Pin 3)	-(Pin 4)		Phase 1 (Pin 16)	Phase 2 (Pin 1)	
Low	High	None	Off	Low	Low
High	Low	None	Low	Off	High
X	X	Yes	Off	Off	High

X = Don't care

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## Reference

A pinned out 3.5 V Reference with a tolerance  $\pm 5.0\%$  is made available to ease the implementation of motor control and allow additional system features. The Reference can be used to program the minimum speed set input, provide Hall sensor power, or thermal sensor voltage scaling when used in conjunction with the uncommitted Op Amp. The Reference output also provides a means to selectively enable or disable the device's automatic low current power down feature. Automatic power down is enabled if the output load current is 1.0 mA or less, and disabled if it is 2.0 mA or greater. The Reference is a source only output and therefore is not designed to sink current from a higher voltage source. It is capable of sourcing in excess of 10 mA over temperature and has short circuit protection. In applications that require additional current capability, the output can be buffered with the addition of an external PNP transistor as shown in Figure 25. This simple circuit has the advantage of moving any additional regulator power dissipation off chip but it does not maintain output short circuit protection.

## Op Amp

A fully compensated Op Amp with access to both inputs and output is provided to facilitate thermal sensor voltage scaling. The amplifier features a wide input common mode voltage range that extends from ground to 4.2 V, a DC voltage gain of 100 dB, and a 70 kHz gain bandwidth product. The amplifier output exhibits an voltage swing that extends from ground to  $V_{DD} - 1.7$  V, is capable of sinking and sourcing up to 10 mA, and is unity gain stability when driving capacitive loads. In applications where a single amplifier input can exceed the upper level of the common mode voltage range, the output will always maintain the proper state. If both inputs exceed the upper level of the common mode voltage range, a low state output phase reversal can occur and although non destructive, it may result in unexpected system behavior.

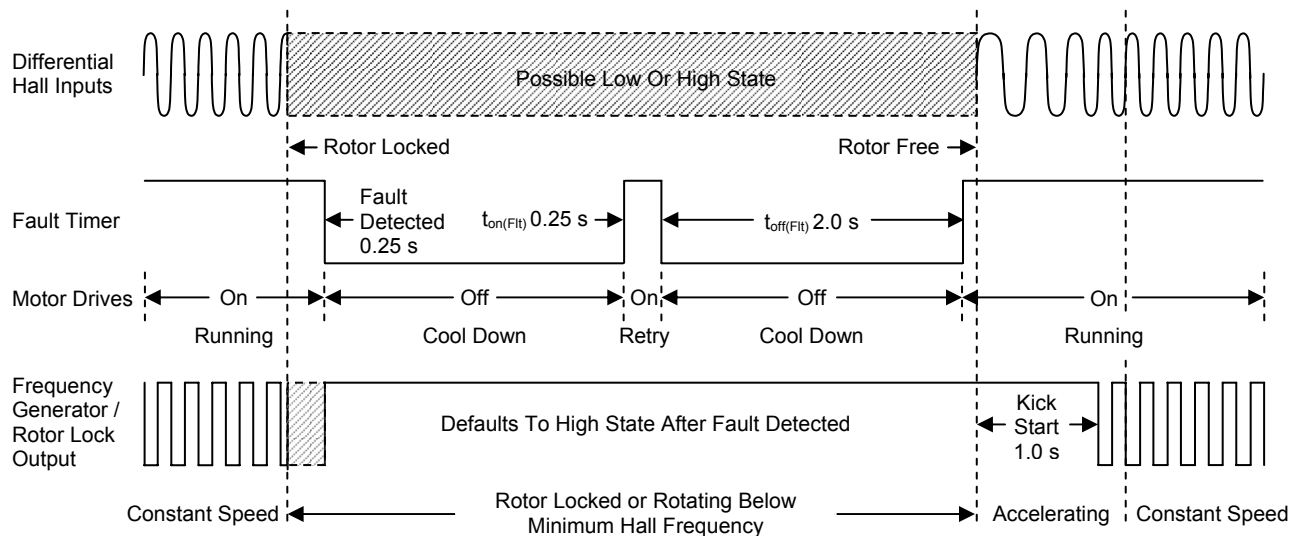
If the intended application does not require use of the Op Amp, the inputs must be connected to a fixed low impedance source in a manner that will force the output into a defined state. This will prevent the possibility of amplifying unwanted noise which can result in erratic circuit behavior. Figure 27 shows three suggested connection methods.

## Frequency Generator / Rotor Lock

Motor speed and fault signals are provided by the Frequency Generator and Rotor Lock output at Pin 15. These signals can provide diagnostic information to a thermal system controller. During normal operation, the output provides a digital square wave that switches at the Hall sensor commutation frequency. Internally, this signal is used to continuously reset the Fault Timer. If the motor encounters an obstruction, the decrease in rotational speed will result in a corresponding increase in time between reset pulses. If this time exceeds 0.25 s ( $t_{on(FIT)}$ ) a fault will be detected, which in turn will terminate motor drive and place Pin 15 into a high state, thus indicating a rotor lock condition. After an off time cool down period of 2.0 s ( $t_{off(FIT)}$ ) has elapsed, the Fault Timer circuit will apply maximum drive in attempt to restart the motor for another 0.25 s. This on/off cycling will repeat indefinitely until the motor restarts, or is commanded to stop by the Speed Control and Minimum Speed Set inputs. Upon a successful restart, Pin 15 will resume switching at the Hall commutation rate after completion of the Kick Start interval.

The Frequency Generator and Rotor Lock output consists of an N-channel open drain device and therefore requires an external pull-up resistor. An internal high gain buffer with hysteresis is used to insure that the output waveform is always rectangular even when the peak to peak Hall output signals are at a low level. The operating waveforms are shown in Figure 17.

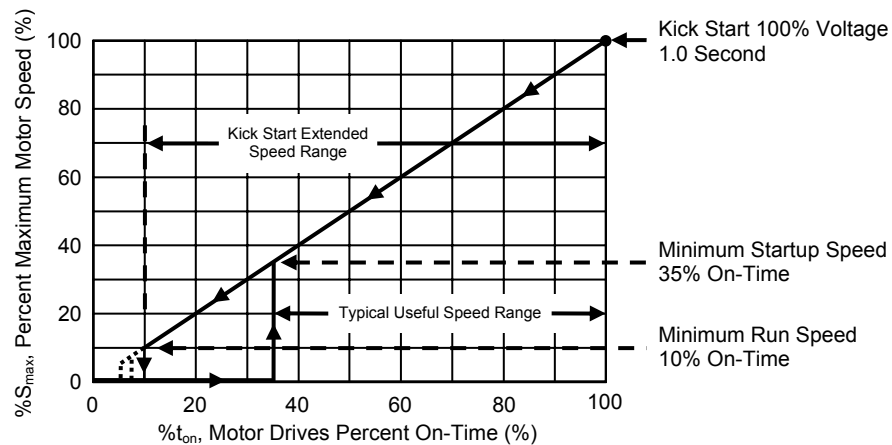
Figure 17- Frequency Generator / Rotor Lock Waveforms



## Kick Start

Most DC motors exhibit a large difference between the voltage required to insure startup and minimum speed operation. Figure 18 shows this difference as a hysteretic characteristic and is dependent upon bearing friction, lubrication, temperature, and rotor inertia. With the majority of motor controllers presently available, the applied voltage for minimum speed operation must be set equal to or greater than that required for startup. This limits the motors useful speed range from about 35 to 100 percent even though most motors will operate down to 10 percent. In order to guarantee near minimum run speed operation, the mechanical startup hysteresis must be overcome. This is accomplished in the aMC8500 by kick starting the motor in a controlled manner where full power is initially applied for a prescribed time, and control then reverts back to the level that is dictated by either the Speed Control or Minimum Speed Set input. This is graphically shown in Figures 1 and 2. With reliable starting guaranteed, the useful speed range is increased by approximately 25%, yielding lower speed operation for reduced acoustic noise and extended motor life.

**Figure 18- Typical DC Motor Startup and Run Characteristics**



The Kick Start time,  $t_{on(KS)}$ , is internally set to 1.0 second and is automatically activated whenever the motor is at rest and commanded to run, or when it is under a command to run and one of the following events takes place:

- 1) Device comes out of power down mode
- 2) Rotor was locked and the obstruction has cleared
- 3) Device recovered from a thermal shutdown
- 4) Device comes out of an under voltage lockout condition

## Current Limit

Abnormally high drive current conditions can occur if the motor is mechanically overloaded and may result in device and the drive coil overheating. During motor overload, any reduction in rotational speed reduces the generated back electromotive force, EMF, resulting in a corresponding increase in drive current. The most severe condition occurs when the rotor is locked and there is no back EMF generated. Under this condition, the drive current is limited only by the resistance total of the MOSFET switch and the driven coil. In order to protect the device and motor from abnormally high currents, a programmable Current Limit Comparator is incorporated. The comparator indirectly senses the drive current and when a maximum level is exceeded, the motor drive on-time is immediately terminated on a cycle-by-cycle basis of either the internal oscillator or the digital control signal applied to the Speed Control Input.

The current limit threshold defaults to a peak current of 1.1 A with Pin 2 open. This level can be reduced by either applying a bias voltage to Pin 2 or by connecting a single resistor from this pin to ground. Figures 11 and 12 show the current limit behavior while Figure 32 illustrates two biasing methods. The Current Limit Set input is high impedance and in most applications will require a 10 nF bypass capacitor to prevent false triggering due to noise pick up.

## Motor Drives

The aMC8500 contains two 0.5  $\Omega$  N-channel power MOSFETs that are designed to directly drive the motor coils from the Phase 1 and Phase 2 outputs. The drive characteristics are shown in Figures 9 and 10. Each output contains a 36 V zener with a series diode that connects from the drain to the gate. This configuration provides active clamp protection for the MOSFETs when switching off the inductive motor load. In applications that demand driving higher current or higher voltage motors, external MOSFET power transistors can be used. Two examples are shown in Figures 29 and 30. Although this device is designed to drive two phase half wave motors, a method for driving single phase full wave motors is shown in Figure 31.

Due to the inherent winding coupling that is present in two phase motors, the drain voltage of the off phase will be driven negative and current will be sourced from that output. This current will cause additional device heating and may affect operation of high current motors at elevated ambient temperatures. A simple solution is to place the cathode of a low forward drop Schottky diode from each drive output to ground. Likewise if the motor windings are highly inductive, the internal active clamp will be required to dissipate this energy which will also result in additional heating. This too can be eliminated with the addition of an external zener diode connected from each drain to ground. The zener breakdown voltage should be in the range of 30 V to 34 V.

## Under Voltage Lockout and Auto Power Down

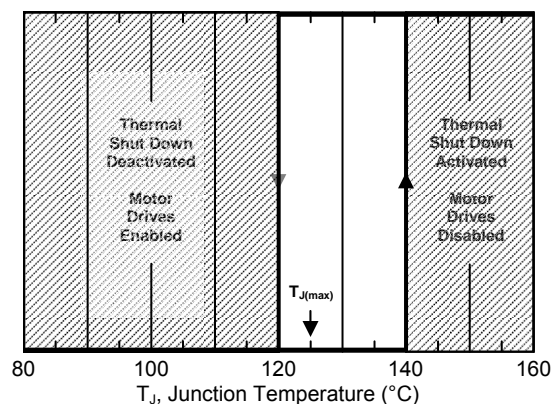
An Under Voltage Lockout circuit has been incorporated to prevent erratic device operation under low power supply conditions. This circuit enables the Motor Drives when  $V_{DD}$  rises above 4.7 V to guarantee full IC functionality, and disables the drives when  $V_{DD}$  falls below 4.2 V. The UVLO circuit has 500 mV of hysteresis to prevent oscillations as the thresholds are crossed during power-up and power-down. The IC is designed to directly drive 9.0 V and 12 V motors.

As previously discussed, the device features a selectable auto Power Down mode. This mode is automatically entered when the voltage applied to the Speed Control Input commands zero or less than zero percent on-time. When entered, the power supply current is reduced from 1.6 mA to 130  $\mu$ A. Refer to Figures 1, 2, and 14.

## Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the device in the event that the maximum junction temperature is exceeded. When activated, typically at 140°C, the Motor Drive outputs are disabled to reduce device power dissipation. This feature is intended to prevent catastrophic device failures in the event of accidental overheating. Although it is possible to operate the device above the specified maximum junction temperature of 125°C, this protection feature is not intended to be used as a substitute for proper thermal system design. When the junction temperature falls below 120°C, normal device operation resumes. Refer to Figure 19.

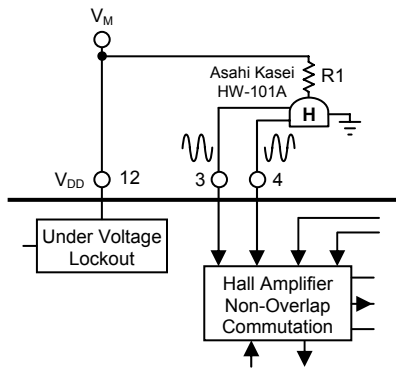
Figure 19- Thermal Shutdown Operation



## SYSTEM APPLICATIONS

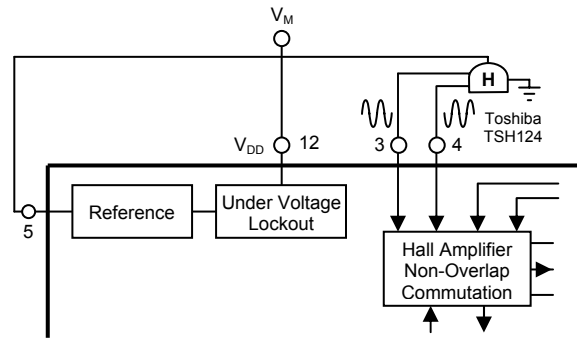
The following section shows numerous device circuit configurations and several complete fan control solutions with a brief description. For clarity, many of the circuits show only the internal functional blocks that are of interest with the associated pin numbers.

**Figure 20- Motor Supply Powered Unbuffered Hall**



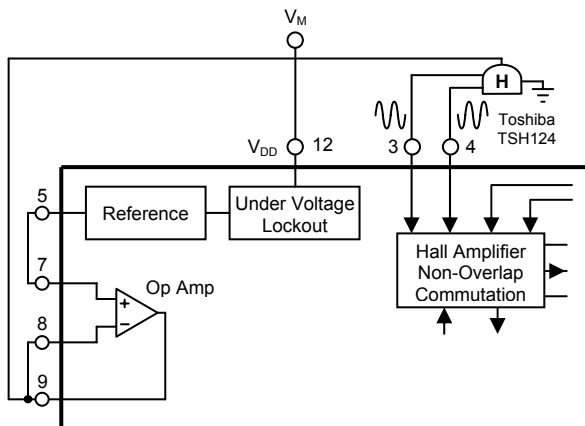
When powering an unbuffered Hall sensor from motor voltage  $V_M$ , resistor R1 is required. This resistor sets the Hall operating current and places the output within the input common mode voltage range of the Hall Amplifier.

**Figure 21- Reference Powered Unbuffered Hall**



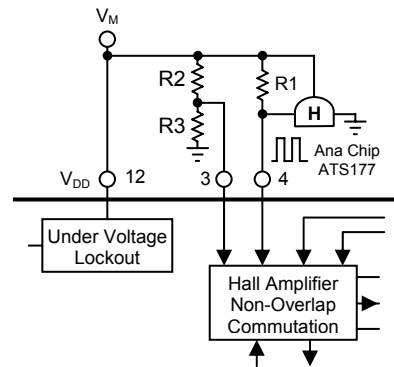
Unbuffered Hall sensors that require less than 10 mA can be powered directly from the Reference output thus eliminating the need for bias resistor R1. This bias method will disable the automatic power down feature if the sensors require more than 2.0 mA.

**Figure 22- Op Amp Powered Unbuffered Hall**



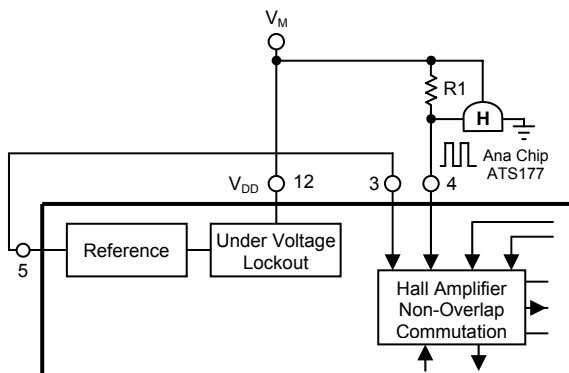
The Op Amp output can be used as alternative method for powering unbuffered Hall sensors that require less than 10 mA. This method eliminates the need for bias resistor R1 while also preserving the automatic power down feature. With this bias method the reference output is essentially unloaded.

**Figure 23- Motor Supply Biased Buffered Hall**



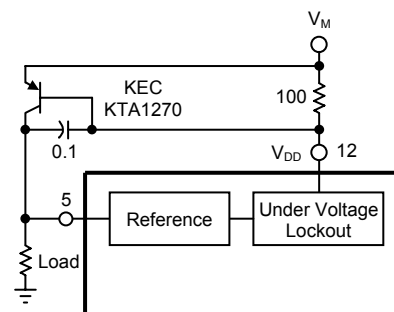
Pull-up resistor R1 is required when using buffered Hall sensors that have an open collector output. Resistors R2 and R3 bias the unused amplifier input to a level that is within its input common mode range.

**Figure 24- Reference Biased Buffered Hall**



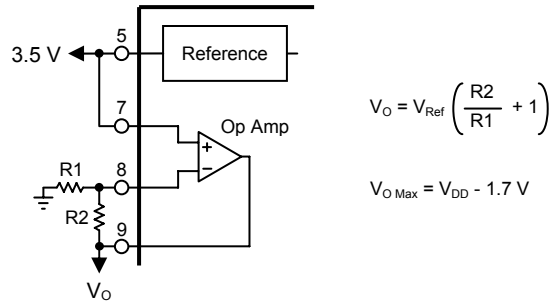
Resistor R1 is required for buffered Hall sensors with an open collector output. Resistors R2 and R3 can be eliminated by biasing the unused amplifier input from the reference.

**Figure 25- Reference Buffer**



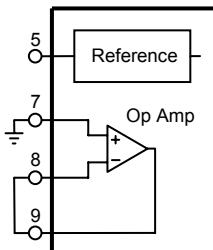
With the addition of an economical PNP transistor, the Reference output current can be boosted above 100 mA. This simple buffer circuit will not have the benefit of maintaining short circuit protection.

Figure 26- Higher Voltage Reference

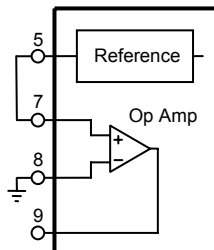


The Op Amp can be used to gain up the Reference voltage in applications that require an additional regulated voltage source. This circuit can supply up to 10 mA for powering additional circuitry or to provide a higher reference voltage. To insure that the Op Amp output maintains regulation, the maximum programmed output voltage must be less than  $V_{DD} - 1.7V$ .

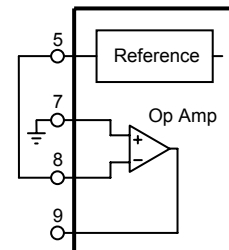
Figure 27- Connections If Op Amp Is Not Required



Unity gain amplifier configuration with the output forced low.

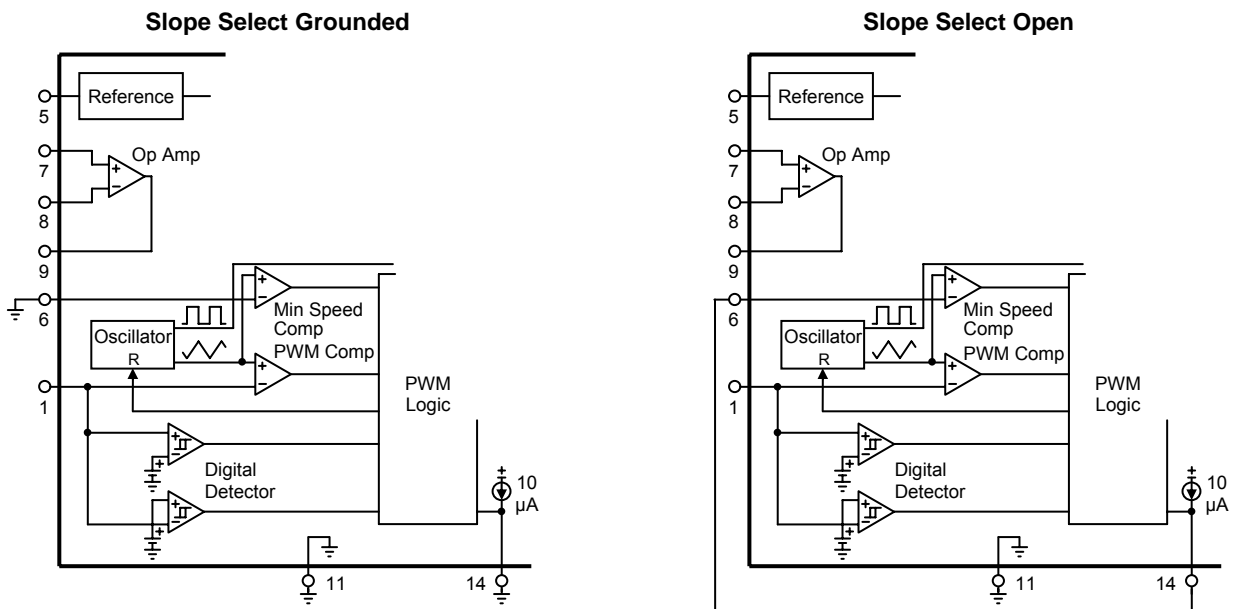


Comparator configuration with the output forced high.



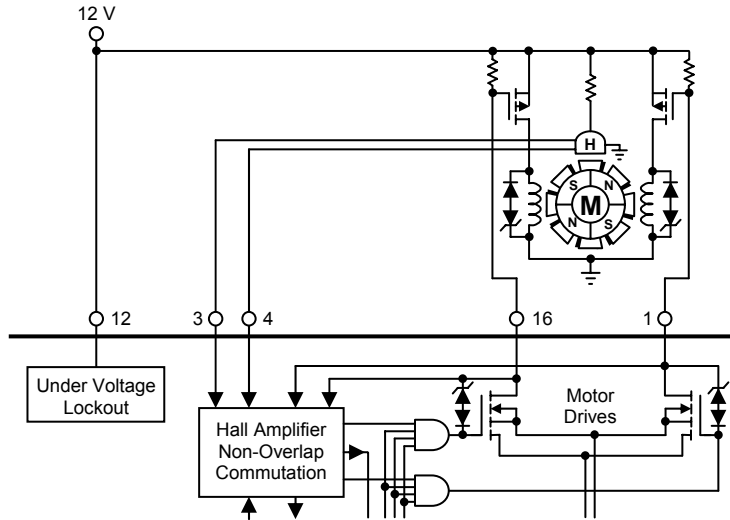
Comparator configuration with the output forced low.

Figure 28- Connections To Disable Minimum Speed Set Or Digital Signal Speed Control Operation



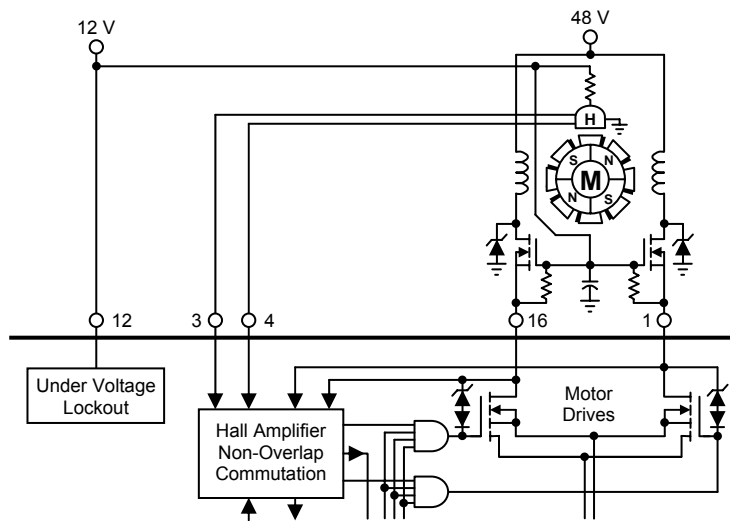
If the end application does not require a programmed minimum speed or is to be controlled by a variable duty cycle digital pulse train, the Minimum Speed Set comparator must be disabled by connecting Pin 6 directly to Pin 14.

Figure 29- Driving Higher Current Motors



The Current Limit Comparator protects the Motor Drives by limiting the output sink current to 1100 mA. In applications that require driving higher current motors, the drive current can be significantly increased with the addition of two external P-channel MOSFET. Current limit protection is not maintained since the load is no longer in series with the internal MOSFETs.

Figure 30- Driving Higher Voltage Motors

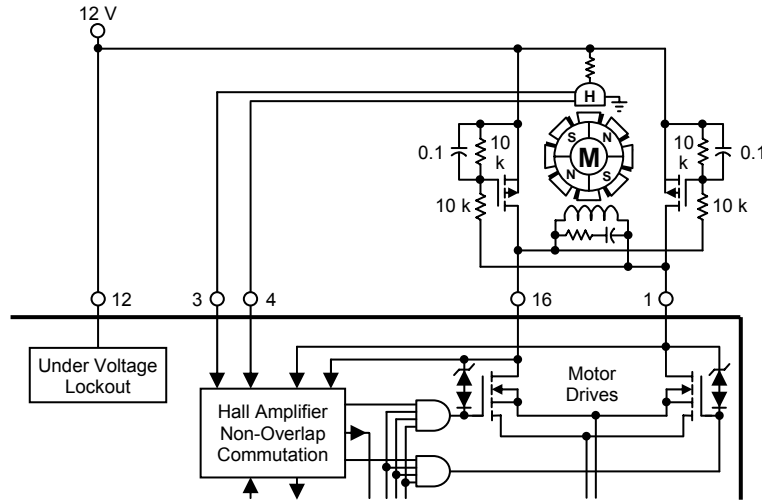


The Motor Drives are limited to a maximum of 36 V. These outputs can be cascoded with two external N-channel MOSFETs for driving higher voltage motors. The cascode configuration maintains current limit protection since the load is in series with the internal MOSFETs.

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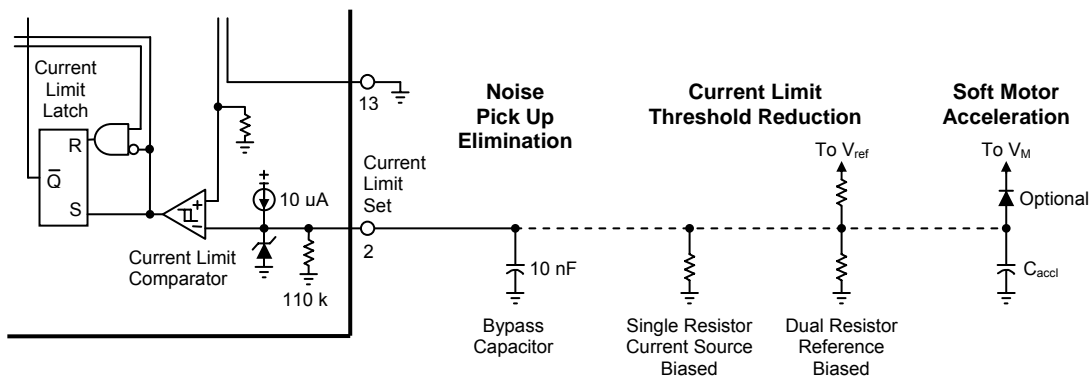
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Figure 31- Driving Single Phase Full Wave Motors



Single phase full wave motors can be driven with the addition of two external P-channel MOSFETs. With the gates cross coupled as shown above, the internal and external MOSFETs can perform as a full bridge driver. Commutation shoot through current is minimized by the internal non-overlapping delay circuit. The resistor capacitor time constant must be just long enough to prevent pulse width modulation of the two external PFETs. Current limit protection is maintained since the load is in series with the internal MOSFETs. The motor drive outputs are limited to a maximum of 36 V.

Figure 32- Current Limit Threshold Programming, Noise Pick Up and Motor Soft Acceleration



The Current Limit Set input is susceptible to noise pick up and in most applications will require a 10 nF bypass capacitor. The Current Limit Comparator threshold can be reduced by connecting a single resistor from Pin 2 to ground. This is the most economical programming method but it is somewhat less accurate than using the dual resistor method shown. This is due to the fact that the Reference Output is more accurate than the absolute values of the internal current source pull-up and terminating resistor. Motor soft acceleration during power-up can be accomplished by connecting a capacitor from Pin 2 to ground. During initial device power-up, the internal current source will charge capacitor  $C_{acc}$  thus gradually increasing the current limit threshold. The diode shown is optional and may not be required if there is sufficient time for the internal components to discharge the capacitor from when the power source is reapplied.

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Figure 33- Pin Function Description

Pin	Function	Description
1	Phase 2 Output	This output directly drives phase 2 of a unipolar motor. It is active low when the voltage applied to the Hall - input exceeds that of Hall +.
2	Current Limit Set	This input is left unconnected for a maximum motor drive current sink current of 1100 mA. The sink current can be programmed to a lower level by connecting a resistor from this input to ground. Most applications will require a 10 nF bypass capacitor on this pin to prevent noise pick up.
3	Hall +	This input connects to the output of an unbuffered differential type Hall sensor.
4	Hall -	This input connects to the output of an unbuffered differential type Hall sensor.
5	Reference Output	This is the reference output and is capable of sourcing in excess of 10 mA. It is also used to selectively enable or disable the automatic power down feature. Automatic power down is enabled if the reference load current is 1.0 mA or less, and disabled if it is 2.0 mA or more.
6	Minimum Speed Set	This input is used in conjunction with the Reference Output to program the minimum motor speed or the threshold for automatic power down. If continuous minimum speed operation is desired, the automatic power down feature must be disabled. The minimum speed set feature is not available when controlling motor speed from a variable duty cycle digital pulse train and this input must be disabled by connected it to Pin 14.
7	Non-Inverting Input	This is the non-inverting input of the Op Amp. It has an operating voltage range that extends from ground to 4.2 V.
8	Inverting Input	This is the inverting input of the Op Amp. It has an operating voltage range that extends from ground to 4.2 V.
9	Op Amp Output	This is the Op Amp output and it is capable of sinking or sourcing up to of 10 mA. The Op Amp can be used in conjunction with the Reference for scaling a speed control signal derived from a temperature sensor.
10	Speed Control Input	A voltage level that ranges from 1.0 V to 3.0 V or a variable duty cycle pulse is applied to this input for controlling the motor speed. A positive or negative speed control slope can be selected via Pin 14.
11	Signal Gnd	This pin is the ground return for the control circuitry. It connects directly to the power source ground terminal. Internally this pin connects to the device substrate and the exposed thermal pad.
12	V <sub>DD</sub>	This pin is the control circuit positive supply. It connects to the power source positive terminal.
13	Power Ground	This pin is the ground return for the motor drive MOSFETs. It connects to the power source ground terminal.
14	Slope Select	This input selects between a positive or a negative speed control slope. When connected to ground, an increasing voltage at Pin 6 or 10 increases motor speed. When not connected, an increasing voltage at Pin 6 or 10 decreases motor speed. This input has an internal 10 $\mu$ A current source pull-up.
15	Freq. Generator / Rotor Lock	This output provides a digital square wave signal that switches at the Hall sensor frequency and is active low when the voltage applied to the Hall - input exceeds that of the Hall +. If the motor turns too slow or is stalled, the output will assume a high state. This is an active low open drain output and it requires a pull-up resistor.
16	Phase 1 Output	This output directly drives phase 1 of a unipolar motor. It is active low when the voltage applied to the Hall + input exceeds that of Hall -.

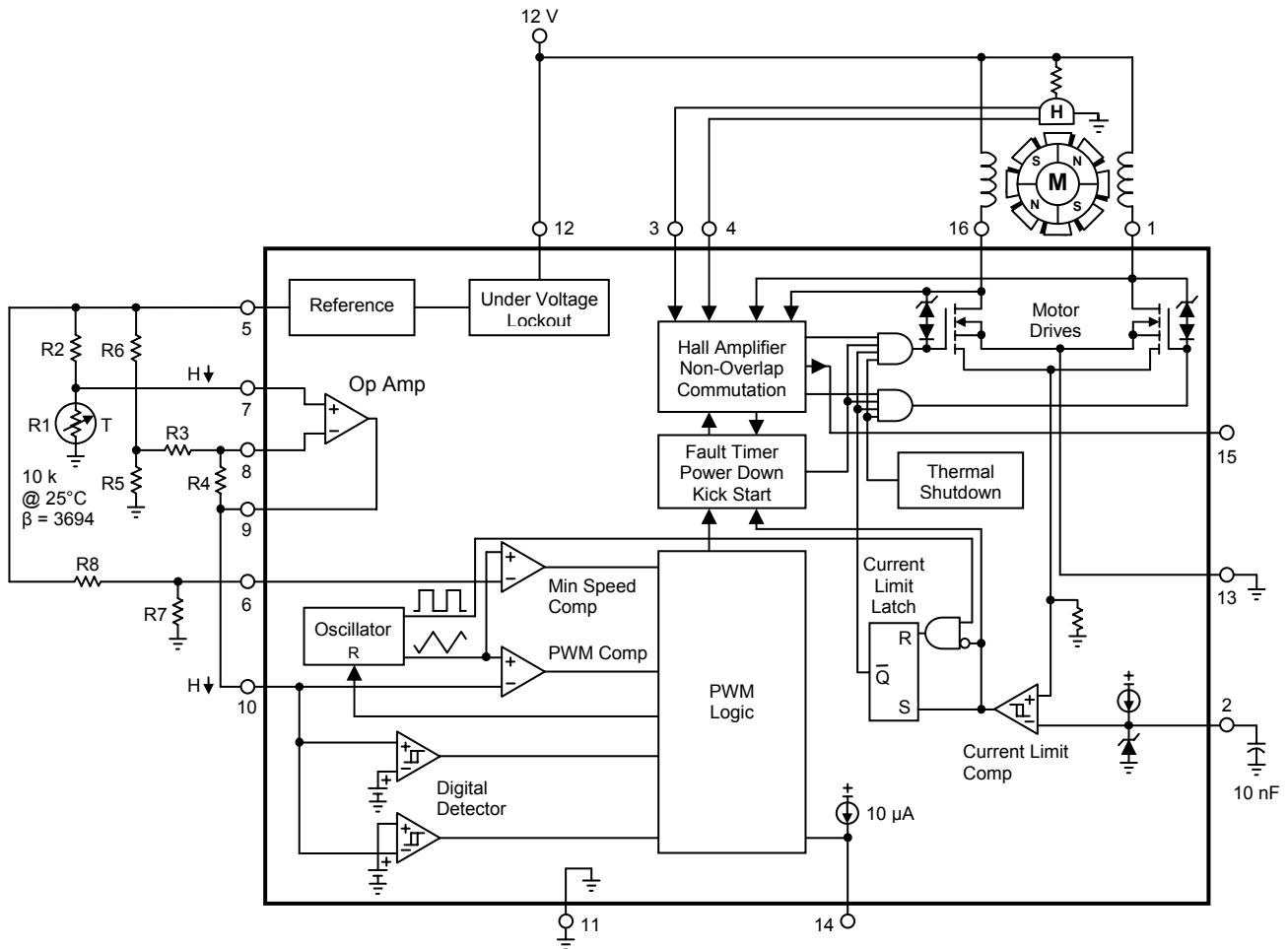
**Layout Considerations**

High frequency printed circuit layout techniques are required to prevent pulse jitter and the possibility of erratic operation. This can be caused by excessive noise pick-up imposed upon the Hall or Error Amplifier inputs. The printed circuit layout should contain as much copper ground as possible with separate low current signal and high current motor drive grounds that return back to the power supply input filter capacitor. Ceramic 0.1  $\mu$ F bypass capacitors connected close to the integrated circuit V<sub>DD</sub> and V<sub>ref</sub> pins may also be required depending upon circuit board layout and the source voltage impedance. The use of bypass capacitors will provide a low impedance path to ground for filtering out high frequency noise. The signal and power ground pins along with the exposed thermal pad must be connected together at the package. All high current loops should be kept as short as possible with wide traces to minimize the generation of radiated electro magnetic interference, EMI. Wide copper trace connections with copious amounts of foil placed under the device will greatly enhance the devices ability to dissipate power.

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Figure 34- Thermistor Sensing Variable Speed Temperature Regulator



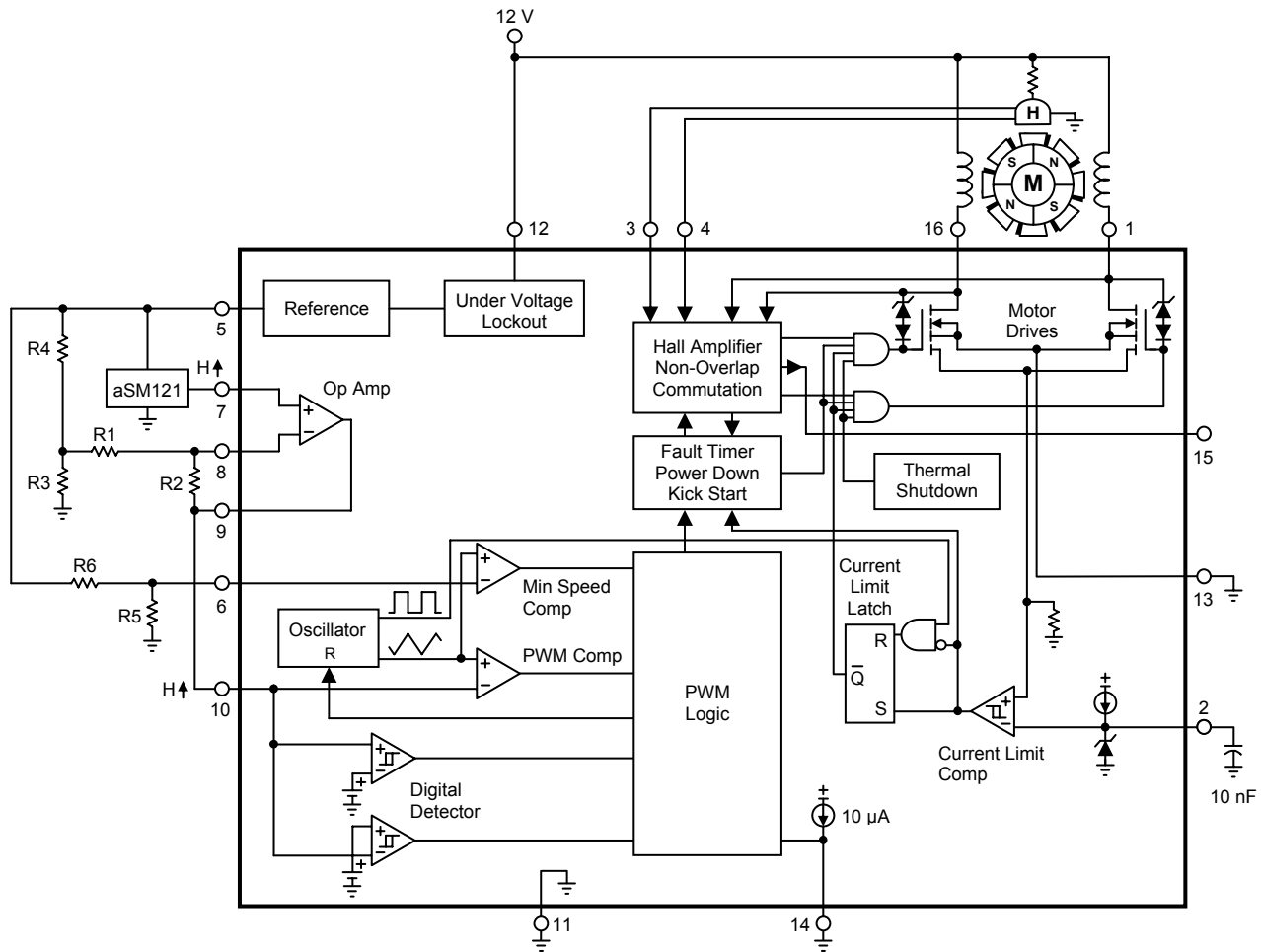
Application Requirements					Closest Standard 1.0% Resistor Values							
$T_{min}$ Speed	PWM	$T_{max}$ Speed	PWM	Minimum Speed Setting	Thermistor	Linearization	Gain		Offset		Min Speed	
°C	%on	°C	%on	%on	R1	R2	R3	R4	R5	R6	R7	R8
°C	%on	°C	%on	%on	Ω	Ω	Ω	Ω	Ω	Ω	Ω	Ω
30	35	40	100	35	10000	6650	11500	32400	1130	1150	2550	1330
30	67	38	100	35	10000	6980	11500	16200	1870	1330	2550	1330
35	30	50	100	0	10000	4990	15400	29100	1370	1300	-	-
37	30	40	100	30	10000	5900	10200	133000	1000	1000	2910	1330
40	30	50	100	30	10000	4640	14700	49900	1000	1000	2910	1330

The Op Amp used in conjunction with the Reference is extremely useful in providing voltage gain and offset to condition the thermistor signal so that it can drive the Speed Control Input. The table shows five different application requirements with the calculated closest standard 1.0% resistor values. In each example, the required motor speed or PWM %on is defined for two sensor temperatures along with a minimum speed setting. In the third application, the minimum speed set input is not required and the comparator must be disabled by connecting Pin 6 to Pin 14. Note that the total Reference load current must exceed 2.0 mA in order to disable the automatic power down feature.

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Figure 35- Simistor™ Sensing Variable Speed Temperature Regulator



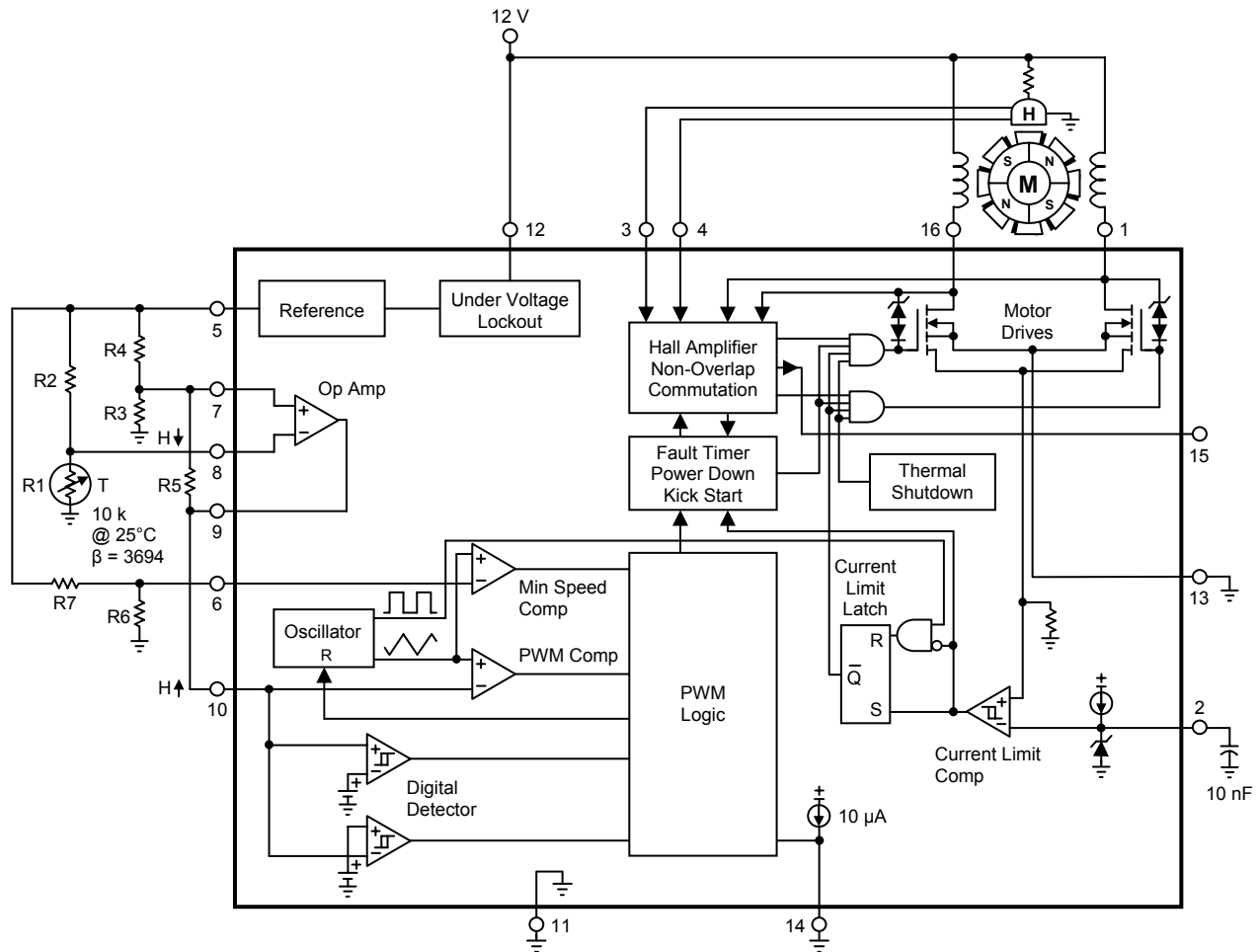
Application Requirements					Closest Standard 1.0% Resistor Values					
T <sub>min</sub> Speed	PWM	T <sub>max</sub> Speed	PWM	Minimum Speed Setting	Gain		Offset		Min Speed	
					R1	R2	R3	R4	R5	R6
°C	%on	°C	%on	%on	Ω	Ω	Ω	Ω	Ω	Ω
30	35	40	100	35	13700	16500	1400	5360	1070	1130
30	67	38	100	35	10500	76800	1370	6810	1070	1130
35	30	50	100	0	1070	8870	232	845	-	-
37	30	40	100	30	1070	48700	1330	4120	1070	1270
40	30	50	100	30	13000	169000	2320	7320	953	1130

This application circuit uses a Simistor™ solid state silicon temperature sensor that provides a precision signal of 10 mV/°C with an offset of 500 mV at 0°C. The Op Amp in conjunction with the Reference is used to gain-up and offset the signal before applying it to the speed control input. The above table shows five application requirements that are similar to those in Figure 33 with the calculated resistor values. The Simistor™ sensor allows a reduced component count when compared to the equivalent thermistor circuit. In each example, the required PWM %on or motor speed is defined for a minimum and maximum sensor temperature, and for a minimum speed setting. In the third application, the minimum speed set input is not required and the comparator must be disabled by connecting Pin 6 to Pin 14. Note that the total Reference load current must exceed 2.0 mA in order to disable the automatic power down feature.

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Figure 36- Thermistor Sensing Thermostatic Temperature Regulator



Application Requirements			Closest Standard 1.0% Resistor Values						
Speed Transition Temperature °C		Minimum Speed Setting	Thermistor	Linearization	Threshold		Hysteresis	Min Speed	
			R1	R2	R3	R4	R5	R6	R7
Min to Max	Max to Min	%on	Ω	Ω	Ω	Ω	Ω	Ω	Ω
30	28	35	10000	8060	1020	1000	158000	1070	1130
35	30	35	10000	7500	1020	1100	66500	1070	1130
38	35	0	10000	6340	1020	1070	113000	-	-
40	38	30	10000	5760	1050	1100	180000	1070	1270
45	40	30	10000	4990	1050	1130	73200	1070	1270

Thermostatic control can be accomplished by configuring the Op Amp as a non-inverting voltage comparator. The above table shows five different application examples with the calculated resistor values. In applications 1, 2, 4, and 5, the motor will switch from the programmed minimum setting to maximum speed as the sensor temperature rises above the required transition temperature. A controlled amount of positive feedback shifts the transition temperatures to provide thermal hysteresis as the sensor cools. In the third application requirement, the motor speed switches between zero and full speed. In this case the minimum speed set input is not required and the comparator must be disabled by connecting Pin 6 to Pin 14. Note that the total Reference load current must exceed 2.0 mA in order to disable the automatic power down feature.

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Figure 38- Balanced Technology Extended (BTX) Closed Loop Speed Control

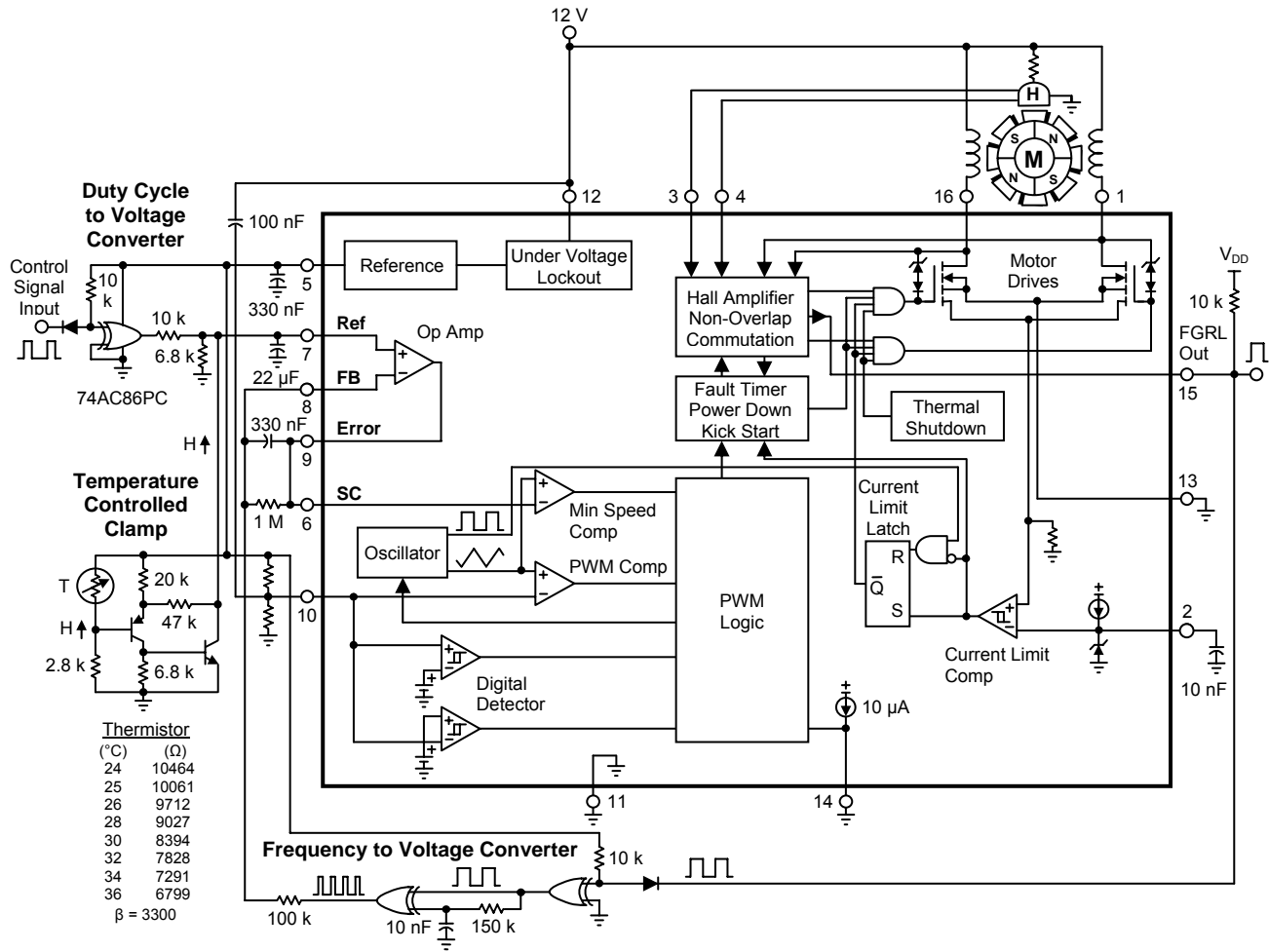


Figure 39- Fan Speed versus Control Signal Duty Cycle for Various Inlet Air Temperatures

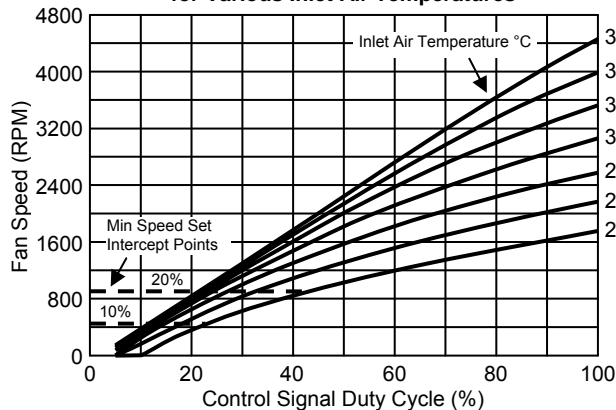
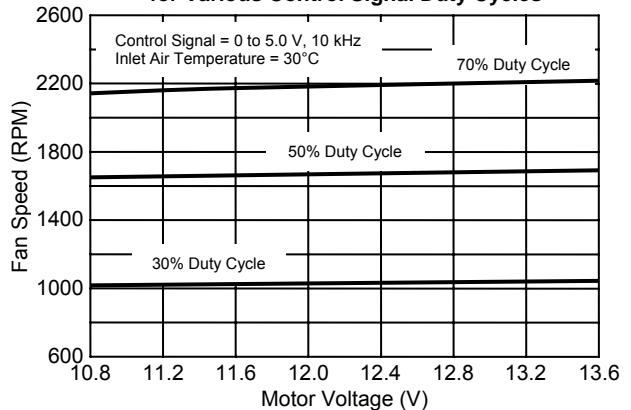


Figure 40- Fan Speed versus Motor Voltage for Various Control Signal Duty Cycles

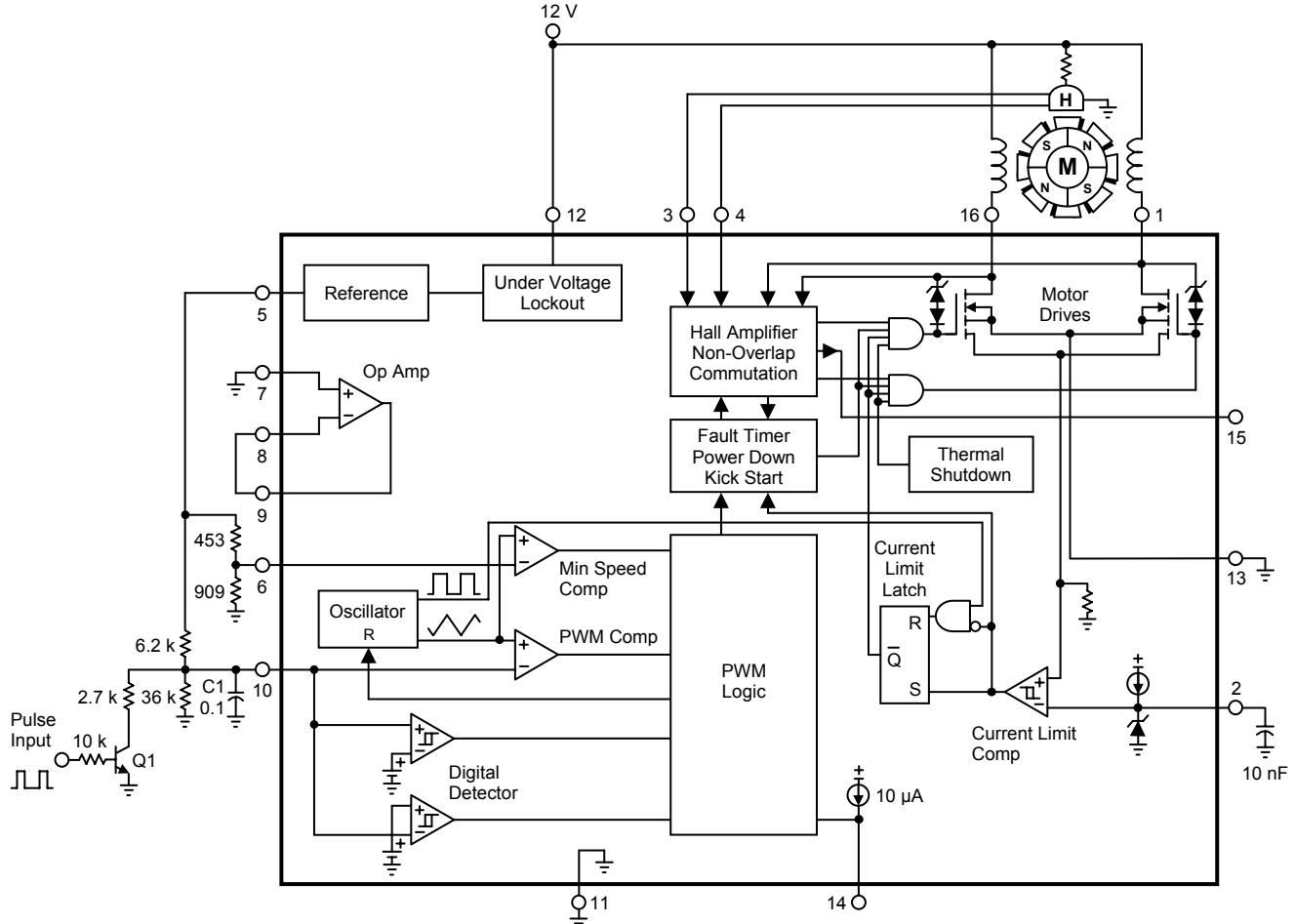


The above circuit controls fan speed in a closed loop manner that is proportional to the control signal duty cycle and inlet air temperature. A voltage indicating the required fan speed or Reference is applied to Pin 7 and is derived from the Duty Cycle to Voltage Converter and Temperature Controlled Clamp circuits. The Duty Cycle to Voltage Converter consists of an XOR gate buffer that drives a 10 k, 22 μF low pass filter, with the high state level limited by the Temperature Controlled Clamp. A voltage indicating the actual fan speed or Feedback is applied to Pin 8 and is derived from the Frequency to Voltage Converter that consists of two XOR gates. The first XOR buffers the FGRL tachometer signal and connects to the second which is configured as an edge transition one-shot that drives a 100 k, 330 nF low pass filter. The Op Amp compares the difference between the Reference and Feedback voltages and generates an Error signal that drives Pin 6 in a corrective fashion causing the fan to run either faster or slower so that the Feedback voltage level becomes the same as the Reference. Performance data is shown in the above graphs. Note that the Error signal is applied to Pin 6 instead of Pin 10 and that Pin 10 must be biased between 1.0 V to 3.0 V for proper operation.

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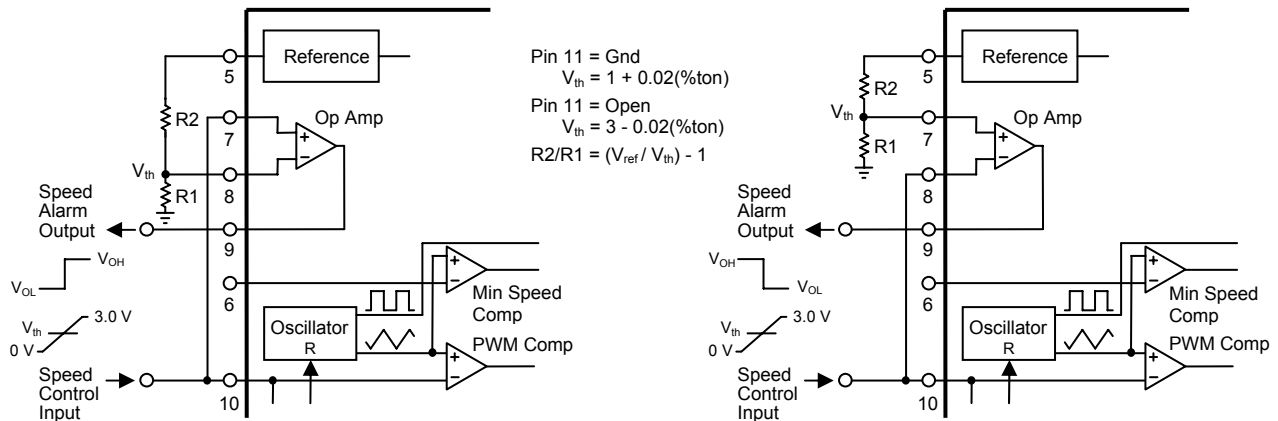
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Figure 41- Digital Pulse Speed Control with Programmable Minimum Speed Set



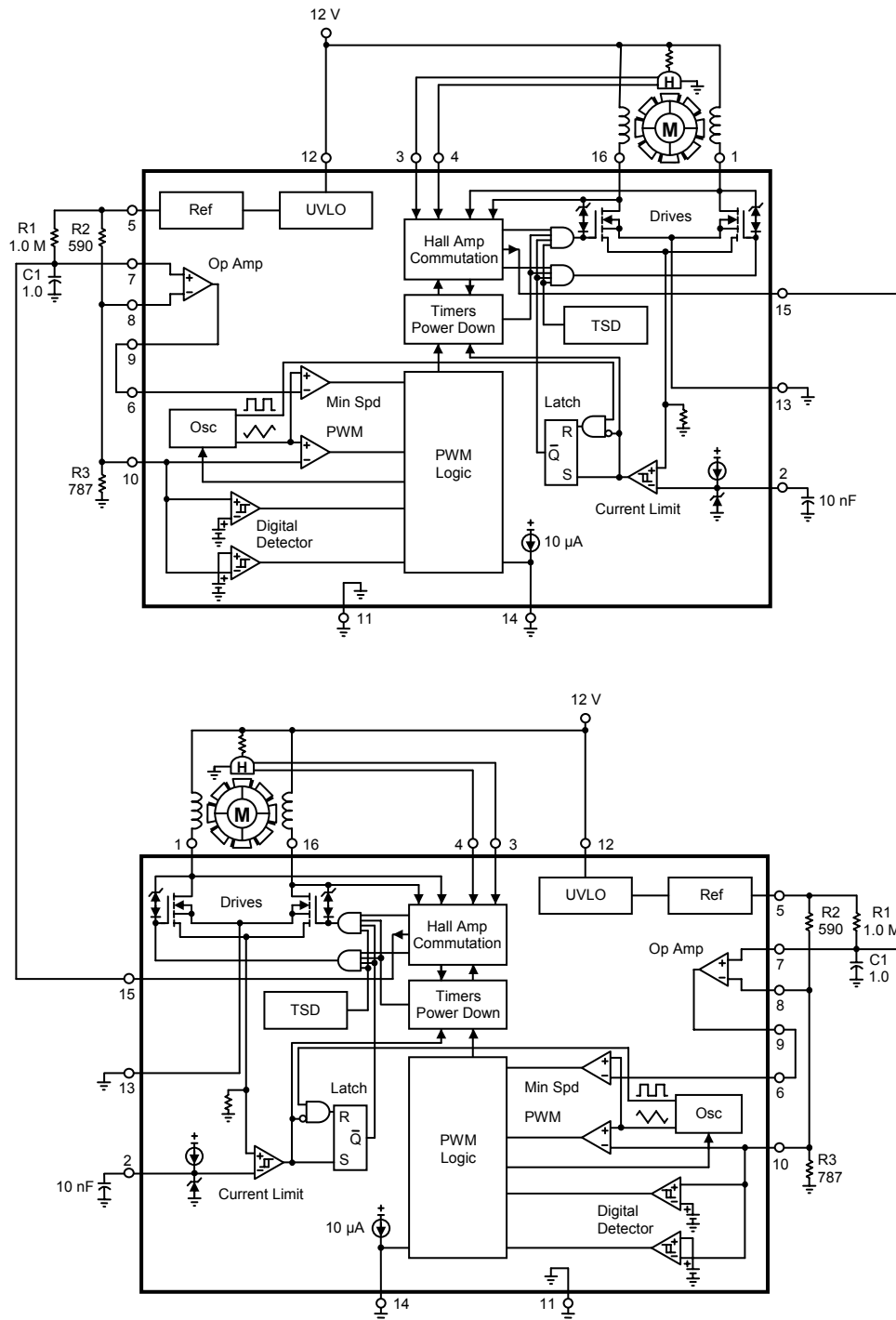
The programmable minimum speed set feature can be preserved when controlling motor speed from a varying duty cycle pulse. The above circuit uses transistor Q1, capacitor C1 and the Reference to convert the digital control signal to an analog voltage. With the resistor values shown, the voltage at Pin 10 varies between 3.0 V with Q1 off and 1.0 V with Q1 on, which represents a PWM on-time of 0% and 100% respectively. The value of capacitor C1 is dependent upon the pulse frequency and should be sized so that the ripple at Pin 10 is less than 10 mV. The Op Amp is not required in this application and is connected as a unity gain follower with the non-inverting grounded. The Minimum Speed Set input is programmed for a PWM on-time of approximately 33%. Since the Reference is always required, the programming resistors also provide a load that exceeds 2.0 mA for disabling the automatic power down feature.

Figure 42- Speed Control Alarm



The Op Amp and Reference can be used to generate a speed control alarm signal. Resistors R1 and R2 divide down the Reference output voltage to set trip threshold  $V_{th}$ . The Op Amp compares the speed control input voltage to the trip threshold and the output changes state when it is crossed. In the circuit on the left, the speed alarm output transitions from a low to high state as the Speed Control Input voltage increases. With the circuit on the right, the speed alarm output transitions from a high to low state as the speed control input voltage increases. Threshold hysteresis can be added to the circuit on the right by placing a resistor from Pin 9 to Pin 7.

Figure 43- Dual Fan Redundancy



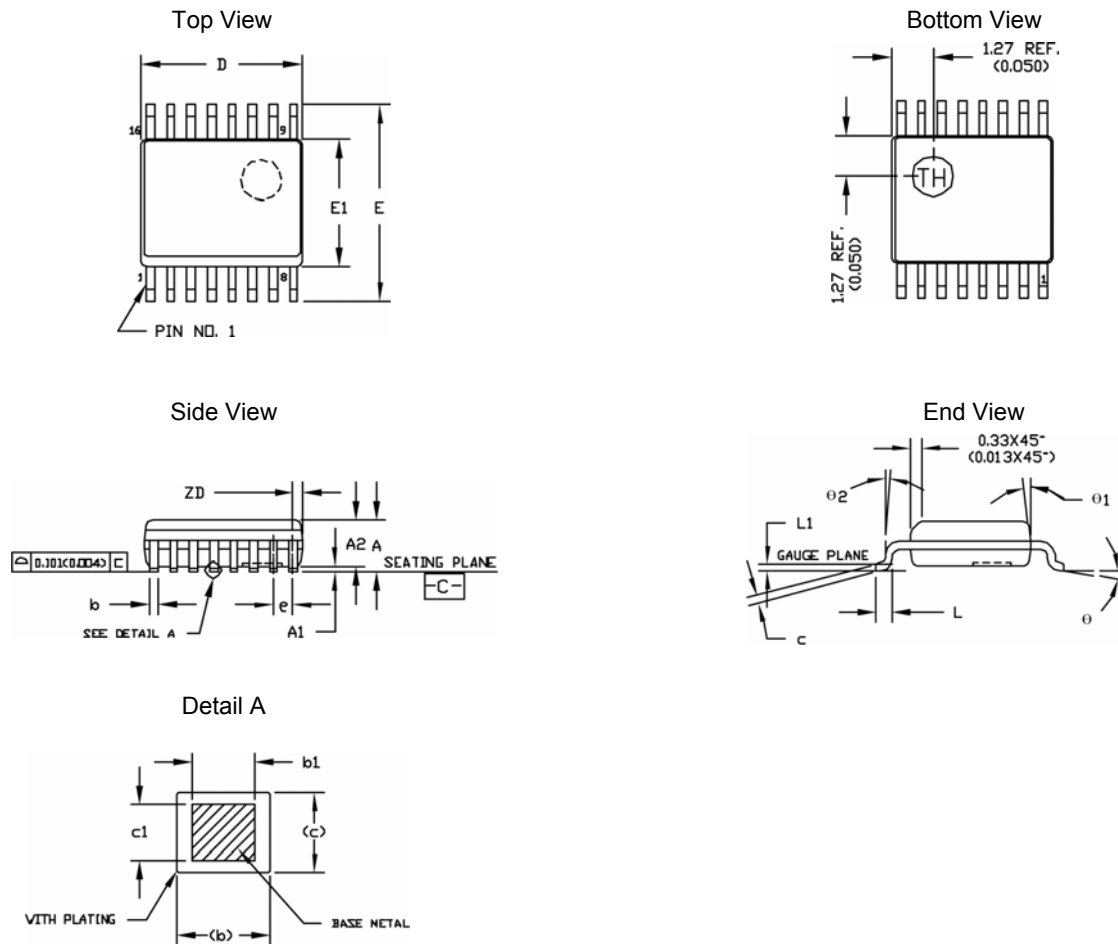
In applications that require increased system reliability, multiple cooling fans can be employed for redundancy. In this example two aMC8500s are cross coupled so that each device drives a fan while monitoring operation of the other. Resistors R2 and R3 program the Speed Control inputs to operate each fan at a 50% speed. During normal operation, the Frequency Generator / Rotor Lock outputs, Pin 15, continuously discharges their respective C1 capacitors. In the event that one fan should fail, Pin 15 will allow R1 to charge C1 above 2.0 V. This causes the Op Amp output to drive the Minimum Speed Set input above 3.0 V for maximum speed on the remaining fan. The values for resistors R2 and R3 are chosen so that each Reference Output is loaded in excess of 2.0 mA in order to disable the automatic power down feature.

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Figure 44- QSOP16 Package Outline Drawing

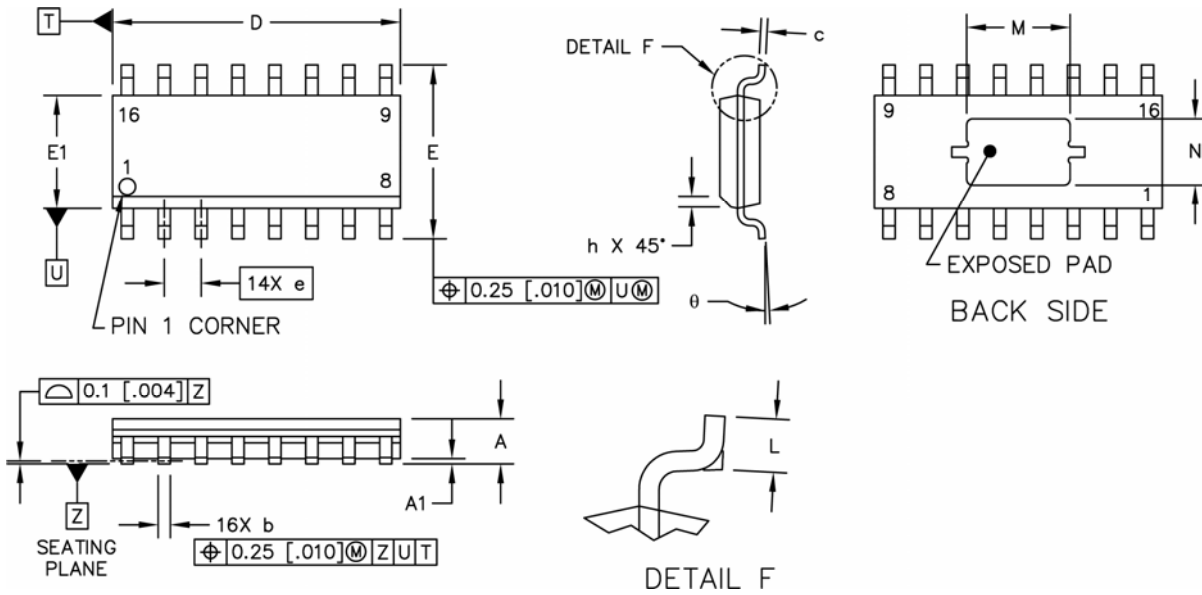


NOTE :

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.152mm (0.006") PER SIDE.
3. DIMENSION 'E' DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.254mm (0.010") PER SIDE.
4. FORMED LEAD SHALL BE PLANNED WITH RESPECT TO ONE ANOTHER WITHIN 0.101mm (0.004") AT SEATING PLANE 'C'.
5. CONTROLLING DIMENSION : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
6. 'TH' IS STAND FOR THAILAND.
7. DIMENSION  $b$  DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm (0.004") TOTAL IN EXCESS OF  $b$  DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION  $b$  BY MORE THAN 0.05mm (0.002") AT LEAST MATERIAL CONDITION.
8. DIMENSION  $ZD$  IS FOR REFERENCE ONLY. MINIMUM  $ZD$  DIMENSION SUCH THAT NO EXPOSED LEAD FRAME MATERIAL IS ALLOWED FOR END LEADS.

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.524	1.651	1.752	0.060	0.065	0.069
A1	0.101	0.177	0.228	0.004	0.007	0.010
A2	1.473 REF.			0.058 REF.		
b	0.203	-	0.304	0.008	-	0.012
b1	0.203	0.254	0.279	0.008	0.010	0.011
c	0.177	-	0.254	0.007	-	0.010
c1	0.177	0.203	0.228	0.007	0.008	0.009
D	4.80	4.902	5.003	0.189	0.193	0.197
ZD	0.228 REF.			0.009 REF.		
E	5.791	5.994	6.197	0.228	0.236	0.244
E1	3.810	3.911	3.987	0.150	0.154	0.157
L	0.406	0.635	1.270	0.016	0.025	0.050
L1	0.254 BSC			0.010 BSC		
e	0.635 BSC			0.025 BSC		
$\theta$	0°	-	8°	0°	-	8°
$\theta 1$	5°	-	15°	5°	-	15°
$\theta 2$	0°	-	-	0°	-	-

Figure 45- SOIC16 Exposed Pad Package Outline Drawing



DIM	MILLIMETERS			INCHES			NOTES
	MIN	TYP	MAX	MIN	TYP	MAX	
A	1.35		1.75	.053		.069	1. CONTROLLING DIMENSION: MILLIMETER.
A1	0.05		0.15	.002		.006	
b	0.35		0.49	.014		.019	
c	0.19		0.25	.007		.010	
D	9.8		10	.386		.393	2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
E	5.8		6.2	.228		.244	
E1	3.8		4	.150		.157	3. MAXIMUM MOLD PROTRUSION 0.15 (.006) PER SIDE.
e		1.27 BSC			.050 BSC		
h	0.25		0.5	.010		.020	
L	0.4		1.25	.016		.049	
θ			7°	0°		7°	4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.127 (.005) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
M	3.456	3.556	3.656	.136	.140	.144	
N	2.186	2.286	2.386	.086	.090	.094	

Preliminary Specification – Subject to change without notice

Preliminary Specification – Subject to change without notice



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