



AO7411

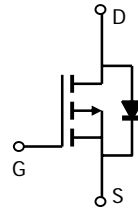
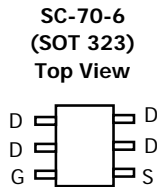
P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO7411 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. *Standard Product AO7411 is Pb-free (meets ROHS & Sony 259 specifications). AO7411L is a Green Product ordering option. AO7411 and AO7411L are electrically identical.*

Features

- $V_{DS} (V) = -20V$
- $I_D = -1.8 A (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 120m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 150m\Omega (V_{GS} = -2.5V)$
- $R_{DS(ON)} < 200m\Omega (V_{GS} = -1.8V)$



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|--------------------------------------|------------|------------|
| Drain-Source Voltage | V_{DS} | -20 | V |
| Gate-Source Voltage | V_{GS} | ± 8 | V |
| Continuous Drain Current ^A | $T_A=25^\circ C$ $T_A=70^\circ C$ | I_D | -1.8 |
| | | | -1.5 |
| Pulsed Drain Current ^B | I_{DM} | -10 | A |
| Power Dissipation ^A | $T_A=25^\circ C$ $T_A=70^\circ C$ | P_D | 0.625 |
| | | | 0.4 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|-----|-----|--------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 160 | 200 | $^\circ C/W$ |
| $t \leq 10s$ | | | | |
| Maximum Junction-to-Ambient ^A | $R_{\theta JL}$ | 130 | 160 | $^\circ C/W$ |
| Steady-State | | | | |
| Maximum Junction-to-Lead ^C | | | | |

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|---|------|-----------|------------|------------------|
| STATIC PARAMETERS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$ | -20 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$ | | | -1 -5 | μA |
| I_{GSS} | Gate-Body leakage current | $V_{DS}=0\text{V}$, $V_{GS}=\pm 8\text{V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$ | -0.4 | -0.55 | -0.8 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$ | -10 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}=-4.5\text{V}$, $I_D=-1.8\text{A}$ $T_J=125^\circ\text{C}$ | | 95 129 | 120 160 | $\text{m}\Omega$ |
| | | $V_{GS}=-2.5\text{V}$, $I_D=-1.6\text{A}$ | | 121 | 150 | $\text{m}\Omega$ |
| | | $V_{GS}=-1.8\text{V}$, $I_D=-1.0\text{A}$ | | 155 | 200 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{DS}=-5\text{V}$, $I_D=-1.8\text{A}$ | 4 | 7 | | S |
| V_{SD} | Diode Forward Voltage | $I_S=-1\text{A}$, $V_{GS}=0\text{V}$ | | -0.83 | -1 | V |
| I_S | Maximum Body-Diode Continuous Current | | | | -0.6 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, $f=1\text{MHz}$ | | 524 | | pF |
| C_{oss} | Output Capacitance | | | 93 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 73 | | pF |
| R_g | Gate resistance | $V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$ | | 12 | | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q_g | Total Gate Charge | $V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-1.8\text{A}$ | | 6.24 | | nC |
| Q_{gs} | Gate Source Charge | | | 0.52 | | nC |
| Q_{gd} | Gate Drain Charge | | | 1.84 | | nC |
| $t_{D(on)}$ | Turn-On Delay Time | $V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $R_L=5.6\Omega$, $R_{GEN}=3\Omega$ | | 10.5 | | ns |
| t_r | Turn-On Rise Time | | | 11.8 | | ns |
| $t_{D(off)}$ | Turn-Off Delay Time | | | 54.5 | | ns |
| t_f | Turn-Off Fall Time | | | 24.7 | | ns |
| t_{rr} | Body Diode Reverse Recovery Time | $I_F=-1.8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 24.7 | | ns |
| Q_{rr} | Body Diode Reverse Recovery Charge | $I_F=-1.8\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 8.2 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev3: August 2005

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

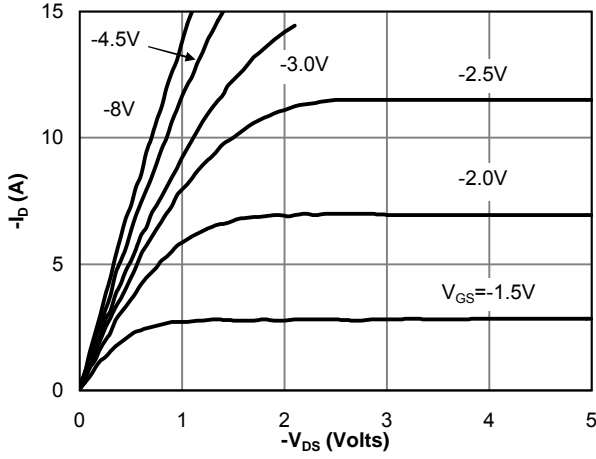


Fig 1: On-Region Characteristics

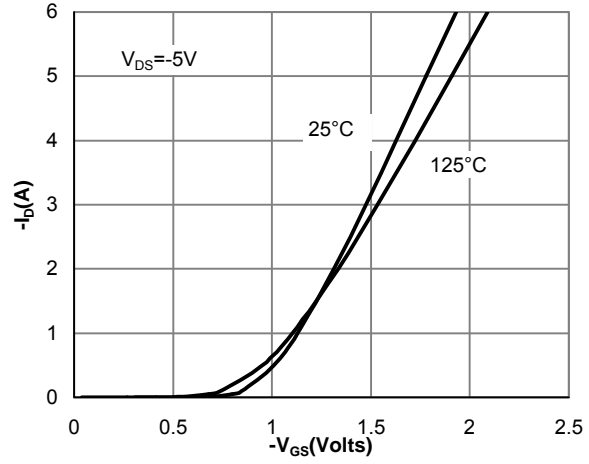


Figure 2: Transfer Characteristics

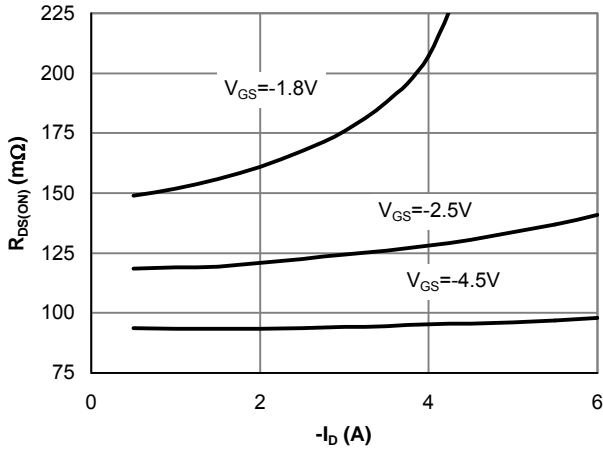


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

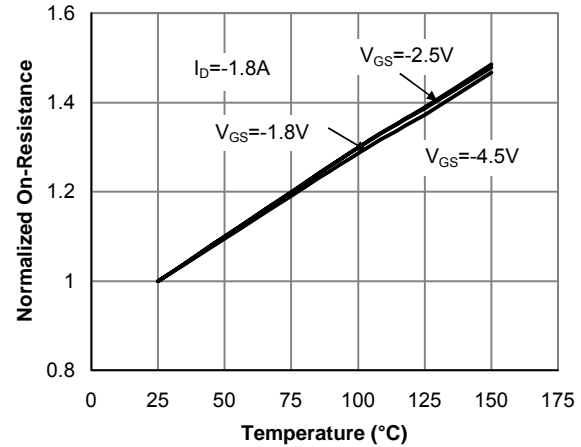


Figure 4: On-Resistance vs. Junction Temperature

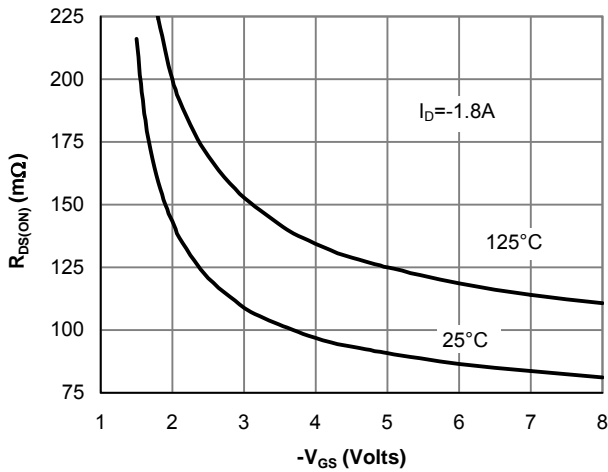


Figure 5: On-Resistance vs. Gate-Source Voltage

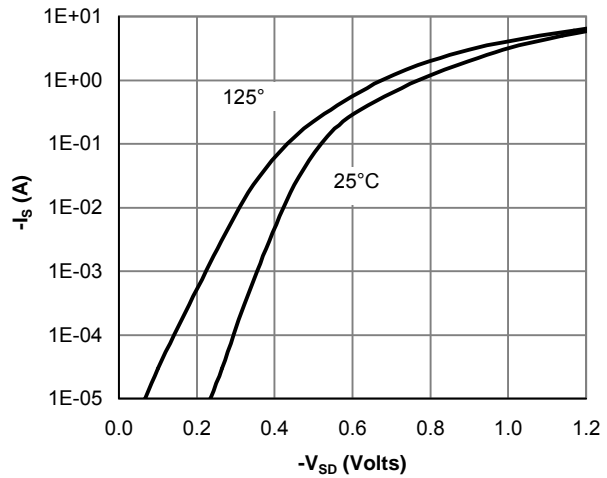


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

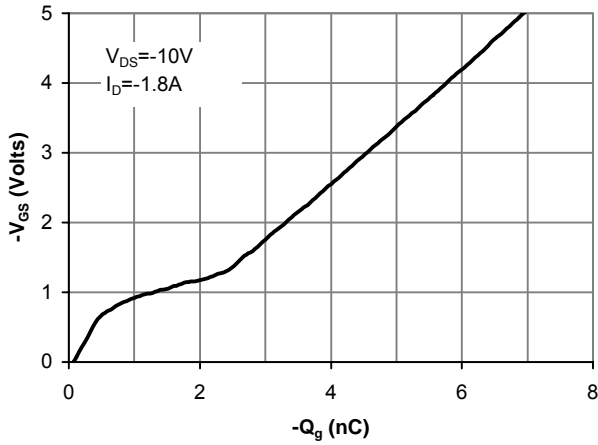


Figure 7: Gate-Charge Characteristics

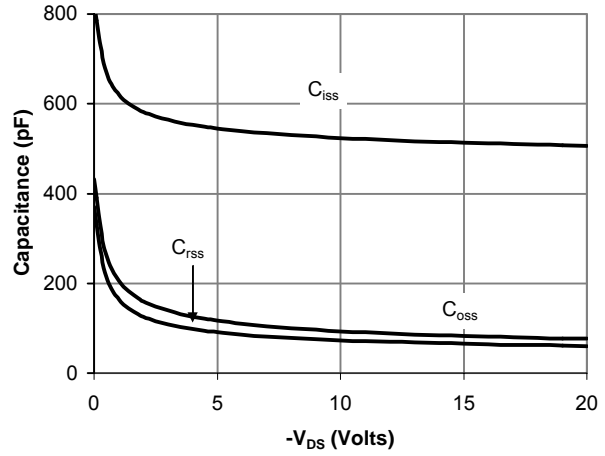


Figure 8: Capacitance Characteristics

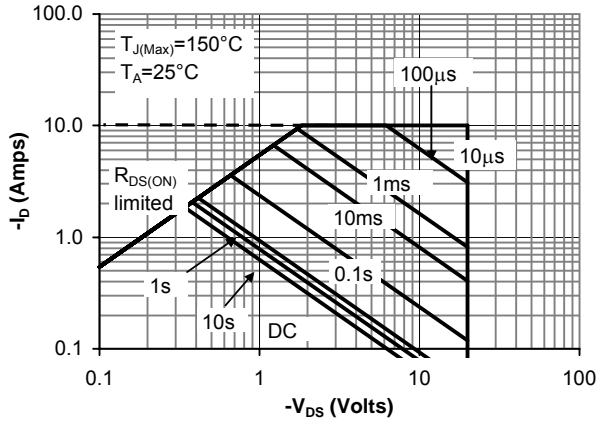


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

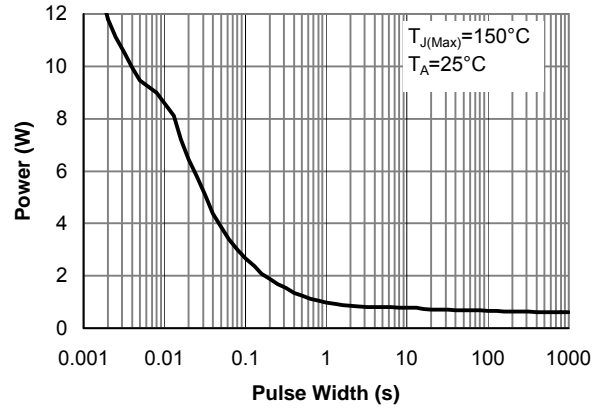


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

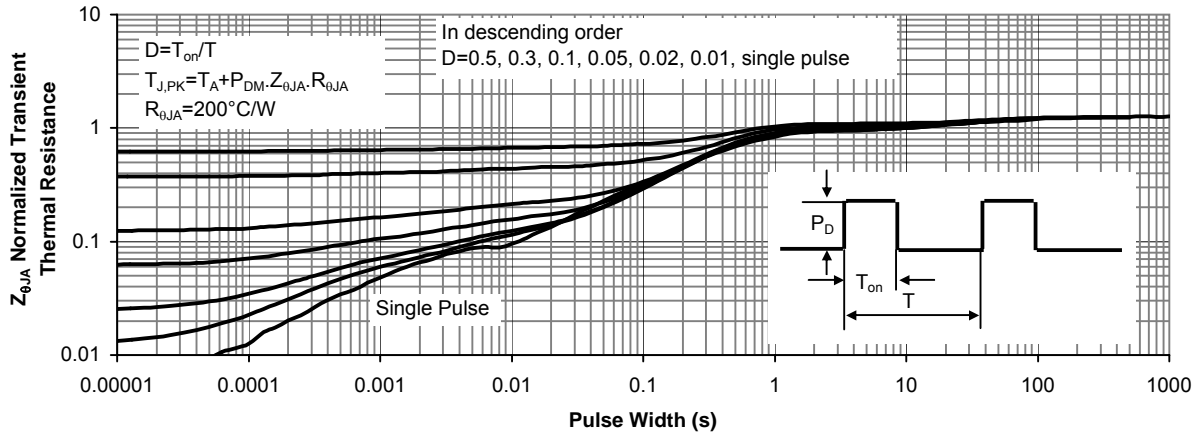


Figure 11: Normalized Maximum Transient Thermal Impedance