Stereo 280mW 8Ω Speaker Driver with Mute

Features

- Operating Voltage
  - Single Supply 3V to 7V
  - Dual Supply ±1.5V to ± 3.5V
- High Signal-to-Noise Ratio 100dB
- High Slew Rate 5V/ µs
- Low Distortion -65dB
- Output Power at 10% THD+N
  - into 8Ω 280mW
  - into 16Ω 160mW
- Large Output Voltage Swing
- Excellent Power Supply Ripple Rejection
- Flexible Mute Function
- Integrated Voltage Divider (V_{DD}/2) to Eliminate External Resistors
- Low Power Consumption
- Short-circuit Elimination
- Wide Temperature Range
- No Switch ON/OFF Clicks
- Available in 8 pin SOP or DIP Package

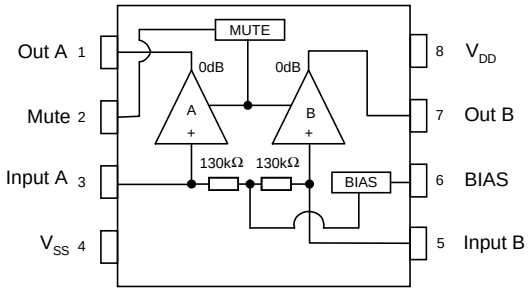
Applications

- Portable Digital Audio
- Personal Computers
- Microphone Preamplifier

General Description

The APA4801 is an integrated class AB stereo headphone amplifier contained in an SO-8 or a DIP-8 plastic package with Mute feature . Besides the common Mute feature , the APA4801 further integrates a voltage divider inside the chip . Thus , the external resistors can be eliminated . The device has been primarily developed for portable digital audio applications .

Block Diagram



Ordering Information

APA4801 □□-□□

- Handling Code
- Temp. Range
- Package Code

Package Code
J : PDIP-8 K : SOP-8
Temp. Range
I : - 40 to 85 °C
Handling Code
TU : Tube
TR : Tape & Reel

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Function Pin Description

Pin Name	I/O	Function Description
Out A	O	A channel output pin
Mute	I	Chip disable control input, high active and low for normal operating
Input A	I	A channel input terminal
V_{SS}		Power ground pin
Input B	I	B channel input terminal
BIAS	I	Right channel bias input pin
OUT B	O	B channel output pin
V_{DD}		Power input pin

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	8	V
$t_{SC(O)}$	Output Short-circuit Duration, at T_A=25°C, P_{tot}=1W	20	S
T_A	Operating Ambient Temperature range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature,10 seconds	260	°C
V_{ESD}	Electrostatic Discharge	-3000 to 3000 *1	V

Note: 1. Human body model : C=100pF, R=1500Ω, 3 positive pulses plus 3 negative pulses

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air		
	DIP-8	109	K/W
	SO-8	210	K/W

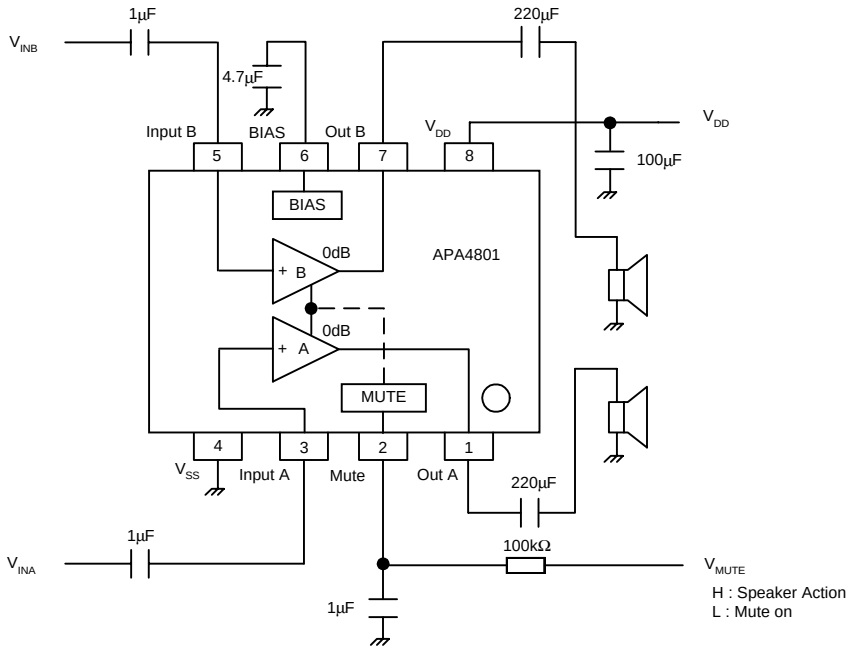
Electrical Characteristics V_{IN}=0dBV, V_{DD}=5V, T_A=25°C, f=1kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA4801			Unit
			Min.	Typ.	Max.	
V_{DD}	Power Supply Voltage		2.7		5.5	**V**
V_{DD}=5V						
I_{DD}	Supply Current	No Load		2.5		mA
$V_{I(OS)}$	Input Offset Voltage			5	50	mV

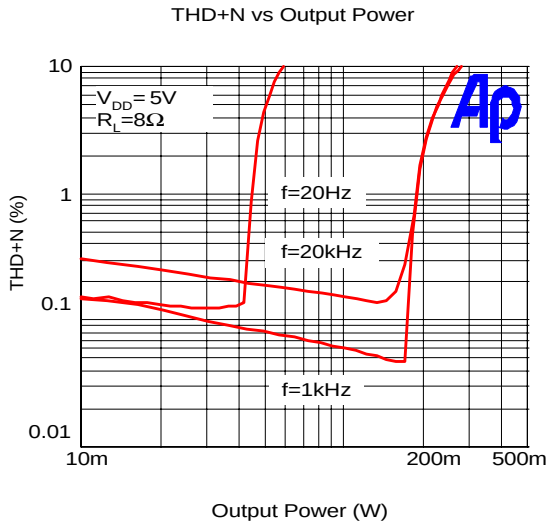
Electrical Characteristics Cont.

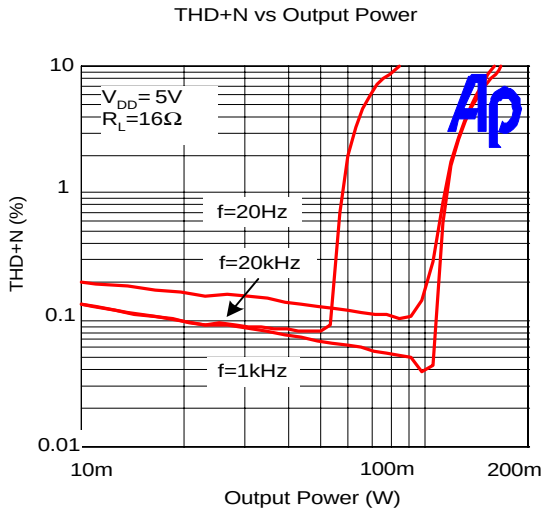
Symbol	Parameter	Test Conditions	APA4801			Unit
			Min.	Typ.	Max.	
I_{SD}	Shunt Current			200		μA
Mutel	Mute Input Voltage			0.8		V
A_{V1}- A_{V2}	Differential Channel Voltage Gain		-0.5	0	0.5	dB
ATT	Mute Attenuation	f_{IN}=1k, V_{IN} =1 Vrms		75	70	dB
AC Characteristics						
(THD+N)/S	Total Harmonic Distortion plus Noise to Signal Ratio	P_O =160mW, R_L=8Ω, f=1kHz P_O =100mW, R_L=16Ω, f=1kHz		0.05 0.05		%
P_O	Output Power	(THD+N)/S=0.1%, f=1kHz, BW<80kHz R_L=8Ω R_L=16Ω			170 100	mW
P_O	Output Power	(THD+N)/S=10%, f=1kHz, BW<80kHz R_L=8Ω R_L=16Ω		280 160		mW
PSRR	Power Supply Rejection Ratio	C_B=4.7 μF,V_{RIPPLE}=200mVrms, f=120Hz		76		dB
S/N	Signal to Noise Ratio	R_L=8Ω				μVrms
V_{DD}=3V						
I_{DD}	Supply Current	No Load		2.2		mA
$V_{I(OS)}$	Input Offset Voltage			5		mV
I_{SD}				200		μA
AC Characteristics						
I_{SD}	Shunt Current			150		μA
Mutel	Mute Input Voltage			0.8		V
A_{V1}- A_{V2}	Differential Channel Voltage Gain		-0.5	0	0.5	dB
ATT	Mute Attenuation	f_{IN}=1k ,V_{IN} = 0.5Vrms		70		dB
(THD+N)/S	Total Harmonic Distortion plus Noise to Signal Ratio	P_O =50mW, R_L=8Ω, f=1kHz P_O =25mW, R_L=16Ω, f=1kHz		0.1 0.1		%
S/N	Signal to Noise Ratio					μVrms
P_O	Output Power	(THD+N)/S=0.1%, f=1kHz, BW<80kHz R_L=8Ω R_L=16Ω		45 25		mW
P_O	Output Power	(THD+N)/S=10%, f=1kHz, BW<80kHz R_L=8Ω R_L=16Ω		80 45		mW
PSRR	Power Supply Rejection Ratio	C_B=4.7μF,V_{RIPPLE}=200mVrms, f=120Hz		76		dB

Test and Application Circuit



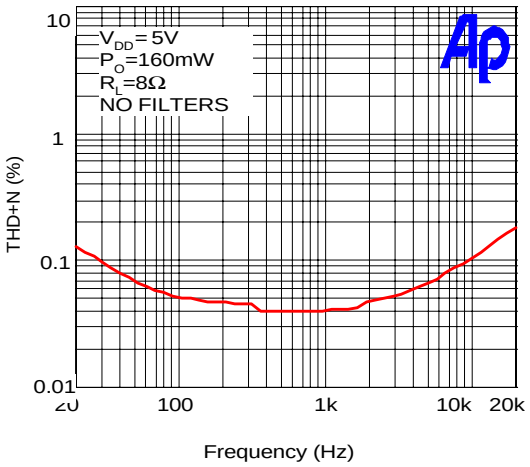
Typical Characteristics



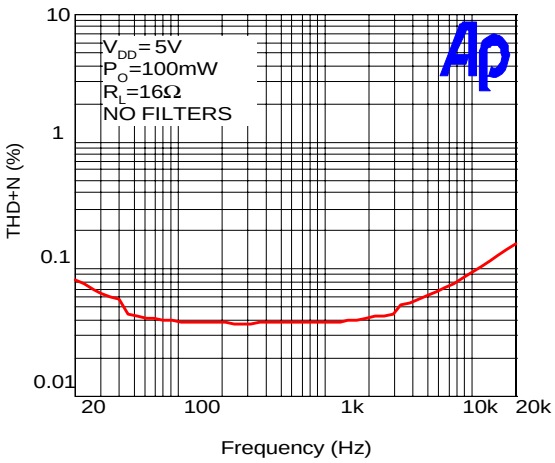


Typical Characteristics Cont.

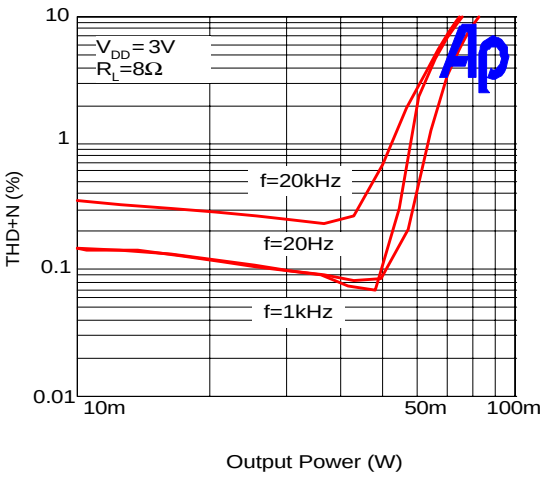
THD+N vs Frequency



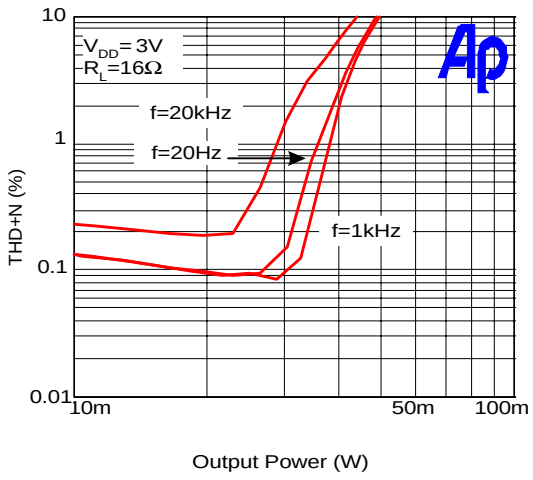
THD+N vs Frequency



THD+N vs Output Power

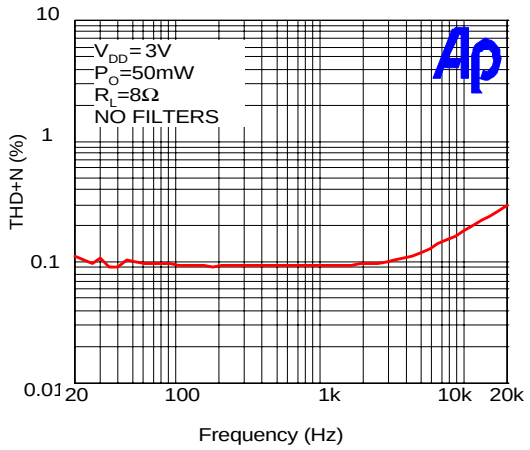


THD+N vs Output Power

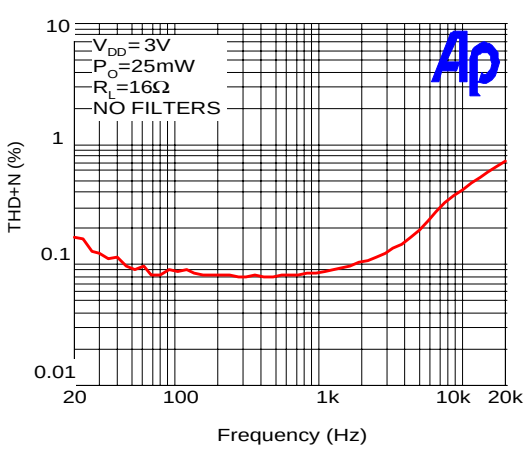


Typical Characteristics Cont.

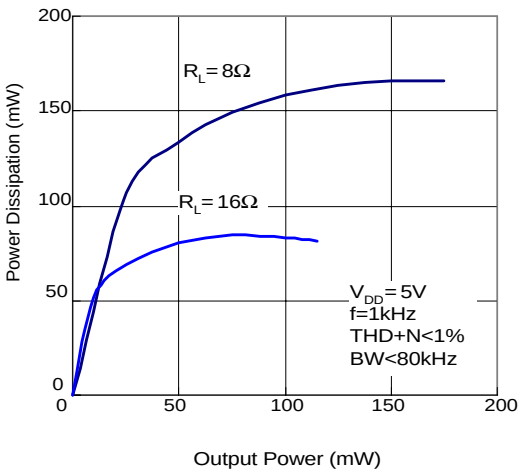
THD+N vs Frequency



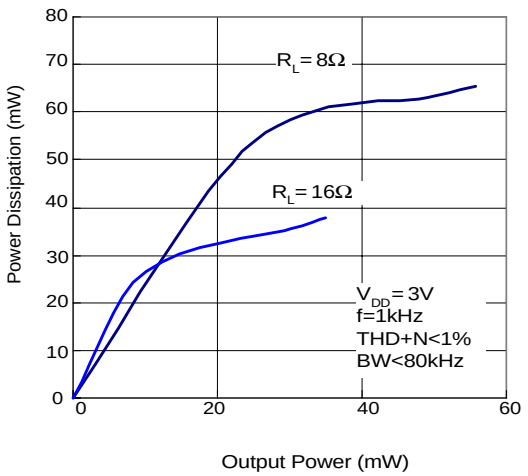
THD+N vs Frequency



Power Dissipation vs Output Power

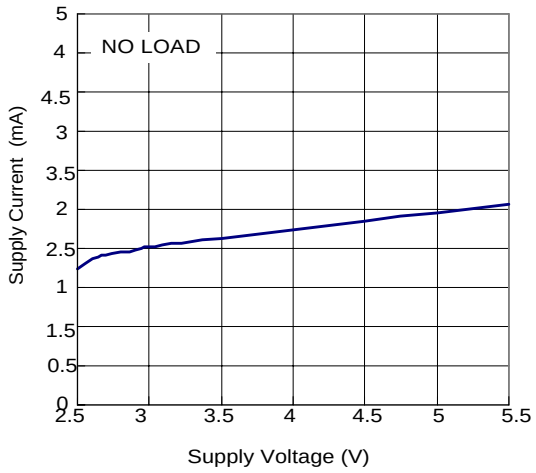


Power Dissipation vs Output Power

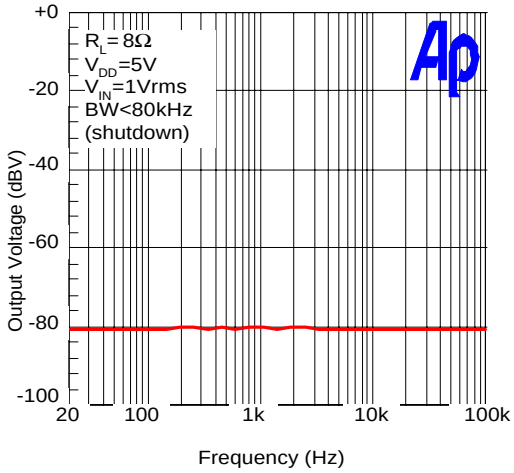


Typical Characteristics Cont.

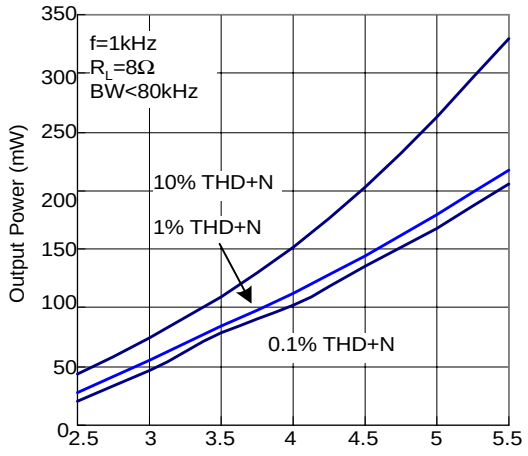
Supply Current vs Supply Voltage



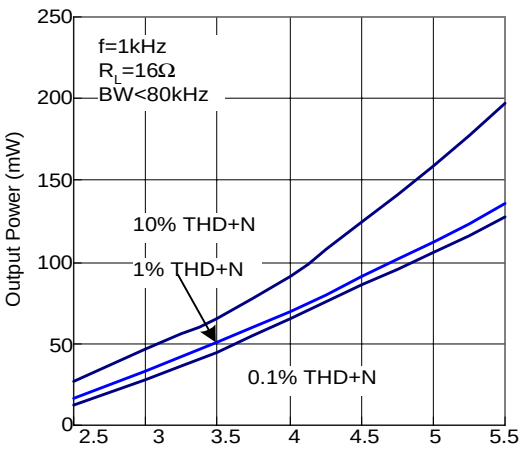
Output Voltage (Mute Attenuation)



Output Power vs Supply Voltage

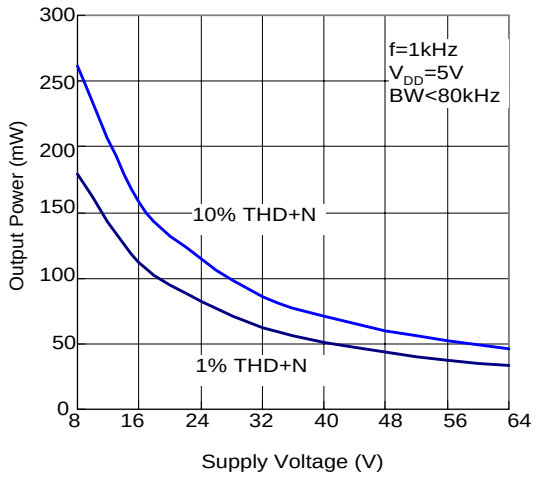


Output Power vs Supply Voltage

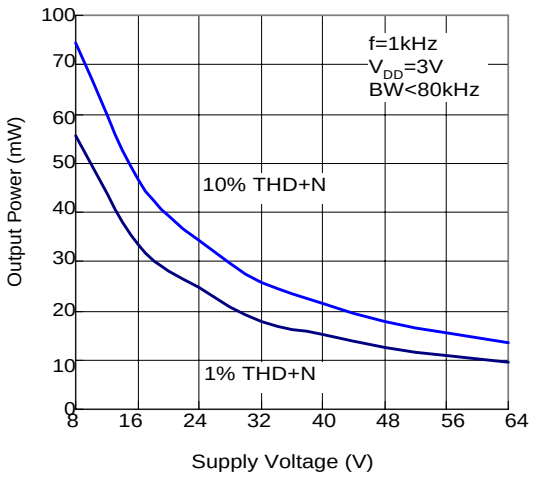


Typical Characteristics Cont.

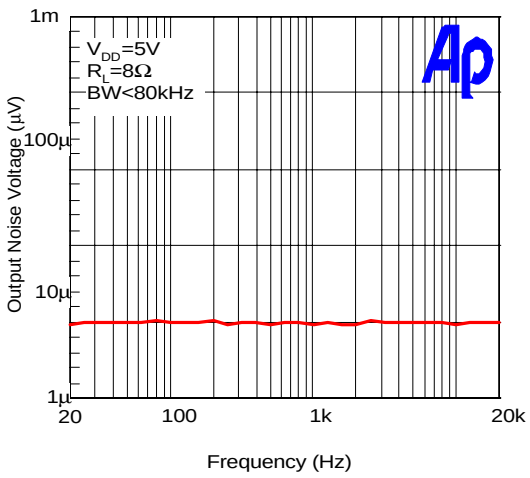
Output Power vs Load Resistance



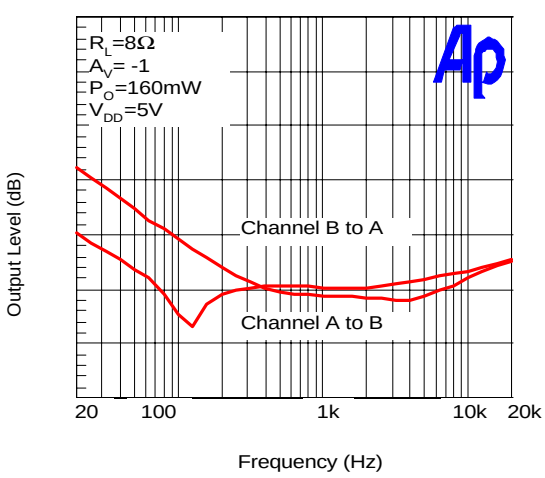
Output Power vs Load Resistance



Noise Floor

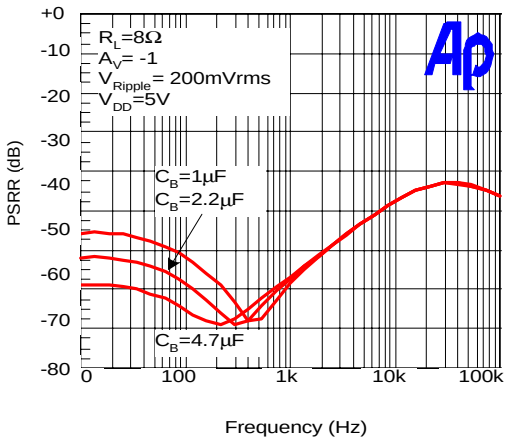


Channel Separation

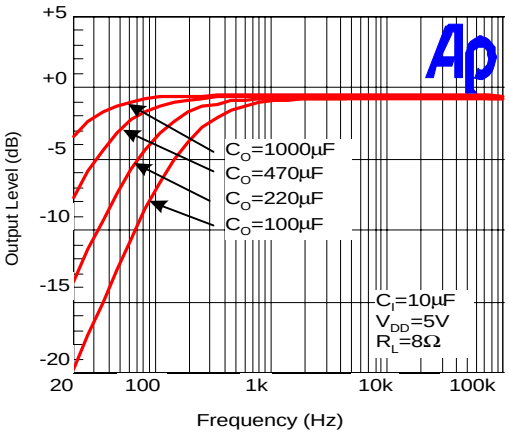


Typical Characteristics Cont.

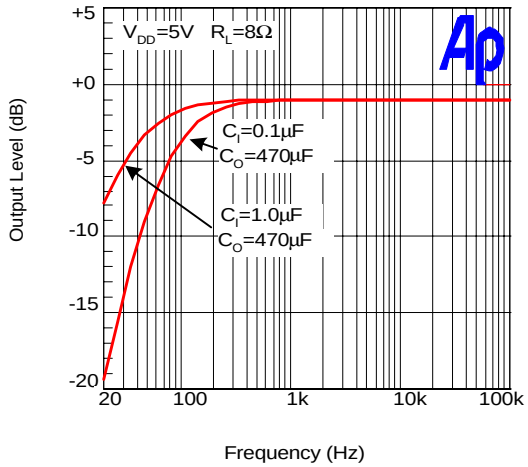
Power Supply Rejection Ratio



Frequency Response vs Output Capacitor Size



Typical Application vs Frequency Response



Application Note

Input Capacitor, Ci

In the typical application an input capacitor , Ci , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation . In this case , the external capacitor Ci and the internal resistance Ri form a high-pass filter with the corner frequency determined in the follow equation :

$$fc\ (highpass) = 1/(2\pi RiCi) \quad (1)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit . Consider the APA4801 where Ri is 130kΩ internal fixed . Equation is reconfigured as follow :

$$Ci = 1/(2\pi * 130k\Omega * fc) \quad (2)$$

And the ceramic capacitor is recommanded

Bias Capacitor, Cb

As with any power amplifier , proper supply bypassing is critical for low noise performance and high power supply rejection . The capacitor location on both the bypass and power supply pins should be as close to the device as possible . The effect of a larger half supply bias capacitor is improved PSRR due to increased half-supply stability . Typical applications employ a 5V regulator with 10µF and a 0.1µF bias capacitors which aid in supply filtering . This does not eliminate the need for bypassing the supply nodes of the APA4801 . The selection of bias capacitors , especially Cb , is thus dependent upon desired PSRR requirements , click and pop performance . The capacitor is fed from a 50kΩ source inside the amplifier. To keep the start-up pop as low as possible , the relationship shown in equation should be maintained.

$$1/(Cb * 50k\Omega) \leq 1/\{Ci * Ri\} \quad (3)$$

As an example , consider a circuit where Cb is 4.7µF , Ci is 1µF and Ri is 130kΩ . Inserting these values into the equation we get 4.26≤ 7.69 which satisfies the rule . Bias capacitor , Cb , values of 2.2µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Output Coupling Capacitor, Cc

In the typical single-supply SE configuration , an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load . As with the input coupling capacitor , the output coupling capacitor and impedance of the load form a high-pass filter governed by equation .

$$fc(highpass) = 1/(2\pi R_L Cc) \quad (4)$$

For example , a 220µF capacitor with an 32Ω speaker would attenuate low frequencies below 22Hz . The main disadvantage , from a performance standpoint, is the load impedance is typically small , which drives the low-frequency corner higher degrading the bass response . Large values of Cc are required to pass low frequencies into the load .

Optimizing Depop Circuitry

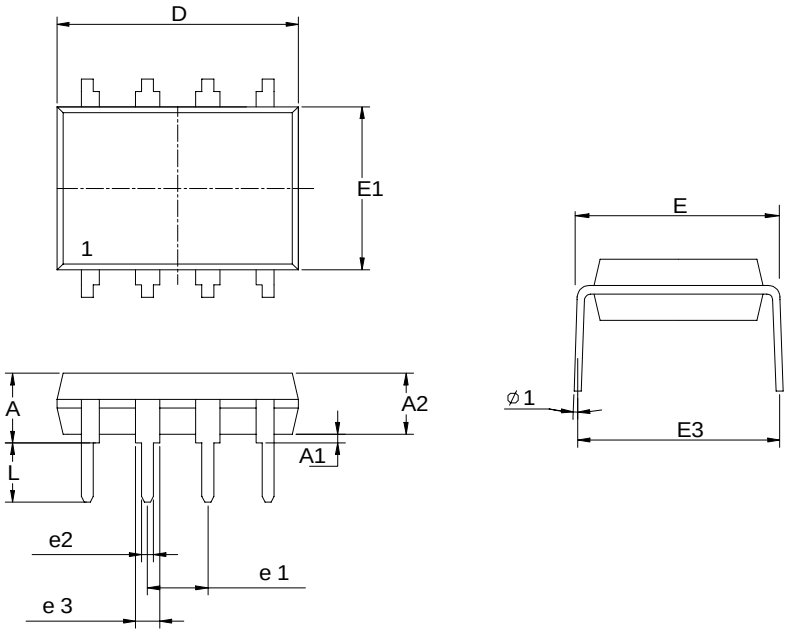
When the amplifier is in mute mode , both of the output stage and input bypass continues to be biased . And no pop noise will be heard during the transition out of mute mode .

Power Supply Decoupling , Cs

APA4801 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible . Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker . The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads . For higher frequency transients , spikes , or digital hash on the line , a good low equivalent-series-resistance (ESR) ceramic capacitor , typically 0.1µF placed as close as possible to the device V_{DD} lead works best . For filtering lower-frequency noise signals , a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended .

Packaging Information

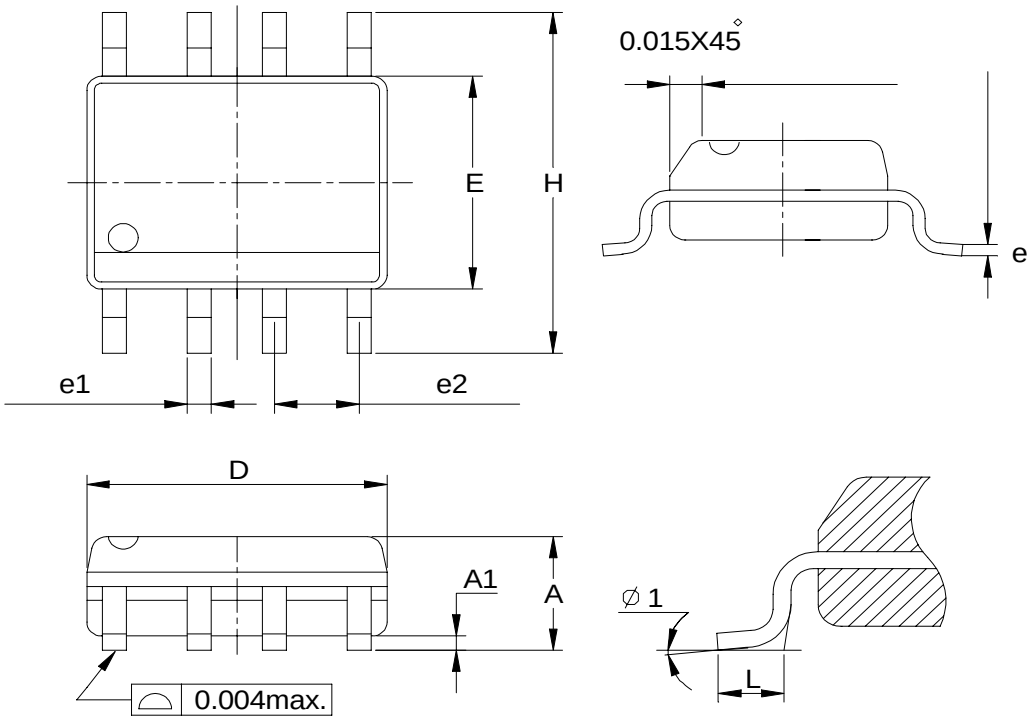
PDIP-8 pin (Reference JEDEC Registration MS-001)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	3.68	0.115	0.145
D	9.02	10.16	0.355	0.400
e1	2.54BSC		0.100BSC	
e2	0.36	0.56	0.014	0.022
e3	1.14	1.78	0.045	0.070
E	7.62 BSC		0.300 BSC	
E1	6.10	7.11	0.240	0.280
E3		10.92		0.430
L	2.92	3.81	0.115	0.150
ϕ 1	15°		15°	

Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)



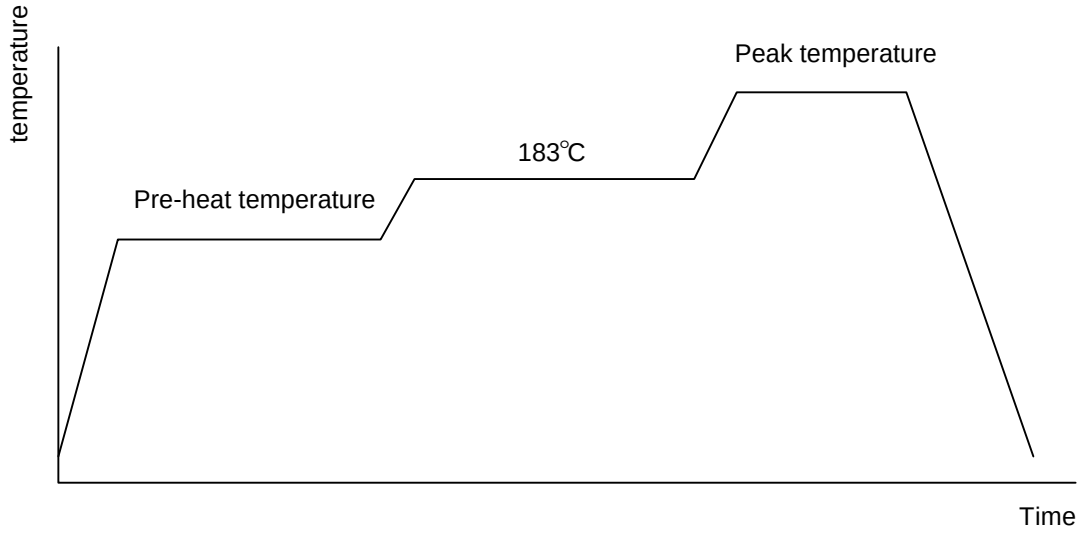
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	0°	8°	0°	8°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2500 devices per reel

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

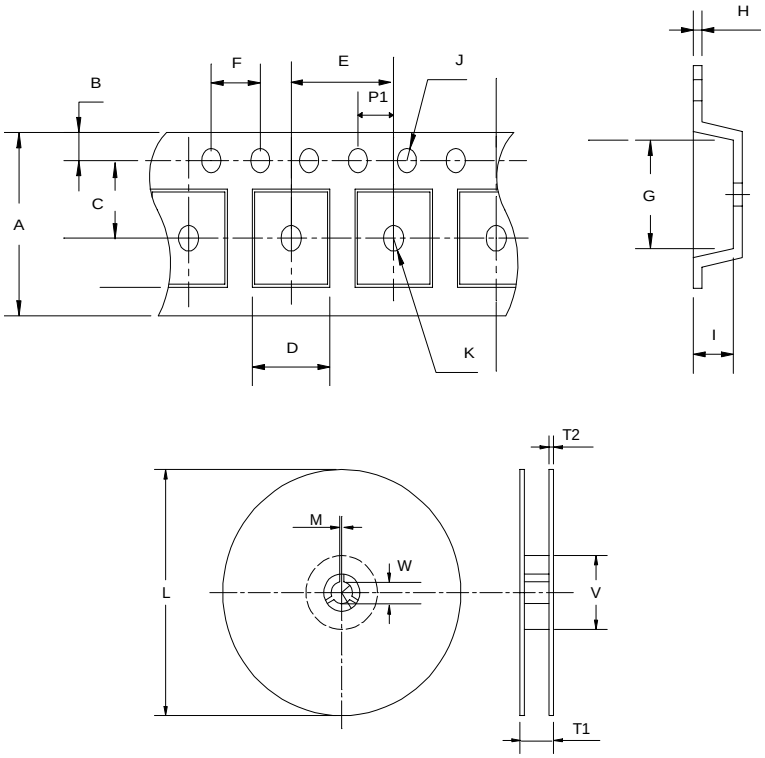
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	E	B	C	J	K	F	P1	D
SOP 8N	12 + 0.3 12 - 0.1	8.0 ± 0.1	1.75± 0.1	5.5± 0.1	1.55± 0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1
Application	G	I	H	L	V	W	M	T1	T2
SOP 8N	5.2 ±0.1	2.1 ± 0.1	0.3±0.013	330±1	100±1	13+0.5 13 -0.1	2.2±0.1	12.5± 0.5	2.0 ± 0.2

(mm)

Cover Tape Dimensions

Carrier Width	12
Cover Tape Width	9.3

(mm)

Customer Service

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