



128K x 36 SSRAM
SYNCHRONOUS ZBL SRAM
FLOW-THRU OUTPUT

FEATURES

- High frequency and 100% bus utilization
- Fast cycle times: 11ns & 12ns
- Single +3.3V $\pm 5\%$ power supply (V_{DD})
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W\ (READ/WRITE) control pin
- CKE\ pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE\
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 8Mb, and 16Mb ZBL SRAM
- Automatic power-down

OPTIONS

- Timing (Access/Cycle/MHz)
 - 8.5ns/11ns/90 MHz
 - 9ns/12ns/83 MHz
- Packages
 - 100-pin TQFP
- Operating Temperature Ranges
 - Military (-55°C to +125°C)
 - Industrial (-40°C to +85°C)

MARKING

- 11
- 12
- DQ No. 1001
- XT
- IT

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. Zero Bus Latency SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

ASI's 4Mb ZBL SRAMs integrate a 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles for READ to WRITE, or WRITE to READ, transitions. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE\), two additional chip enables for easy depth expansion (CE2, CE2\), cycle start input (ADV/LD\), synchronous clock enable (CKE\), byte write enables (BWA\, BWB\, BWC\, and BWD\)) and read/write (R/W\).

Asynchronous inputs include the output enable (OE\), which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE\.

WRITE cycles can be from one to four bytes wide as controlled by the write control inputs. All READ, WRITE and DESELECT cycles are initiated by the ADV/LD\ input. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV/LD\). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the flow-through ZBL SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITES need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWA\ controls DQa pins; BWB\ controls DQb pins; BWC\ controls DQc pins; and BWD\ controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD\ is LOW. Parity/ECC bits are available on this device.

Austin's 4Mb ZBL SRAMs operate from a +3.3V V_{DD} power supply, and all inputs and outputs are LVTTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

For more products and information
please visit our web site at
www.austinsemiconductor.com



PIN DESCRIPTIONS (continued)

| TQFP PINS | SYMBOL | TYPE | DESCRIPTION |
|--|------------------------------------|--------------|---|
| 64 | ZZ | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. |
| 89 | CLK | Input | Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 98, 92 | CE \setminus , CE2 \setminus | Input | Synchronous Chip Enable: These active LOW inputs are used to enable the device and are sampled only when a new external address is loaded (ADV/LD \setminus LOW). CE2 \setminus can be used for memory depth expansion. |
| 97 | CE2 | Input | Synchronous Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD \setminus LOW). This input can be used for memory depth expansion. |
| 86 | OE \setminus (G \setminus) | Input | Output Enable: This active LOW, asynchronous inputs enables the data I/O output drivers. G \setminus is the JEDEC-standard term for OE \setminus . |
| 85 | ADV/LD \setminus | Input | Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD \setminus is HIGH, R/W is ignored. A LOW on ADV/LD \setminus clocks a new address at the CLK rising edge. |
| 31 | MODE (LBO \setminus) | Input | Mode: This inputs selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO \setminus is the JEDEC-standard term for MODE. |
| (a) 51, 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79, 80 (c) 1, 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29, 30 | DQa DQb DQc DQd | Input/Output | SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge CLK. |
| 15, 16, 41, 65, 91 | V _{DD} | Supply | Power Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 5, 10, 14, 17, 21, 26 40, 55, 60, 66, 67, 71 76, 90 | V _{SS} | Ground | Ground: GND |
| 4, 11, 20, 27, 54, 61 70, 77 | V _{DDQ} | Supply | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 38, 39, 42, 43, 83, 84 64 | NC | ---- | No Connect: These pins can be left floating or connected to GND to minimize thermal impedance. |
| 38, 39, 42, 43 | DNU | ---- | Do Not Use: These signals may with be unconnected or wired to GND to minimize thermal impedance. |
| 83, 84 | NF | ---- | No Function: These pins are internally connected to the die and will have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. Pins 83 and 84 are reserved for address expansion. |



INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|-----------------------------|------------------------------|-----------------------------|------------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X00 | X...X11 | X...X10 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X10 | X...X01 | X...X00 |

LINEAR BURST ADDRESS TABLE (MODE = LOW)

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|-----------------------------|------------------------------|-----------------------------|------------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X10 | X...X11 | X...X00 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X00 | X...X01 | X...X10 |

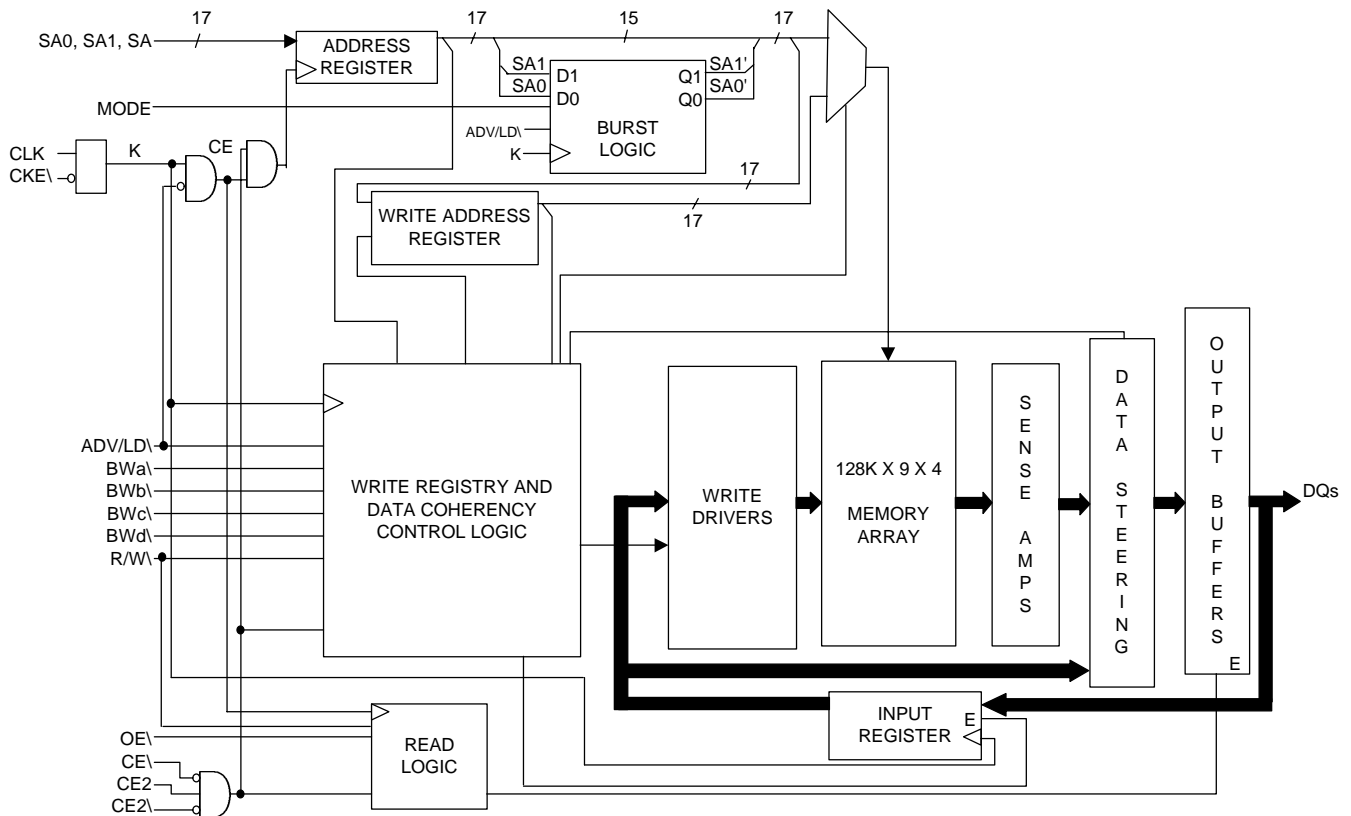
PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS*

| FUNCTION | R/W\ | BWa\ | BWb\ | BWc\ | BWd\ |
|--|------|------|------|------|------|
| READ | H | X | X | X | X |
| Write Abort/NOP | L | H | H | H | H |
| Write Byte a (DQa, DQP _a) ² | L | L | H | H | H |
| Write Byte b (DQb, DQP _b) ² | L | H | L | H | H |
| Write Byte c (DQc, DQP _c) ² | L | H | H | L | H |
| Write Byte d (DQd, DQP _d) ² | L | H | H | H | L |
| Write all bytes | L | L | L | L | L |

* **NOTE:** Using R/W\ and byte write(s), any one or more bytes may be written.



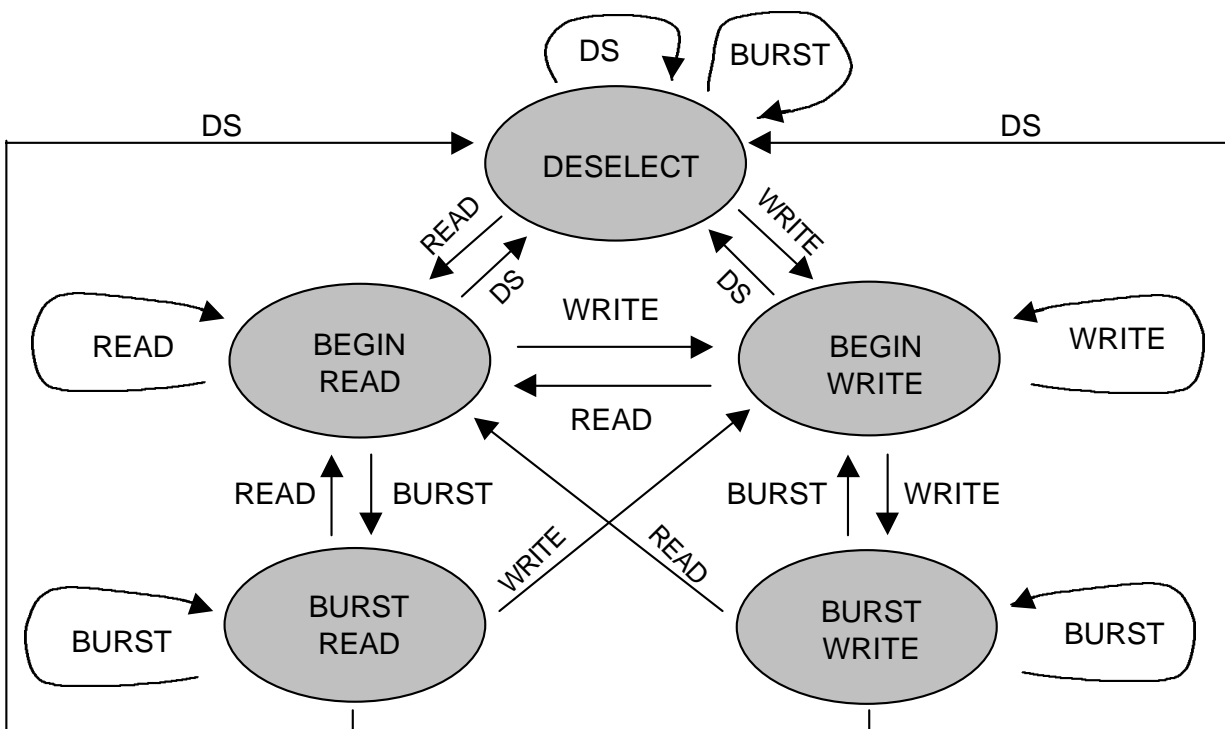
FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.



STATE DIAGRAM FOR ZBL SRAM



KEY:

| COMMAND | ACTION |
|---------|--|
| DS | DESELECT |
| READ | New READ |
| WRITE | New WRITE |
| BURST | BURST READ, BURST WRITE or CONTINUE DESELECT |

- NOTE:**
1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE\ HIGH only blocks the clock (CLK) input and does not change the state of the device.
 2. States change on the rising edge of the clock (CLK).



TRUTH TABLE (5-10)

| OPERATION | ADDRESS USED | CE\ | CE2\ | CE2 | ZZ | ADV/LD\ | R/W\ | BWx | OE\ | CKE\ | CLK | DQ | NOTES |
|----------------------------------|--------------|-----|------|-----|----|---------|------|-----|-----|------|-----|--------|-------------|
| DESELECT CYCLE | None | H | X | X | L | L | X | X | X | L | L→H | High-Z | |
| DESELECT CYCLE | None | X | H | X | L | L | X | X | X | L | L→H | High-Z | |
| DESELECT CYCLE | None | X | X | L | L | L | X | X | X | L | L→H | High-Z | |
| CONTINUE DESELECT CYCLE | None | X | X | X | L | H | X | X | X | L | L→H | High-Z | 1 |
| READ CYCLE (Begin Burst) | External | L | L | H | L | L | H | X | L | L | L→H | Q | |
| READ CYCLE (Continue Burst) | Next | X | X | X | L | H | X | X | L | L | L→H | Q | 1, 11 |
| NOP/DUMMY READ (Begin Burst) | External | L | L | H | L | L | H | X | H | L | L→H | High-Z | 2 |
| DUMMY READ (Continue Burst) | Next | X | X | X | L | H | X | X | H | L | L→H | High-Z | 1, 2, 11 |
| WRITE CYCLE (Begin Burst) | External | L | L | H | L | L | L | L | X | L | L→H | D | 3 |
| WRITE CYCLE (Continue Burst) | Next | X | X | X | L | H | X | L | X | L | L→H | D | 1, 3, 11 |
| NOP/WRITE ABORT (Begin Burst) | None | L | L | H | L | L | L | H | X | L | L→H | High-Z | 2, 3 |
| WRITE ABORT (Continue Burst) | Next | X | X | X | L | H | X | H | X | L | L→H | High-Z | 1, 2, 3, 11 |
| IGNORE CLOCK EDGE (Stall) | Current | X | X | X | L | X | X | X | X | H | L→H | --- | 4 |
| SNOOZE MODE | None | X | X | X | H | X | X | X | X | X | X | High-Z | |

NOTE:

1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is first executed.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE\ may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. OE\ may be used when the bus turn-on and turn-off times do not meet an applications requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWA\, BWb\, BWc\, BWd\) are HIGH. BWx = L means all byte write signals are LOW.
6. BWA\ enables WRITES to Byte "a" (DQa pins); BWb\ enables WRITES to Byte "b" (DQb pins); BWc\ enables WRITES to Byte "c" (DQc pins); BWd\ enables WRITES to Byte "d" (DQd pins).
7. All inputs except OE\ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE\ HIGH.
9. This device contains circuitry that will ensure that the outputs will be in the High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST cycle.
11. The address counter is incremented for all CONTINUE BURST cycles.



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS}.....-0.5V to +4.6V
 Voltage on V_{DD}Q Supply Relative to V_{SS}.....-0.5V to V_{DD}
 V_{IN}.....-0.5V to V_{DD}Q+0.5V
 Storage Temperature (Plastics)-55°C to +150°C
 Short Circuit Output Current100mA
 Max. Junction Temperature*.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 **Junction Temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(-55°C ≤ T_A ≤ +125°C; V_{DD}, V_{DD}Q = +3.3V ±0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|---|-------------------|-------|-----------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.0 | V _{DD} + 0.3 | V | 1, 2 |
| Input High (Logic 1) Voltage | DQ Pins | V _{IH} | 2.0 | V _{DD} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.3 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | I _{LI} | -1.0 | 1.0 | μA | 3 |
| Output Leakage Current | Output(s) Disabled, 0V ≤ V _{IN} ≤ V _{DD} | I _{LO} | -1.0 | 1.0 | μA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | --- | V | 1, 4 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | --- | 0.4 | V | 1, 4 |
| Supply Voltage | | V _{DD} | 3.135 | 3.465 | V | 1 |
| Isolated Output Buffer Supply | | V _{DD} Q | 3.135 | V _{DD} | V | 1, 5 |

CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-------------------------------|--|-----------------|-----|-----|-------|-------|
| Control Input Capacitance | T _A = 25°C; f = 1 MHz V _{DD} = 3.3V | C _I | 3 | 4 | pF | 6 |
| Input/Output Capacitance (DQ) | | C _O | 4 | 5 | pF | 6 |
| Address Capacitance | | C _A | 3 | 3.5 | pF | 6 |
| Clock Capacitance | | C _{CK} | 3 | 3.5 | pF | 6 |

NOTE:

- All voltages referenced to V_{SS} (GND).
- Overshoot: V_{IH} ≤ +4.6V for t ≤ t_{KHKH} / 2 for I ≤ 20mA.
 Undershoot: V_{IL} ≤ -0.7V for t ≤ t_{KHKH} / 2 for I ≤ 20mA.
 Power-up: V_{IH} ≤ +3.465V and V_{DD} ≤ 3.135V for t ≤ 200ms.
- MODE pin has an internal pull-up, and input leakage = ± 10μA.
- The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
- V_{DD}Q should never exceed V_{DD}. V_{DD} and V_{DD}Q should be externally wired together to the same power supply.
- This parameter is sampled.



I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(-55°C ≤ T_A ≤ +125°C; V_{DD}, V_{DD}Q = +3.3V ±0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYM | MAX | | UNITS | NOTES |
|---------------------------------|--|-------------------|-----|-----|-------|-------|
| | | | -11 | -12 | | |
| Power Supply Current: Operating | Device selected; All inputs ≤ V _{IL} or ≥ V _{IH} ; Cycle time ≥ t _{KC} (MIN) V _{DD} = MAX; Outputs open | I _{DD} | 275 | 250 | mA | 1, 2 |
| Power Supply Current: Idle | Device selected; V _{DD} = MAX; CKE\ ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} -0.2; Cycle time ≥ t _{KC} (MIN) | I _{DD1} | 22 | 20 | mA | 1, 2 |
| CMOS Standby | Device selected; V _{DD} = MAX; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} -0.2; All inputs static; CLK frequency = 0 | I _{SB2} | 10 | 10 | mA | 2 |
| TTL Standby | Device selected; V _{DD} = MAX; All inputs ≤ V _{IL} or ≥ V _{IH} ; All inputs static; CLK frequency = 0 | I _{SB3} | 25 | 25 | mA | 2 |
| Clock Running | Device selected; V _{DD} = MAX; ADV/LD\ ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ t _{KC} (MIN) | I _{SB4} | 65 | 60 | mA | 2 |
| Snooze Mode | ZZ ≥ V _{IH} | I _{SB2Z} | 10 | 10 | mA | 2 |

THERMAL RESISTANCE

| DESCRIPTION | CONDITIONS | SYM | TYP | UNITS | NOTES |
|--|---|-----------------|-----|-------|-------|
| Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | θ _{JA} | 46 | °C/W | 3 |
| Thermal Resistance (Junction to Top of Case) | | θ _{JC} | 2.8 | °C/W | 3 |

NOTE:

- I_{DD} is specified with no output current and increases with faster cycle times. I_{DD}Q increases with faster cycle times and greater output loading.
- “Device deselected” means device is in a deselected cycle as defined in the truth table. “Device selected” means device is active (not in deselected mode).
- This parameter is sampled.



AC ELECTRICAL CHARACTERISTICS 6, 8, 9

($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$; $V_{DD}, V_{DDQ} = +3.3\text{V} \pm 0.165\text{V}$)

| DESCRIPTION | SYM | -11 | | -12 | | UNITS | NOTES |
|---------------------------|-------------|-----|-----|-----|-----|-------|------------|
| | | MIN | MAX | MIN | MAX | | |
| CLOCK | | | | | | | |
| Clock cycle time | t_{KHKH} | 11 | | 12 | | ns | |
| Clock frequency | t_{KF} | | 90 | | 83 | MHz | |
| Clock HIGH time | t_{KHKL} | 3.0 | | 3.0 | | ns | 1 |
| Clock LOW time | t_{KLKH} | 3.0 | | 3.0 | | ns | 1 |
| OUTPUT TIMES | | | | | | | |
| Clock to output valid | t_{KHQV} | | 8.5 | | 9.0 | ns | |
| Clock to output invalid | t_{KHQX} | 3.0 | | 3.0 | | ns | 2 |
| Clock to output in Low-Z | t_{KHQX1} | 3.0 | | 3.0 | | ns | 2, 3, 4, 5 |
| Clock to output in High-Z | t_{KHQZ} | | 5.0 | | 5.0 | ns | 2, 3, 4, 5 |
| OE\ to output valid | t_{GLQV} | | 5.0 | | 5.0 | ns | 6 |
| OE\ to output in Low-Z | t_{GLQX} | 0 | | 0 | | ns | 2, 3, 4, 5 |
| OE\ to output in High-Z | t_{GHQZ} | | 5.0 | | 5.0 | ns | 2, 3, 4, 5 |
| SETUP TIMES | | | | | | | |
| Address | t_{AVKH} | 2.2 | | 2.5 | | ns | 7 |
| Clock enable (CKE\) | t_{EVKH} | 2.2 | | 2.5 | | ns | 7 |
| Control signals | t_{CVKH} | 2.2 | | 2.5 | | ns | 7 |
| Data-in | t_{DVKH} | 2.2 | | 2.5 | | ns | 7 |
| HOLD TIMES | | | | | | | |
| Address | t_{KHAX} | 0.5 | | 0.5 | | ns | 7 |
| Clock enable (CKE\) | t_{KHEX} | 0.5 | | 0.5 | | ns | 7 |
| Control signals | t_{KHXC} | 0.5 | | 0.5 | | ns | 7 |
| Data-in | t_{KHDX} | 0.5 | | 0.5 | | ns | 7 |

NOTE:

1. Measured as HIGH above V_{IH} and LOW below V_{IL} .
2. Contact ASI for more information on these parameters.
3. This parameter is sampled.
4. This parameter is measured with the output loading shown in Figure 2.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage.
6. OE\ can be considered a "Don't Care" during WRITES; however, controlling OE\ can help fine-tune a system for ZBL timing.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD\ is LOW to remain enabled.
8. Test conditions as specified with the output loading shown in Figure 1, unless otherwise noted.
9. A WRITE cycle is defined by R/W\ LOW having been registered into the device at ADV/LD\ LOW. A READ cycle is defined by R/W\ HIGH with ADV/LD\ LOW. Both cases must meet setup and hold times.



AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input pulse levels | Vss to 3.3V |
| Input slew rate | 1 ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

OUTPUT LOADS

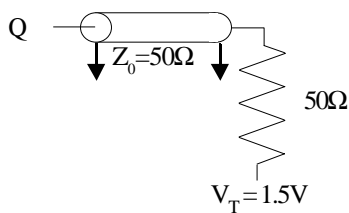


Fig. 1 OUTPUT LOAD EQUIVALENT

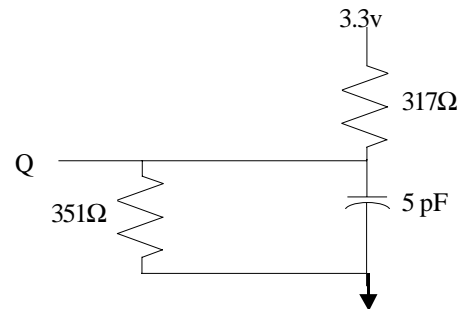


Fig. 2 OUTPUT LOAD EQUIVALENT

LOAD DERATING CURVES

The ASI 128K x 36 ZBL SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.



SNOOZE MODE

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to I_{SB2Z} . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

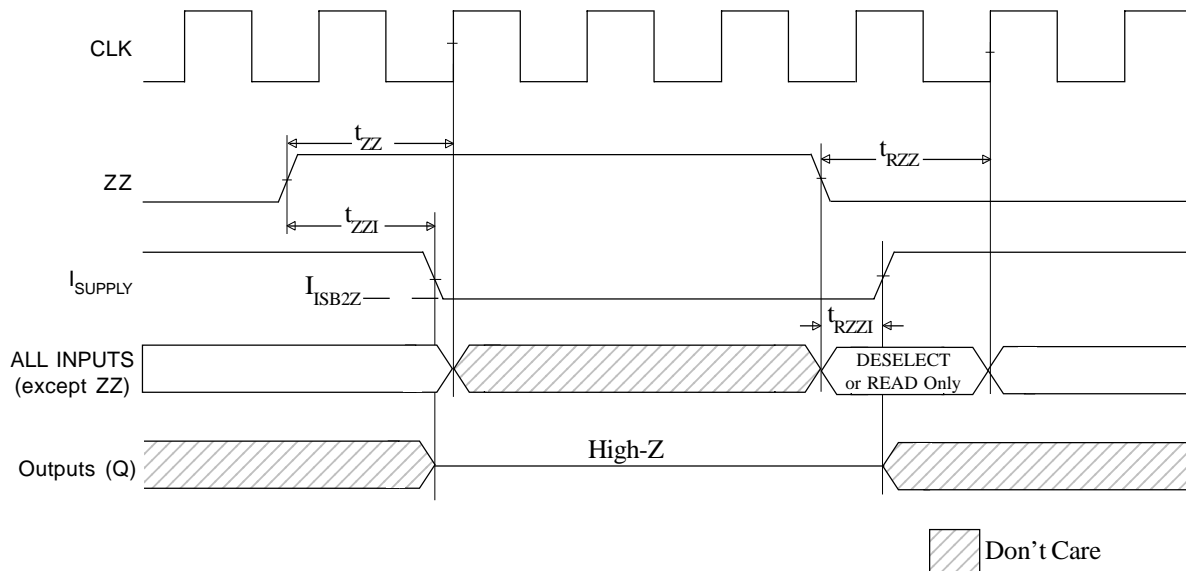
The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin

becomes a logic HIGH, I_{SB2Z} is guaranteed after the time t_{ZZI} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during t_{RZZ} , only a DESELECT or READ cycle should be given.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

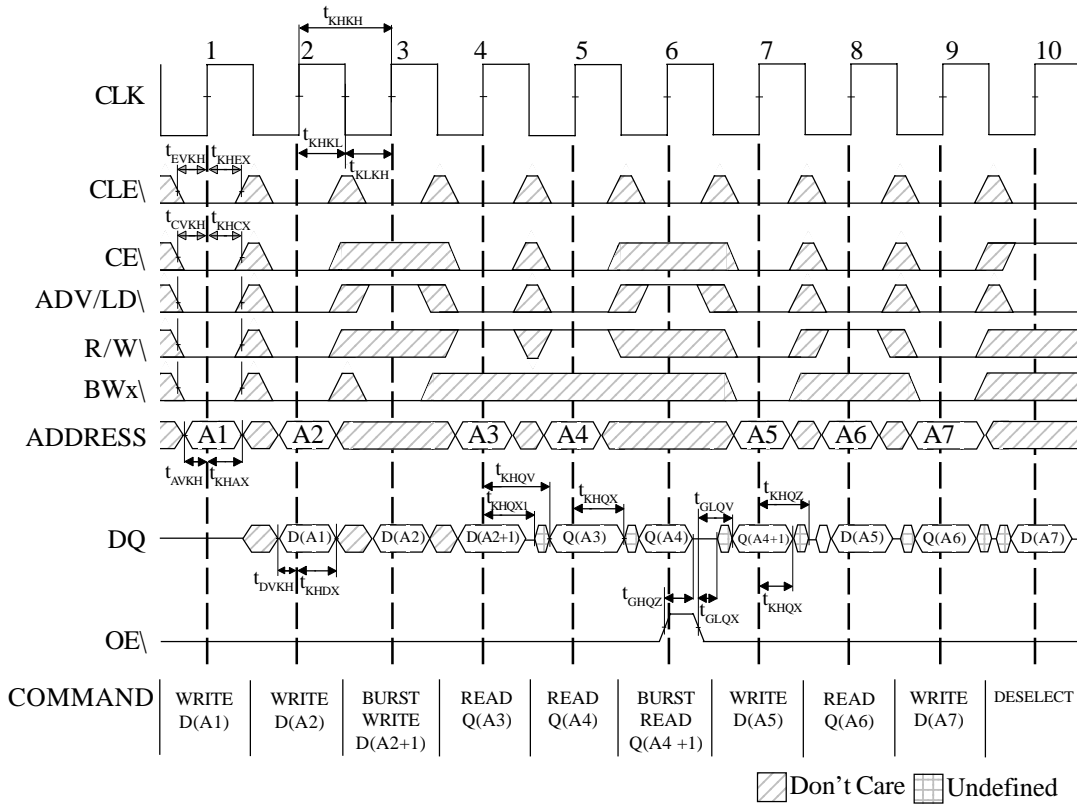
| DESCRIPTION | CONDITIONS | SYM | MIN | MAX | UNITS | NOTES |
|------------------------------------|------------------|------------|-----|------------|-------|-------|
| Current during SNOOZE MODE | $ZZ \geq V_{IH}$ | I_{SB2Z} | | 10 | mA | |
| ZZ active to input ignored | | t_{ZZ} | 0 | t_{KHKH} | ns | 1 |
| ZZ inactive to input sampled | | t_{RZZ} | 0 | t_{KHKH} | ns | 1 |
| ZZ active to snooze current | | t_{ZZI} | | t_{KHKH} | ns | 1 |
| ZZ inactive to exit snooze current | | t_{RZZI} | 0 | | ns | 1 |

SNOOZE MODE WAVEFORM





READ/WRITE TIMING



READ/WRITE TIMING PARAMETERS

| SYMBOL | -11 | | -12 | |
|--------------------|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| t _{KHKH} | 11 | | 12 | |
| t _{KF} | | 90 | | 83 |
| t _{KHKL} | 3.0 | | 3.0 | |
| t _{KLKH} | 3.0 | | 3.0 | |
| t _{KHQV} | | 8.5 | | 9.0 |
| t _{KHQX} | 3.0 | | 3.0 | |
| t _{KHQX1} | 3.0 | | 3.0 | |
| t _{KHQZ} | | 5.0 | | 5.0 |
| t _{GLQV} | | 5.0 | | 5.0 |
| t _{GLQX} | 0 | | 0 | |

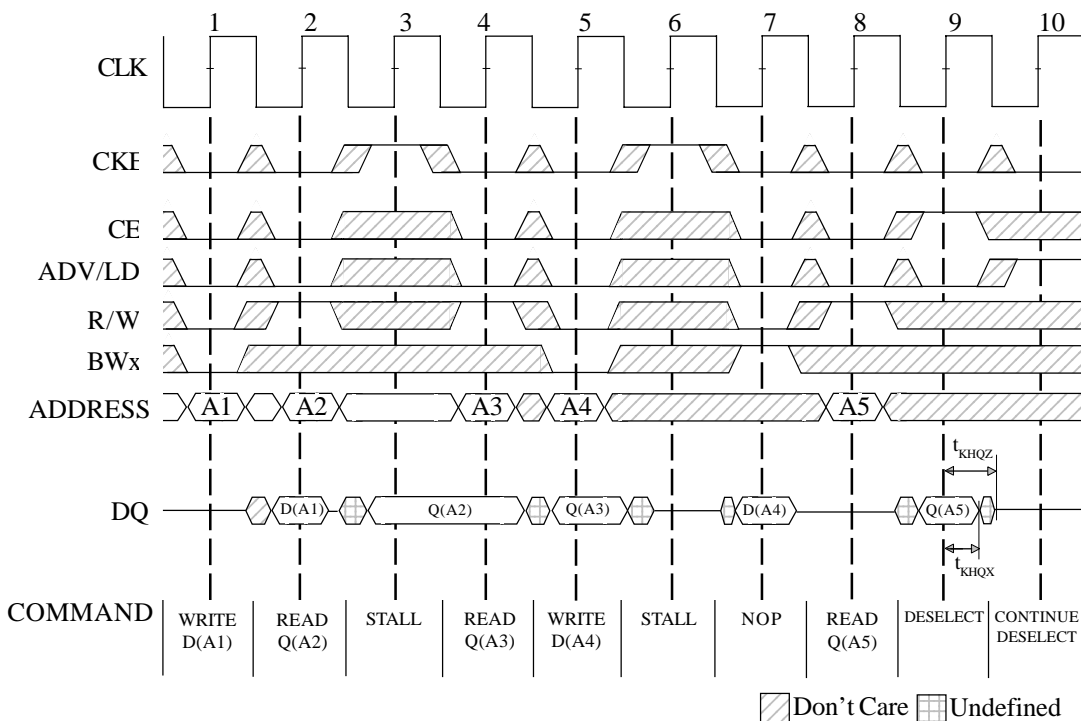
| SYMBOL | -11 | | -12 | |
|-------------------|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| t _{GHQZ} | | 5.0 | | 5.0 |
| t _{AVKH} | 2.2 | | 2.5 | |
| t _{EVKH} | 2.2 | | 2.5 | |
| t _{CVKH} | 2.2 | | 2.5 | |
| t _{DVKH} | 2.2 | | 2.5 | |
| t _{KHAX} | 0.5 | | 0.5 | |
| t _{KHEX} | 0.5 | | 0.5 | |
| t _{KHCX} | 0.5 | | 0.5 | |
| t _{GLDX} | 0.5 | | 0.5 | |

NOTE:

- For this waveform, ZZ is tied LOW.
- Burst sequence order is determined by MODE (0=linear, 1=interleaved). BURST operations are optional.
- CE\ represents three signals. When CE\ = 0, it represents CE\ = 0, CE2\ = 0, CE2 = 1.
- Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.



NOP, STALL AND DESELECT CYCLES



NOP, STALL AND DESELECT TIMING PARAMETERS

| SYMBOL | -11 | | -12 | |
|------------|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| t_{KHQX} | 3.0 | | 3.0 | |
| t_{KHQZ} | | 5.0 | | 5.0 |

NOTE:

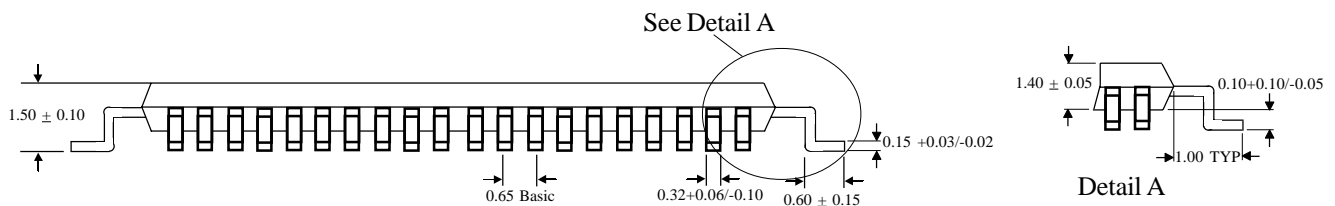
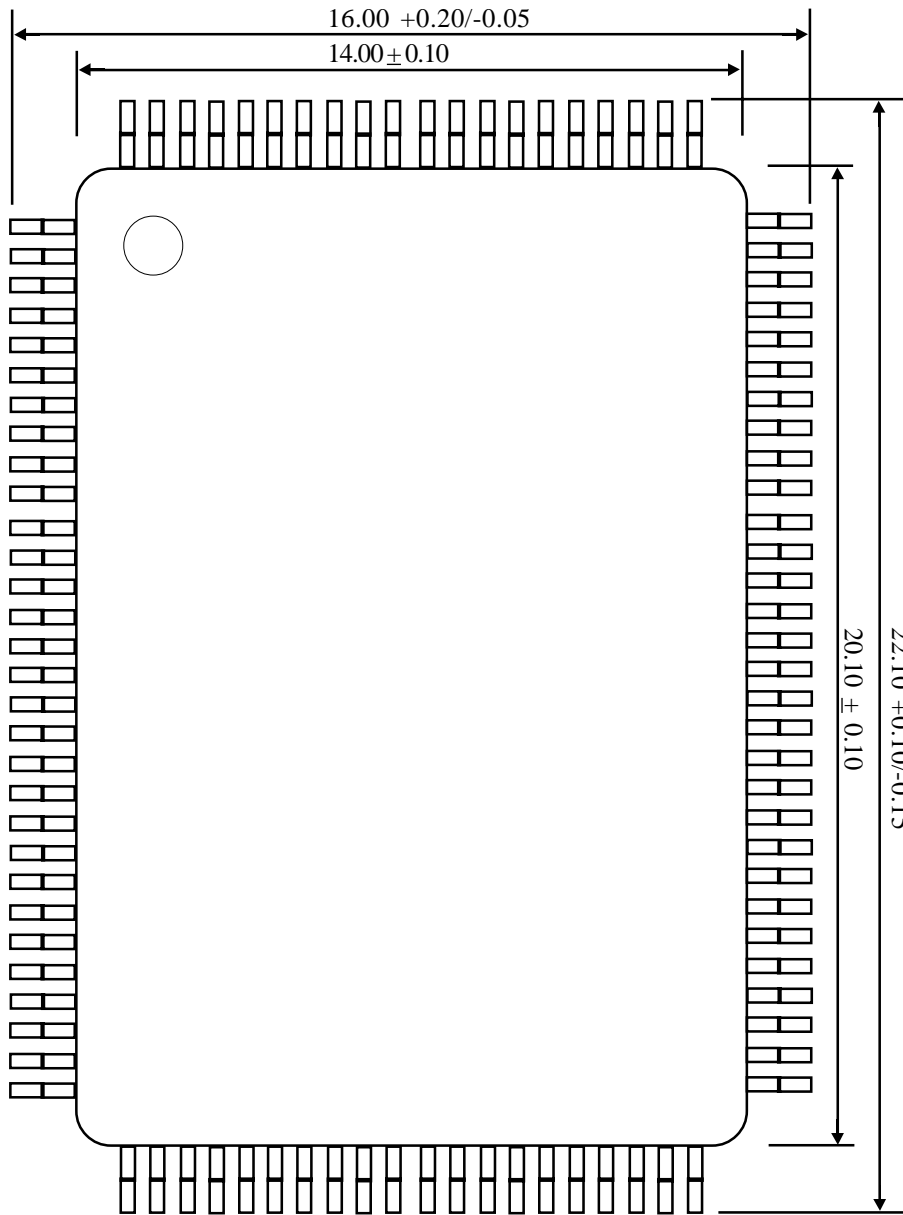
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE\ being used to create a "pause". A WRITE is not performed during this cycle.
2. For this waveform, ZZ and OE\ are tied LOW.
3. CE\ represents three signals. When CE\ = 0, it represents CE\ = 0, CE2\ = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.



Austin Semiconductor, Inc.

SRAM
AS5SS128K36

ASI Case # 1001 (Package Designator DQ)



NOTE: All dimensions in Millimeters.



ORDERING INFORMATION

EXAMPLE: AS5SS128K36DQ-11/IT

| Device Number | Package Type | Speed ns | Process |
|---------------|--------------|----------|---------|
| AS5SS128K36 | DQ | -11 | /* |
| AS5SS128K36 | DQ | -12 | /* |

*AVAILABLE PROCESSES

IT = Industrial Temperature Range

-40°C to +85°C

XT = Extended Temperature Range

-55°C to +125°C