



13 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs

Features

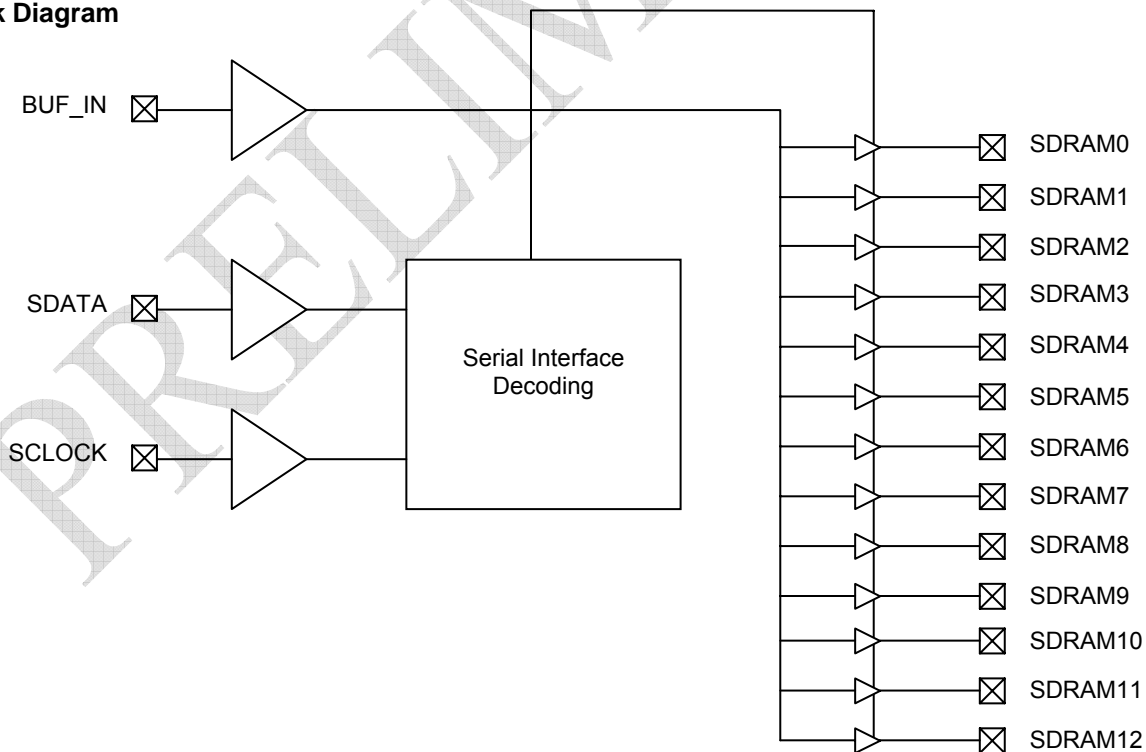
- One input to 13 Output Buffer/Driver
- Supports up to three SDRAM DIMMs
- One additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 133MHz operation
- Multiple V<sub>DD</sub> and V<sub>SS</sub> pins for noise reduction
- Low EMI outputs
- 28 pin SOIC (300-mil) Package
- 3.3V operation

Functional Description

The ASM2I2313ANZ is a 3.3V buffer designed to distribute high-speed clocks in desktop PC applications. The part has 13 outputs, 12 of which can be used to drive up to three SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133MHz, thus making it compatible with Pentium® II processors. The ASM2I2313ANZ can be used in conjunction with the clock synthesizer for a complete Pentium II motherboard solution. The ASM2I2313ANZ also includes a serial interface, which can enable or disable each output clock. On power-up, all output clocks are enabled.

\*Pentium is a registered trademark of Intel Corporation.

Block Diagram

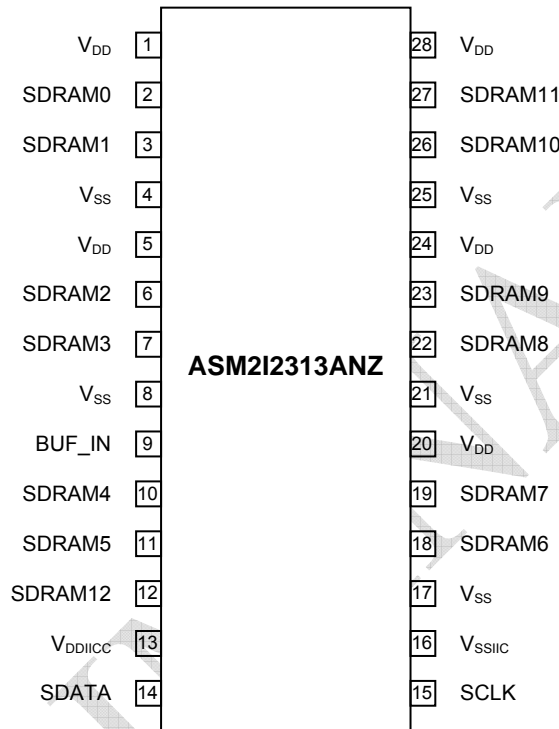




rev 0.4

Pin Configuration

28 Pin SOIC Package -- Top View



Pin Description

Pins	Name	Type	Description
1, 5, 20, 24, 28	VDD	P	3.3V Digital Voltage supply
4, 8, 17, 21, 25	VSS	P	Ground
13	VDDIIC	P	3.3V Serial Interface voltage supply
16	VSSIIC	P	Ground for serial interface
9	BUF_IN	I	Input clock .5V Tolerant
14	SDATA	I/O	Serial data input, internal pull-up to VDD .5V Tolerant
15	SCLK	I	Serial clock input, internal pull-up to VDD .5V Tolerant
2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	SDRAM [0-12]	O	SDRAM Clock Outputs



rev 0.4

**Serial Configuration Map**

- The Serial bits will be read by the clock driver in the following order:
  - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved bits should be programmed to "0" or "1".
- Serial interface address for the ASM2I2313ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 0: SDRAM Active/Inactive Register**  
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	11	SDRAM5 (Active/Inactive)
Bit 6	10	SDRAM4 (Active/Inactive)
Bit 5	--	Reserved
Bit 4	--	Reserved
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

**Byte 1: SDRAM Active/Inactive Register**  
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM11 (Active/Inactive)
Bit 6	26	SDRAM10 (Active/Inactive)
Bit 5	23	SDRAM9 (Active/Inactive)
Bit 4	22	SDRAM8 (Active/Inactive)
Bit 3	--	Reserved
Bit 2	--	Reserved
Bit 1	19	SDRAM7 (Active/Inactive)
Bit 0	18	SDRAM6 (Active/Inactive)

**Byte 2: SDRAM Active/Inactive Register**  
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	--	Reserved
Bit 6	12	SDRAM12 (Active/Inactive)
Bit 5	--	Reserved
Bit 4	--	Reserved
Bit 3	--	Reserved
Bit 2	--	Reserved
Bit 1	--	Reserved
Bit 0	--	Reserved

Note 1 : When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

**IIC Byte Flow**

Byte	Description
1	IIC Address
2	Command (dummy value, ignored)
3	Byte Count (dummy value, ignored)
4	IIC Data Byte 0
5	IIC Data Byte 1
6	IIC Data Byte 2



rev 0.4

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
$V_{DD}$	Supply Voltage to Ground Potential	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Except BUF_IN)	-0.5 to $V_{DD} + 0.5$	V
$V_{BUF\ IN}$	DC Input Voltage (BUF_IN)	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_J$	Junction Temperature	150	°C
$T_{DV}$	Static Discharge Voltage (As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions<sup>1</sup>

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	3.135	3.465	V
$T_A$	Operating Temperature (Ambient Temperature)	0	70	°C
$C_L$	Load Capacitance	20	30	pF
$C_{IN}$	Input Capacitance	-	7	pF
$t_{PU}$	Power-up time for all $V_{DD}$ 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	mS

Note: 1. Electrical parameters are guaranteed under the operating conditions specified.



rev 0.4

## Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input LOW Voltage	Except serial interface pins	-		0.8	V
$V_{ILIC}$	Input LOW Voltage	For serial interface pins only	-		0.7	V
$V_{IH}$	Input HIGH Voltage		2.0		-	V
$V_{OL}$	Output LOW Voltage <sup>1</sup>	$I_{OL} = 25 \text{ mA}$	-		0.4	V
$V_{OH}$	Output HIGH Voltage <sup>1</sup>	$I_{OH} = -36 \text{ mA}$	2.4		-	V
$I_{CC}$	Quiescent Supply Current	$V_{DD} = 3.465\text{V}$ , $V_i = V_{DD}$ or GND, $I_o = 0$		50	100	$\mu\text{A}$
$I_{OZ}$	High Impedance Output Current	$V_{DD} = 3.465\text{V}$ , $V_i = V_{DD}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Off-State Current (for SCL, SDATA)	$V_{DD} = 0\text{V}$ , $V_i = 0\text{V}$ or $5.5\text{V}$			50	$\mu\text{A}$
$\Delta I_{CC}$	Change in Supply Current	$V_{DD} = 3.135\text{V}$ to $3.465\text{V}$ One Input at $V_{DD}-0.6$ , All other Inputs at $V_{DD}$ or GND			500	$\mu\text{A}$
$I_i$	Input Leakage	$V_{DD} = 3.465\text{V}$ or GND (Applicable to all Input Pins)	-5		+5	$\mu\text{A}$
$I_{DD}$	Supply Current <sup>1</sup>	Unloaded outputs, 133MHz			266	mA
$I_{DD}$	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 133MHz			360	mA
$I_{DD}$	Supply Current <sup>1</sup>	Unloaded outputs, 100MHz	-		200	mA
$I_{DD}$	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 100MHz	-		290	mA
$I_{DD}$	Supply Current <sup>1</sup>	Unloaded outputs, 66.67MHz	-		150	mA
$I_{DD}$	Supply Current <sup>1</sup>	Loaded outputs, 30pF, 66.67MHz	-		185	mA
$I_{DDS}$	Supply Current	BUF_IN= $V_{DD}$ or $V_{SS}$ All other inputs at $V_{DD}$	-		500	$\mu\text{A}$

Note: 1. Parameter is guaranteed by design and characterization. Not 100% tested in production.



rev 0.4

Switching Characteristics<sup>1</sup>

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
$F_{in}$	Maximum Operating Frequency		-	-	133	MHz
$t_D$	Duty cycle <sup>2,3</sup> = $t_2 \div t_1$	Measured at 1.5V	45.0	50.0	55.0	%
$t_3$	Rising Edge Rate <sup>3</sup>	Measured between 0.4V and 2.4V	1	2	4	V/nS
$t_4$	Falling Edge Rate <sup>3</sup>	Measured between 2.4V and 0.4V	1	2	4	V/nS
$t_5$	Output to Output Skew <sup>3</sup>	All outputs equally loaded		150	225	pS
$t_6$	SDRAM Buffer LH Prop. Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	2.7	3.5	nS
$t_7$	SDRAM Buffer HL Prop. Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	2.7	3.5	nS
$t_{PLZ}, t_{PHZ}$	SDRAM Buffer Enable Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	3	5	nS
$t_{PZL}, t_{PZH}$	SDRAM Buffer Disable Delay <sup>3</sup>	Input edge greater than 1 V/nS	1	3	5	nS
$t_r$	Rise Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	$C_L = 10pF$	6			nS
		$C_L = 400pF$			250	
$t_f$	Fall Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	$C_L = 10pF$	20			nS
		$C_L = 400pF$			250	

Note: 1. All parameters specified with loaded outputs.  
 2. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/nS  
 3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Test Circuit for SDRAM Enable and Disable Times

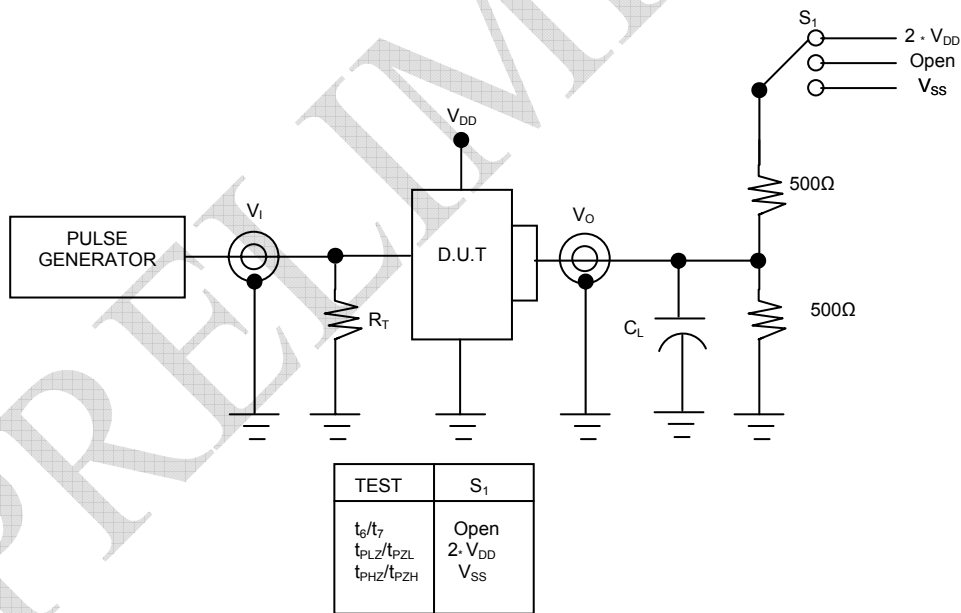


Figure 1. Load circuit for Switching times



rev 0.4

SDRAM Enable and Disable Times

$V_M = 1.5V$

$V_X = V_{OL} + 0.3V$

$V_Y = V_{OH} - 0.3V$

$V_{OH}$  and  $V_{OL}$  are the typical Output Voltage drop that occur with the output load

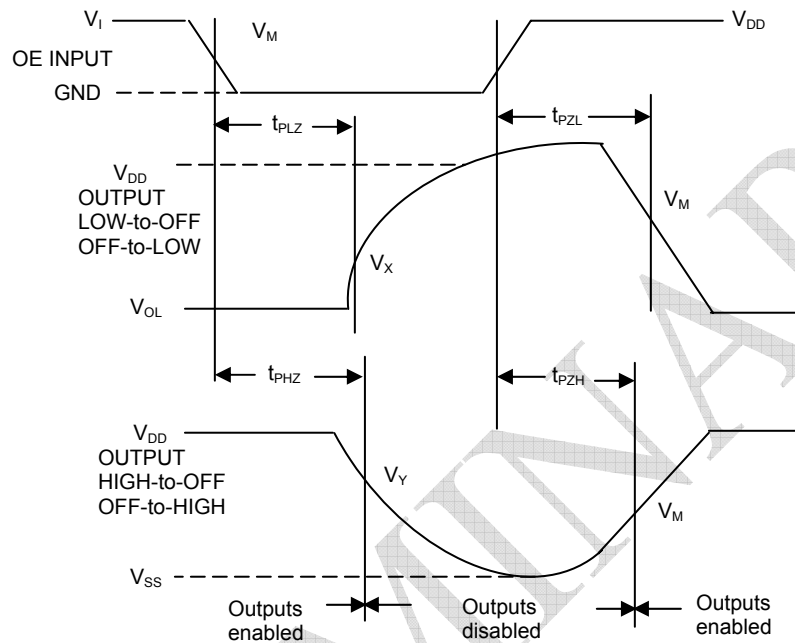


Figure 2. 3-State Enable and Disable times

Test Circuit for IIC Rise and Fall Times

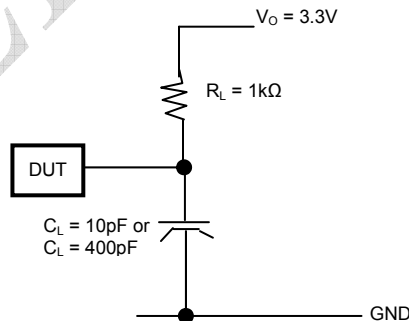


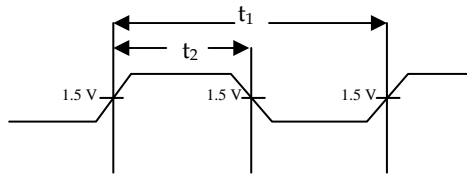
Figure 3. Test Circuit for IIC



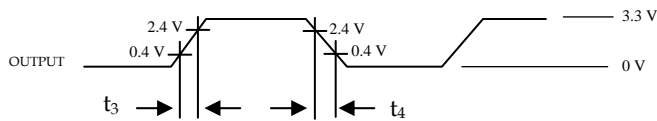
rev 0.4

### Switching Waveforms

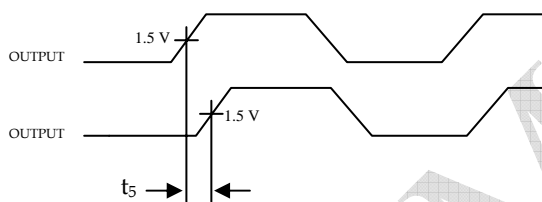
#### Duty Cycle Timing



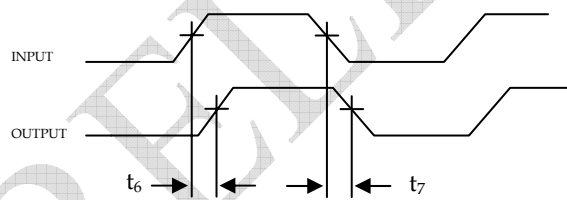
#### All Outputs Rise/Fall Time



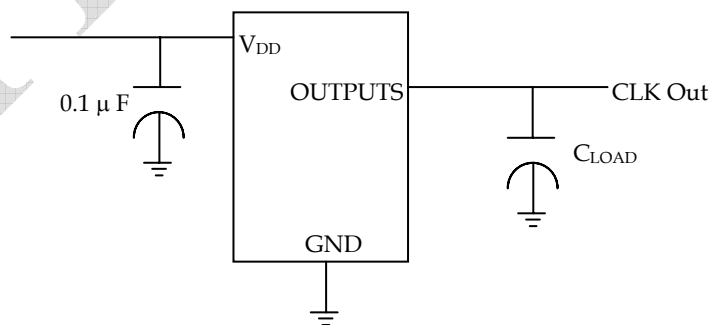
#### Output - Output Skew



#### SDRAM Buffer LH and HL Propagation Delay



#### Test Circuit





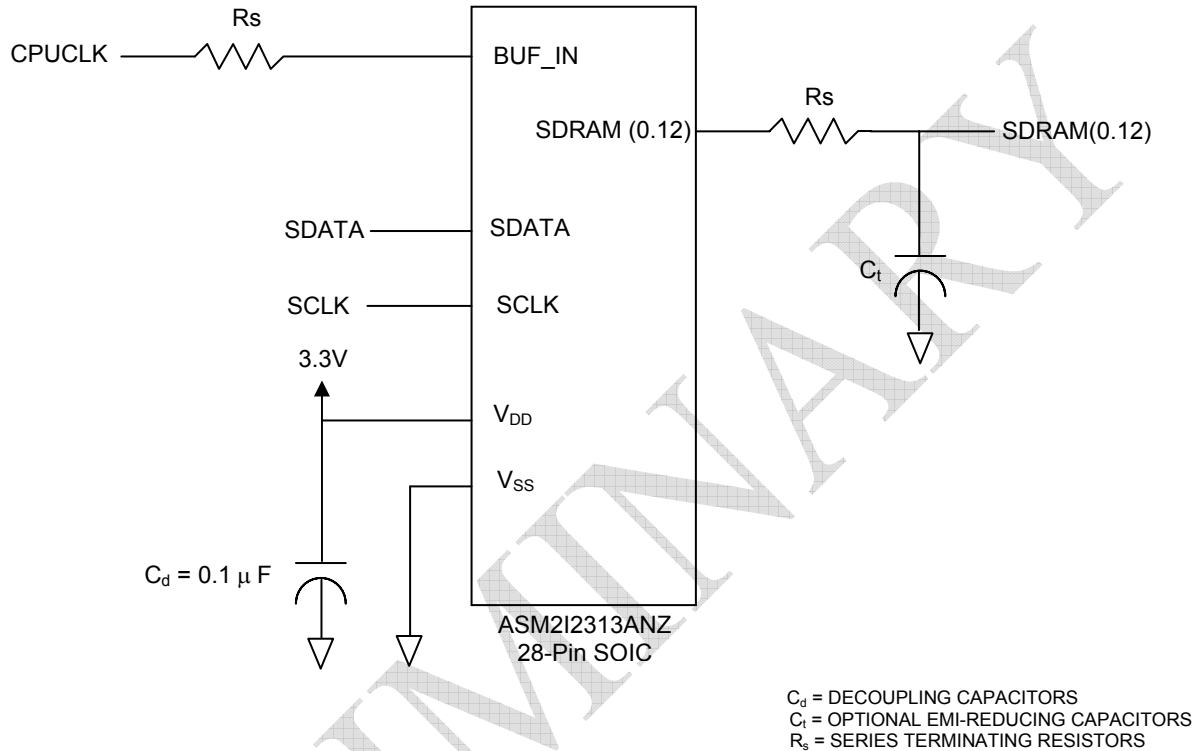


## rev 0.4

## Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.

## Application Circuit



## Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1  $\mu$ F. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the buffer (typically 25 $\Omega$ ), and  $R_{series}$  is the series terminating resistor.
 
$$R_{series} > R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7pF to 22pF.
- A Ferrite Bead may be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50 $\Omega$  impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a 10 $\mu$ F–22 $\mu$ F tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.



**IIC Serial Interface Information**

The information in this section assumes familiarity with IIC programming.

**How to program ASM2I2313ANZ through IIC:**

- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- ASM2I2313ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- ASM2I2313ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count
- ASM2I2313ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0
- ASM2I2313ANZ device will acknowledge Byte 0
- Master (host) sends the Byte 1
- ASM2I2313ANZ device will acknowledge Byte 1
- Master (host) sends the Byte 2
- ASM2I2313ANZ device will acknowledge Byte 2
- Master (host) sends a Stop bit.

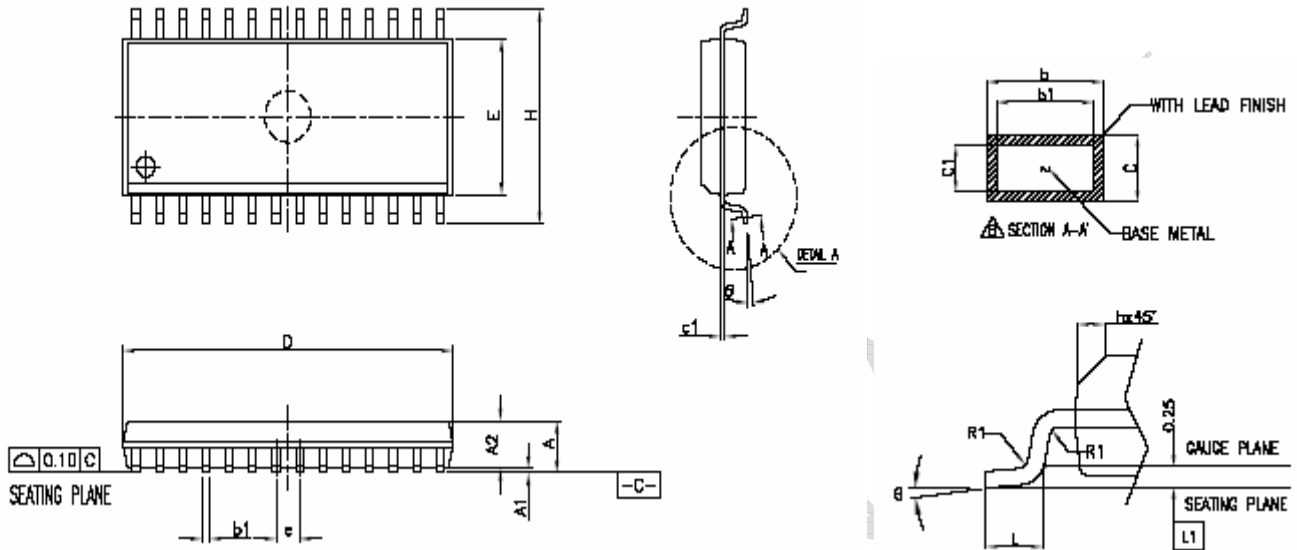
Controller (Host)	ASM2I2313ANZ (slave/receiver)
Start Bit	
Slave Address D3(H)	
	ACK
Command Byte	
	ACK
Byte count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Stop Bit	



rev 0.4

Package Information

28L SOIC Package(300 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.088	0.094	2.25	2.40
D	0.697	0.712	17.70	18.10
h	0.010	0.029	0.25	0.75
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
R1	0.003	....	0.08	.....
b	0.013	0.022	0.33	0.56
b1	0.013	0.020	0.33	0.51
c	0.009	0.015	0.23	0.38
c1	0.009	0.013	0.23	0.33
L	0.016	0.050	0.40	1.27
e	0.050 BSC		1.27 BSC	
θ	0°	8°	0°	8°



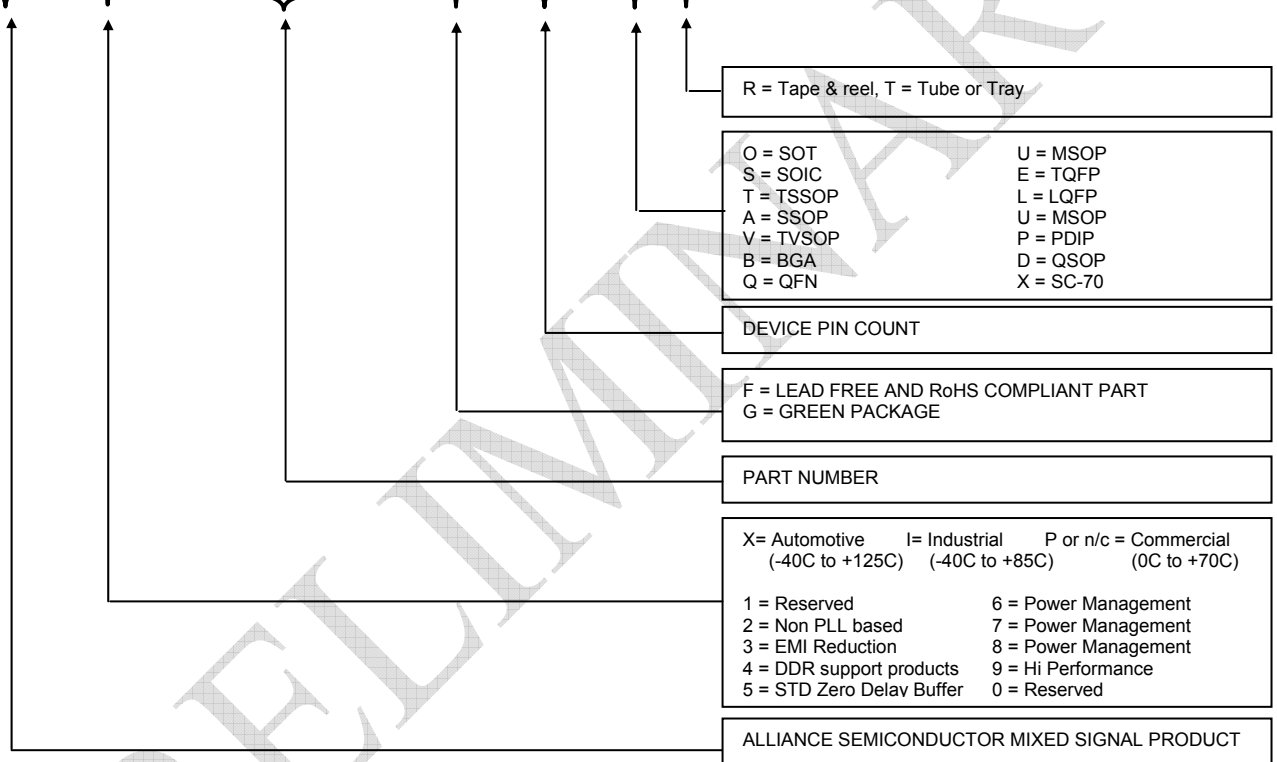
rev 0.4

Ordering Information

Ordering Code	Marking	Package Type	Operating Range
ASM2I2313ANZ-28-ST	2I2313ANZ	28 Pin SOIC, Tube	Industrial
ASM2I2313ANZ-28-SR	2I2313ANZ	28 Pin SOIC, Tape and Reel	Industrial
ASM2I2313AGNZ-28-ST	2I2313AGNZ	28 Pin SOIC, Tube, Green	Industrial
ASM2I2313AGNZ-28-SR	2I2313AGNZ	28 Pin SOIC, Tape and Reel, Green	Industrial

Device Ordering Information

A S M 2 I 2 3 1 3 A N Z G - 2 8 - S R



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



Alliance Semiconductor Corporation  
2575, Augustine Drive,  
Santa Clara, CA 95054  
Tel# 408-855-4900  
Fax: 408-855-4999  
www.alsc.com

Copyright © Alliance Semiconductor  
All Rights Reserved  
Part Number: ASM22313ANZ  
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

© Copyright 2004 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.