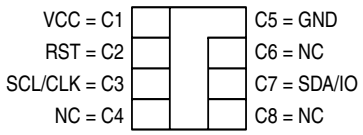
Features

- **One of a Family of Devices with User Memories from 1-Kbit to 1-Mbit**
- **16-Kbit EEPROM User Memory**
  - **Sixteen 128 x 8 (1-Kbit) Zones**
  - **Self-timed Write Cycle (5 ms)**
  - **Single Byte or 16-byte Page Write Mode**
  - **Programmable Access Rights for Each Zone**
- **2-Kbit Configuration Zone**
  - **37-byte OTP Area for User-defined Codes**
  - **160-byte Area for User-defined Keys and Passwords**
- **Low Voltage Operation: 2.7V to 5.5V**
- **Dual Protocol**
  - **ISO 7816-3 Asynchronous T = 0 Protocol**
  - **Synchronous Two-wire Protocol**
- **High Security Features**
  - **64-bit Patented Dynamic Symetric Mutual Authentication Protocol (**under exclusive patent license from **ELVA**)
  - **Encrypted Checksum**
  - **Stream Encryption**
  - **Four Key Sets for Authentication and Encryption**
  - **Eight Sets of Two 24-bit Passwords**
  - **Anti-tearing Function**
  - **Voltage and Frequency Monitor**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 10 years**
  - **ESD Protection: 4,000V min**
- **ISO-compliant Bond Pad Locations and Package Options**

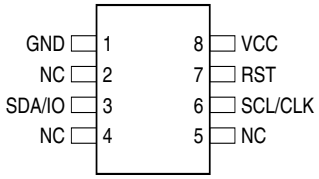
Table 1. Pin Configuration

Pad	Description	ISO Module Contact	Standard Package Pin
VCC	Supply Voltage	C1	8
GND	Ground	C5	1
SCL/CLK	Serial Clock Input	C3	6
SDA/IO	Serial Data Input/Output	C7	3
RST	Reset Input	C2	7

Card Module Contact



8-lead SOIC, PDIP or LAP



8 x 128 x 16 CryptoMemory™

AT88SC1616C

Summary

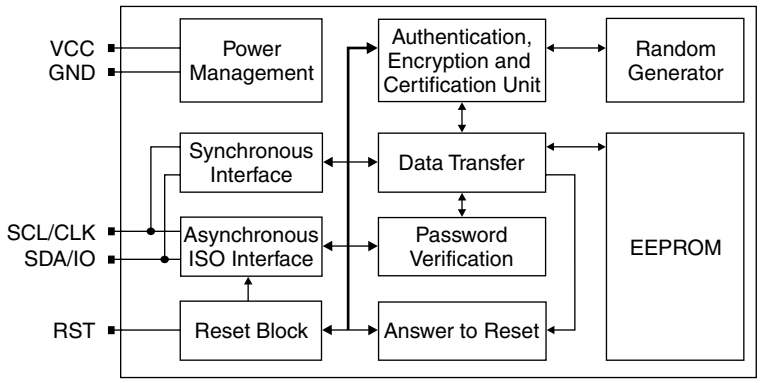
Rev. 2030AS–09/01

Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Description

The AT88SC1616C member of the CryptoMemory family is a high performance secure memory providing 16 Kbits of user memory with advanced security and cryptographic features built in. The user memory is divided into 16 zones, each of which may be individually set with different security access rights or combined together to provide space for 1 to 16 data files. The AT88SC1616C provides high security, low cost and ease of implentation for smart card applications without the need for a microprocessor operating system. The embedded cryptographic engine provides for a dynamic, symmetric-mutual authentication between the device and host as well as performing stream encryption for all data and passwords exchanged between the device and host. Up to four unique key sets may be used for these operations. The AT88SC1616C offers the ability to communicate with virtually any smart card reader using the asynchronous T = 0 protocol defined in ISO 7816-3. For closed systems or applications using the device on a circuit board. The AT88SC1616C will also communicate using a synchronous two-wire protocol at clock speeds up to 2 MHz. In this communication mode, up to 15 devices may be connected and individually addressed on the same serial data bus. The two-wire protocol may also be used for high speed personalization of the device in card form.

Figure 1. Block Diagram



Pin Descriptions

Supply Voltage (V_{CC}) The V_{CC} input is a 2.7V to 5.5V positive voltage supplied by the host.

Clock (SCL/CLK) In the asynchronous T = 0 protocol, the SCL/CLK input is used to provide the device with a carrier frequency *f*. The nominal length of one bit emitted on I/O is defined as an "elementary time unit" (ETU) and is equal to 372/*f*.

When the synchronous protocol is used, the SCL/CLK input is used to positive edge clock data into the device and negative edge clock data out of the device.

Serial Data (SDA/IO) The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open drain or open collector devices. An external pull-up resistor should be connected between SDA and V_{CC}. The value of this resistor and the system capacitance loading the SDA bus will determine the rise time of SDA. This rise time will determine the maximum frequency during Read operations. Low value pull-up resistors will allow higher frequency operations while drawing higher average power supply current.

Reset (RST)

The AT88SC1616C provides an ISO 7816-3 compliant asynchronous answer to reset sequence. When the reset sequence is activated, the device will output the data programmed into the 64-bit answer to reset register. An internal pull-up on the RST input pad allows the device to be used in synchronous mode without bonding RST. The AT88SC1616C does not support the synchronous answer to reset sequence.

Device Architecture

User Zones

The EEPROM user memory is divided into 16 zones of 1024 bits each. Multiple zones allow for different types of data or files to be stored in different zones. Access to the user zones is allowed only after security requirements have been met. These security requirements are defined by the user during the personalization of the device in the configuration zone. If the same security requirements are selected for multiple zones, then these zones may effectively be accessed as one larger zone.

Table 2. User Zones

ZONE	$0	$1	$2	$3	$4	$5	$6	$7	
User 0									$000
	128 bytes								–
									–
									$078
User 1									$000
									–
									–
									–
User 14									$078
User 15									$000
	128 bytes								–
									–
									$078

Control Logic

Access to the user zones occurs only through the control logic built into the device. This logic is configurable through access registers, key registers and keys programmed into the configuration zone during device personalization. Also implemented in the control logic is a cryptographic engine for performing the various higher level security functions of the device.

Configuration Zone

The configuration zone consists of 2048 bits of EEPROM memory used for storing passwords, keys, codes and defining security levels to be used for each user zone. Access rights to the configuration zone are defined in the control logic and may not be altered by the user.

Table 3. Configuration Zone

Component	Address
Answer to Reset	$00
Fab Code	
Memory Test Zone	
Card Manufacturers Code	
Lot History Code	
Identification Number	$18
Device Configuration Register	
Access Registers	
Password/Key Registers	
Authentication Attempts Counters	$50
Cryptograms	
Session Encryption Keys	
Secret Seeds	$90
Password Attempts Counters	$B0
Write Passwords	
Read Passwords	
Reserved	$F0

Security Fuses

There are three fuses on the device that must be blown during the device personalization process. Each fuse locks certain portions of the configuration zone as OTP memory. Fuses are designed for the module manufacturer, card manufacturer and card issuer and should be blown in sequence, although all programming of the device and blowing of the fuses may be performed at one final step.

Protocol Selection

The AT88SC1616C is compatible with two different communication protocols: asynchronous T = 0 as defined by ISO 7816-3 or a synchronous two-wire protocol. The power-up sequence determines which of the two protocols will be used.

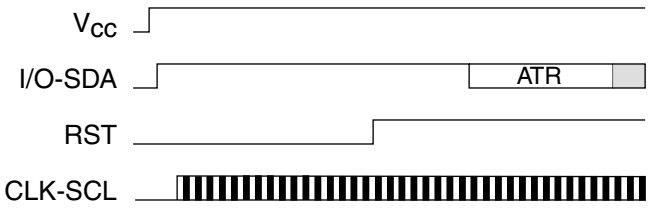
Asynchronous T = 0 Protocol

The power-up sequence complies with ISO 7816-3 for a cold reset.

- V_{CC} goes high with RST, I/O-SDA and CLK-SCL low.
- Set I/O-SDA in receive mode.
- Provide a clock signal to CLK-SCL.
- RST goes high after 400 clock cycles.

The device will respond with a 64-bit ATR code, including hystorical bytes to indicate the memory density within the CryptoMemory family. Once the asynchronous mode has been selected, it is not possible to switch to the synchronous mode without powering off the device.

Figure 2. Asynchronous T = 0 Protocol

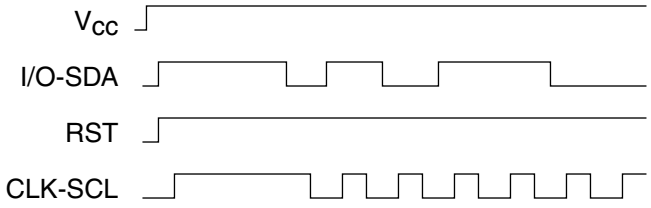


Synchronous Two-wire Protocol

The synchronous mode is the default after powering up V_{CC} due to the internal pull-up on RST.

- Power-up V_{CC}, RST goes high also.
- After stable V_{CC}, CLK-SCL and I/O-SDA may be driven.

Figure 3. Synchronous Two-wire Protocol



Communication Security Modes

Communications between the device and host operate in three basic modes. Standard mode is the default mode for the device after power-up. Authentication mode is activiated by a successful authentication sequence. Encryption mode is activated by a successful encryption activation following a successful authentication.

Table 4. Communication Security Modes[1]

Mode	Configuration Data	User Data	Passwords	Data Integrity Check
Standard	Clear	Clear	Clear	MDC
Authentication	Clear	Clear	Encrypted	MAC
Encryption	Clear	Encrypted	Encrypted	MAC

Note: 1. Configuration data includes viewable areas of the Configuration Zone except the passwords:
MDC: Modification Detection Code.
MAC: Message Authentication Code.

Security Options

Anti-tearing

In the event of a power loss during a write cycle, the integrity of the device's stored data may be recovered. This function is optional: the host may choose to activate the anti-tearing function, depending on application requirements. When anti-tearing is active, write commands take longer to execute, since more write cycles are required to complete them, and data are limited to eight bytes.

Data are written first to a buffer zone in EEPROM instead of the intended destination address, but with the same access conditions. The data are then written in the required location. If this second write cycle is interrupted due to a power loss, the device will automatically recover the data from the system buffer zone at the next power-up.

In two-wire mode, the host is required to perform ACK polling for up to 20 ms after write commands when anti-tearing is active. At power-up, the host is required to perform ACK polling, in some cases for up to 10 ms, in the event that the device needs to carry out the data recovery process.

Write Lock

If a user zone is configured in the write lock mode, the lowest address byte of an 8-byte page constitutes a write access byte for the bytes of that page.

Example: The write lock byte at $080 controls the bytes from $080 to $087.

$080	$081	$082	$083	$084	$085	$086	$087	@
11011001	xxxx xxxx locked	xxxx xxxx locked	xxxx xxxx	xxxx xxxx	xxxx xxxx locked	xxxx xxxx	xxxx xxxx	$80

The write lock byte may also be locked by writing its least significant (rightmost) bit to "0". Moreover, when write lock mode is activated, the write lock byte can only be programmed – that is, bits written to "0" cannot return to "1".

In the write lock configuration, only one byte can be written at a time. Even if several bytes are received, only the first byte will be taken into account by the device.

Password Verification

Passwords may be used to protect read and/or write access of any user zone. When a valid password is presented, it is memorized and active until power is turned off, unless a new password is presented or RST becomes active. There are eight password sets that may be used to protect any user zone. Only one password is active at a time, but write passwords give read access also.

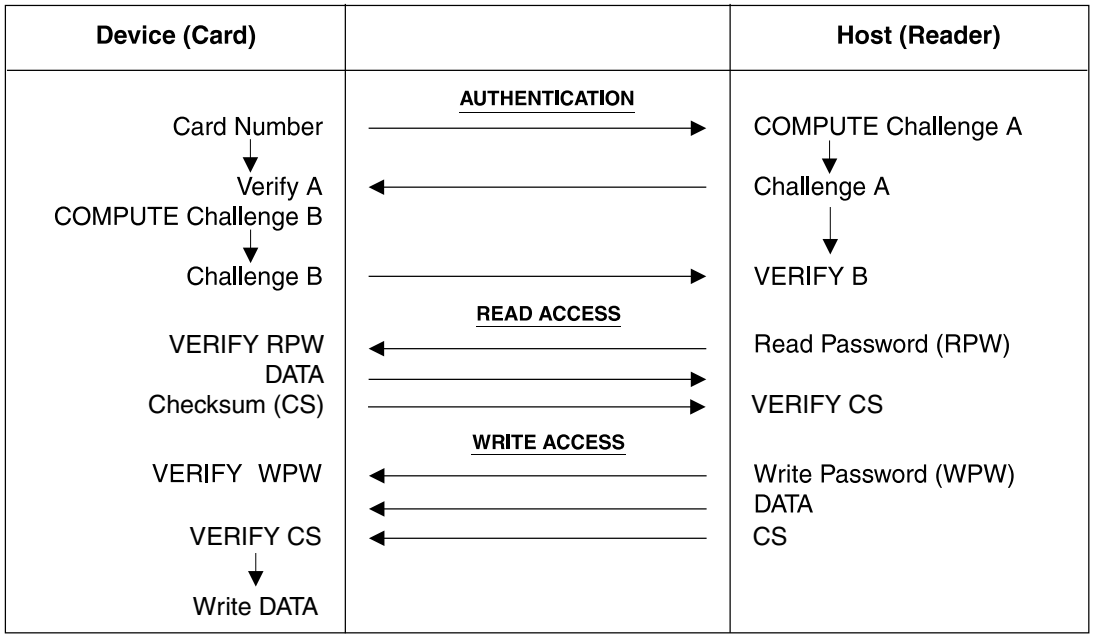
Authentication Protocol

The access to a user zone may be protected by an authentication protocol. Any one of four keys may be selected to use with a user zone.

The authentication success is memorized and active as long as the chip is powered, unless a new authentication is initialized or RST becomes active. If the new authentication request is not validated, the card loses its previous authentication and it should be presented again. Only the last request is memorized.

Note: Password and authentication may be presented at any time and in any order. If the trials limit has been reached (after four consecutive incorrect attempts), the password verification or authentication process will not be taken into account.

Figure 4. Password and Authentication Operations



Checksum

The AT88SC1616C implements a data validity check function in the form of a checksum, which may function in standard, authentication or encryption modes.

In the standard mode, the checksum is implemented as a Modification Detection Code (MDC), in which the host may read a MDC from the device in order to verify that the data sent was received correctly.

In the authentication and encryption modes, the checksum becomes more powerful since it provides a bidirectional data integrity check and data origin authentication capability in the form of a Message Authentication Code (MAC). Only the host/device that carried out a valid authentication is capable of computing a valid MAC. While operating in the authentication or encryption modes, the use of a MAC is required. For an ingoing command, if the device calcu-

lates a MAC different from the MAC transmitted by the host, not only is the command abandoned but the mode is also reset. A new authentication and/or encryption activation will be required to reactivate the MAC.

Encryption

The data exchanged between the device and the host during read, write and verify password commands may be encrypted to ensure data confidentiality.

The issuer may choose to require encryption for a user zone by settings made in the configuration zone. Any one of four keys may be selected for use with a user zone. In this case, activation of the encryption mode is required in order to read/write data in the zone and only encrypted data will be transmitted. Even if not required, the host may elect to activate encryption provided the proper keys are known.

Supervisor Mode

Enabling this feature allows the holder of one specific password to gain full access to all 8 password sets including the ability to change passwords.

Modify Forbidden

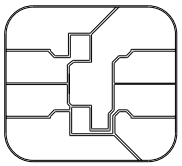
No write access is allowed in a user zone protected with this feature at any time. The user zone must be written during device personalization prior to blowing the security fuses.

Program Only

For a user zone protected by this feature, data within the zone may be changed from a “1” to a “0”, but never from a “0” to a “1”.

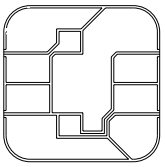
Packaging Information

Ordering Code: 09NT



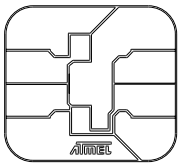
Module Size: **M2**
Dimension*: 12.6 x 11.4 [mm]
Glob Top: Square – 8.8 x 8.8 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 mm

Ordering Code: 09CT



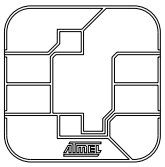
Module Size: **M4**
Dimension*: 12.6 x 12.6 [mm]
Glob Top: Square – 9.0 x 9.0 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 mm

Ordering Code: 09PT



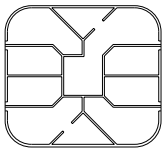
Module Size: **M2**
Dimension*: 12.6 x 11.4 [mm]
Glob Top: Square – 8.8 x 8.8 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 mm

Ordering Code: 09DT



Module Size: **M4**
Dimension*: 12.6 x 12.6 [mm]
Glob Top: Square – 9.0 x 9.0 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 mm

Ordering Code: 09ET

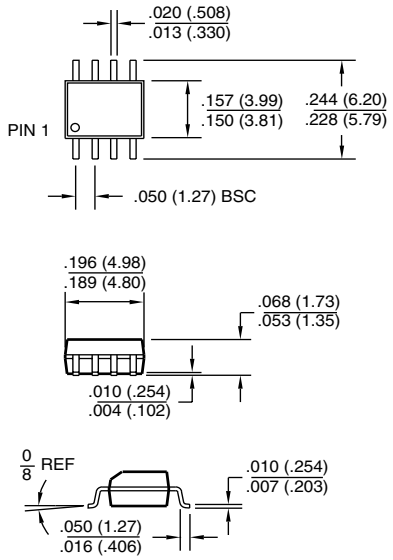


Module Size: **M2**
Dimension*: 12.6 x 11.4 [mm]
Glob Top: Round – ∅ 8.0 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 mm

Note: The module dimensions listed refer to the dimensions of the exposed metal contact area. The actual dimensions of the module after excise or punching from the carrier tape are generally 0.4 mm greater in both directions (i.e., a punched M2 module will yield 13.0 x 11.8 mm).

Ordering Code: 10SC

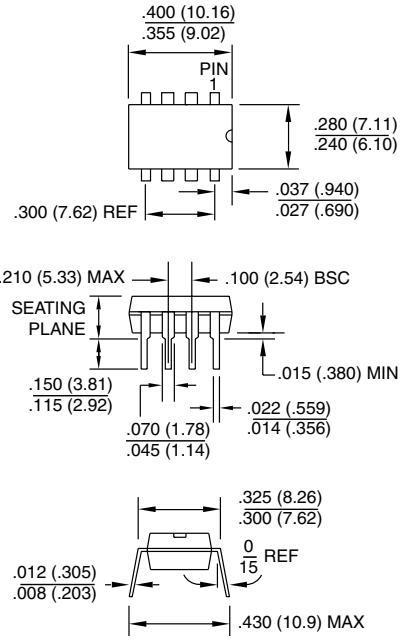
8S1, 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



Packaging Information

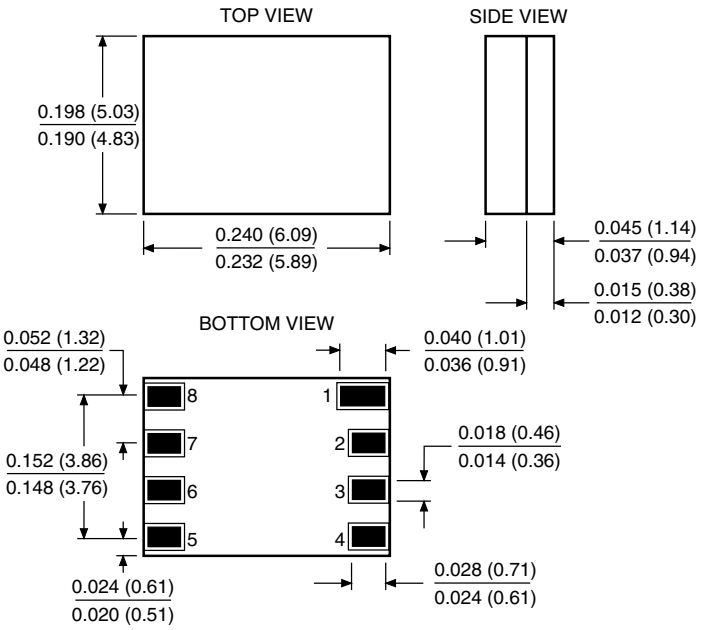
Ordering Code: 10PC

8P3, 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



Ordering Code: 10CC

8C, 8-lead, 0.230" Wide, Leadless Array Package (LAP)
Dimensions in Inches and (Millimeters)



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