Features

- **Incorporates the ARM926EJ-S™ ARM® Thumb® Processor**
  - **DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration**
  - **16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer**
  - **220 MIPS at 200 MHz**
  - **Memory Management Unit**
  - **EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support**
- **Additional Embedded Memories**
  - **One 32 Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed**
  - **One 32 Kbyte Internal SRAM, Single-cycle Access at Maximum Matrix Speed**
- **External Bus Interface (EBI)**
  - **EBI Supports Mobile DDR, SDRAM, Low Power SDRAM, Static Memory, Synchronous CellularRAM, ECC-enabled NAND Flash and CompactFlash™**
- **Metal Programmable (MP) Block**
  - **500,000 Gates/250,000 Gates Metal Programmable Logic (through 5 Metal Layers) for AT91CAP9S500A/AT91CAP9S250A Respectively**
  - **Ten 512 x 36-bit Dual Port RAMs**
  - **Eight 512 x 72-bit Single Port RAMs**
  - **High Connectivity for Up to Three AHB Masters and Four AHB Slaves**
  - **Up to Seven AIC Interrupt Inputs**
  - **Up to Four DMA Hardware Handshake Interfaces**
  - **Delay Lines for Double Data Rate Interface**
  - **UTMI+ Full Connection**
  - **Up to 77 Dedicated I/Os**
- **LCD Controller**
  - **Supports Passive or Active Displays**
  - **Up to 24 Bits per Pixel in TFT Mode, Up to 16 Bits per Pixel in STN Color Mode**
  - **Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Wider Screen Buffers**
- **Image Sensor Interface**
  - **ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate**
  - **12-bit Data Interface for Support of High Sensibility Sensors**
  - **SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format**
- **USB 2.0 Full Speed (12 Mbits per second) OHCI Host Double Port**
  - **Dual On-chip Transceivers**
  - **Integrated FIFOs and Dedicated DMA Channels**
- **USB 2.0 High Speed (480 Mbits per second) Device Port**
  - **On-chip Transceiver, 4 Kbyte Configurable Integrated DPRAM**
  - **Integrated FIFOs and Dedicated DMA Channels**
  - **Integrated UTMI+ Physical Interface**
- **Ethernet MAC 10/100 Base T**
  - **Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)**
  - **28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit**
- **Multi-Layer Bus Matrix**
  - **Twelve 32-bit-layer Matrix, Allowing a Maximum of 38.4 Gbps of On-chip Bus Bandwidth at Maximum 100 MHz System Clock Speed**
  - **Boot Mode Select Option, Remap Command**
- **Fully-featured System Controller, Including**
  - **Reset Controller, Shutdown Controller**

Customizable Microcontroller Processor

AT91CAP9S500A AT91CAP9S250A

Summary

Preliminary

- – **Four 32-bit Battery Backup Registers for a Total of 16 Bytes**
- – **Clock Generator and Power Management Controller**
- – **Advanced Interrupt Controller and Debug Unit**
- – **Periodic Interval Timer, Watchdog Timer and Real-Time Timer**
- **Reset Controller (RSTC)**
  - – **Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control**
- **Shutdown Controller (SHDC)**
  - – **Programmable Shutdown Pin Control and Wake-up Circuitry**
- **Clock Generator (CKGR)**
  - – **32,768 Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock**
  - – **8 to 16 MHz On-chip Oscillator**
  - – **Two PLLs up to 240 MHz**
  - – **One USB 480 MHz PLL**
- **Power Management Controller (PMC)**
  - – **Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities**
  - – **Four Programmable External Clock Signals**
- **Advanced Interrupt Controller (AIC)**
  - – **Individually Maskable, Eight-level Priority, Vectored Interrupt Sources**
  - – **Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected**
- **Debug Unit (DBGU)**
  - – **2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention**
- **Periodic Interval Timer (PIT)**
  - – **20-bit Interval Timer plus 12-bit Interval Counter**
- **Watchdog Timer (WDT)**
  - – **Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock**
- **Real-Time Timer (RTT)**
  - – **32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler**
- **Four 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC and PIOE)**
  - – **128 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os**
  - – **Input Change Interrupt Capability on Each I/O Line**
  - – **Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output**
- **DMA Controller (DMAC)**
  - – **Acts as one Bus Matrix Master**
  - – **Embeds 4 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control**
  - – **Supports Four External DMA Requests and Four Internal DMA Requests from the Metal Programmable Block (MPBlock)**
- **Twenty-two Peripheral DMA Controller Channels (PDC)**
- **One 2.0A and 2.0B Compliant CAN Controller**
  - – **16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter**
- **Two Multimedia Card Interfaces (MCI)**
  - – **SDCard/SDIO and MultiMedia™ Card 3.31 Compliant**
  - – **Automatic Protocol Control and Fast Automatic Data Transfers with PDC**
- **Two Synchronous Serial Controllers (SSC)**
  - – **Independent Clock and Frame Sync Signals for Each Receiver and Transmitter**
  - – **I²S Analog Interface Support, Time Division Multiplex Support**
  - – **High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer**

- **One AC97 Controller (AC97C)**
  - **6-channel Single AC97 Analog Front End Interface, Slot Assigner**
- **Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
  - **Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding**
  - **Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support**
- **Two Master/Slave Serial Peripheral Interface (SPI)**
  - **8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects**
  - **Synchronous Communications at Up to 90 Mbits/sec**
- **One Three-channel 16-bit Timer/Counters (TC)**
  - **Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel**
  - **Double PWM Generation, Capture/Waveform Mode, Up/Down Capability**
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
  - **Master and Slave Mode Support, All Two-wire Atmel EEPROMs Supported**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Required Power Supplies:**
  - **1.08V to 1.32V for VDDCORE and VDDBU**
  - **3.0V to 3.6V for VDDOSC, VDDPLL and VDDIOP0 (Peripheral I/Os)**
  - **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOP1 (Peripheral I/Os) and for VDDIOM (Memory I/Os) and VDDIOMPP/VDDIOMP (MP Block I/Os)**
- **Available in 324- and 400-ball LFBGA RoHS-compliant Packages**

1. Description

The AT91CAP9S500A/AT91CAP9S250A family is based on the integration of an ARM926EJ-S processor with fast ROM and SRAM memories, and a wide range of peripherals. By providing up to 500K gates of metal programmable logic, AT91CAP9S500A/AT91CAP9S250A is the ideal platform for creating custom designs.

The AT91CAP9S500A/AT91CAP9S250A embeds a USB High-speed Device, a 2-port USB OHCI Host, an LCD Controller, a 4-channel DMA Controller, and one Image Sensor Interface. It also integrates several standard peripherals, such as USART, SPI, TWI, Timer Counters, PWM generators, Multimedia Card interface, and one CAN Controller.

The AT91CAP9S500A/AT91CAP9S250A is architectured on a 12-layer matrix, allowing a maximum internal bandwidth of twelve 32-bit buses. It also features one external memory bus (EBI) capable of interfacing with a wide range of memory devices.

The initial release of the AT91CAP9S500A/AT91CAP9S250A is packaged in a 400-ball LFBGA RoHS-compliant package. A future release will also be available in a 324-ball LFBGA RoHS-compliant package.

2. AT91CAP9S500A/AT91CAP9S250A Block Diagram

Figure 2-1.   AT91CAP9S500A/AT91CAP9S250A Block Diagram

3.   Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1.   Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOMPA	MP Block I/O A Lines Power Supply	Power		1.65V to 3.6V
VDDIOMPB	MP Block I/O B Lines Power Supply	Power		1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDUTMII	USB UTMI+ Interface Power Supply	Power		3.0V to 3.6V
VDDUTMIC	USB UTMI+ Core Power Supply	Power		1.08V to 1.32V
VDDUPLL	USB UTMI+ PLL Power Supply	Power		1.08V to 1.32V
VDDANA	ADC Analog Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDUTMII	USB UTMI+ Interface Ground	Ground		
GNDUTMIC	USB UTMI+ Core Ground	Ground		
GNDUPLL	USB UTMI+ PLL Ground	Ground		
GNDANA	ADC Analog Ground	Ground		
GNDBU	Backup Ground	Ground		
GNDTHERMAL	Thermal Ground Ball	Ground		Thermally coupled with package substrate
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Do not tie over VDDBU
WKUP	Wake-Up Input	Input		Accept between 0V and VDDBU

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	No pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor
RTCK	Return Test Clock	Output		
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		Pull-up resistor
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC - PIOD				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD31	Parallel IO Controller D	I/O		Pulled-up input at reset
Direct Memory Access Controller - DMA				
DMARQ0-DMARQ3	DMA Requests	Input		
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS5	Chip Select Lines	Output	Low	
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
DDR/SDRAM Controller				
SDCK	DDR/SDRAM Clock	Output		
SDCKN	DDR Inverted Clock	Output		
DQS0	DDR Data Qualifier Strobe 0	I/O		
DQS1	DDR Data Qualifier Strobe 1	I/O		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Burst CellularRAM Controller				
BCCK	Burst CellularRAM Clock	Output		
BCCRE	Burst CellularRAM Enable	Output		
BCADV	Burst CellularRAM Burst Advance Signal	Output		
BCWE	Burst CellularRAM Write Enable	Output		
BCOE	Burst CellularRAM Output Enable	Output		
BCOWAIT	Burst CellularRAM Output Wait	Input		
Multimedia Card Interface MCI				
MCIx_CK	Multimedia Card Clock	Output		
MCIx_CD	Multimedia Card Command	I/O		
MCIx_D0 - D3	Multimedia Card Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USART				

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
Synchronous Serial Controller - SSC				
TDx	SSCx Transmit Data	Output		
RDx	SSCx Receive Data	Input		
TKx	SSCx Transmit Clock	I/O		
RKx	SSCx Receive Clock	I/O		
TFx	SSCx Transmit Frame Sync	I/O		
RFx	SSCx Receive Frame Sync	I/O		
AC97 Controller - AC97C				
AC97RX	AC97 Receive Signal	Input		
AC97TX	AC97 Transmit Signal	Output		
AC97FS	AC97 Frame Synchronization Signal	Output		
AC97CK	AC97 Clock signal	Input		
Timer/Counter - TC				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
Pulse Width Modulation Controller- PWMC				
PMWx	Pulse Width Modulation Output	Output		
Serial Peripheral Interface - SPI				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1 - SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
CAN Controller				
CANRX	CAN input	Input		
CANTX	CAN output	Output		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
LCD Controller - LCDC				
LCDD0 - LCDD23	LCD Data Bus	Input		
LCDVSYNC	LCD Vertical Synchronization	Output		
LCDHSYNC	LCD Horizontal Synchronization	Output		
LCDDOTCK	LCD Dot Clock	Output		
LCDDEN	LCD Data Enable	Output		
LCDCC	LCD Contrast Control	Output		
Ethernet 10/100 E				
ETXCK/EREFCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	RMII only
USB High Speed Device				
FSDM	USB Full Speed Data -	Analog		
FSDP	USB Full Speed Data +	Analog		
HSDM	USB High Speed Data -	Analog		
HSDP	USB High Speed Data +	Analog		
VBG	Bias Voltage Reference	Analog		
PLLRCU	USB PLL Test Pad	Analog		
OHCI USB Host Port				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data -	Analog		
ADC				
AD0-AD7	Analog Inputs	Analog		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
ADVREF	ADC Voltage Reference	Analog		
ADTRIG	ADC Trigger	Input		
Image Sensor Interface - ISI				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data Clock	Input		
MPBLOCK - MPB				
MPIOA0-MPIOA31	MPBlock I/Os A	I/O		
MPIOB0-MPIOB44	MPBlock I/Os B	I/O		

4. Package and Pinout

The AT91CAP9S500A/AT91CAP9S250A is available in a 400-ball RoHS-compliant BGA package, 17 x 17 mm, 0.8mm ball pitch.

4.1 400-ball BGA Package Outline

Figure 4-1 shows the orientation of the 400-ball BGA Package.

A detailed mechanical description is given in the section "AT91CAP9S500A/AT91CAP9S250A Mechanical Characteristics" of the product datasheet.

Figure 4-1. 400-ball BGA Package Outline (Top View)
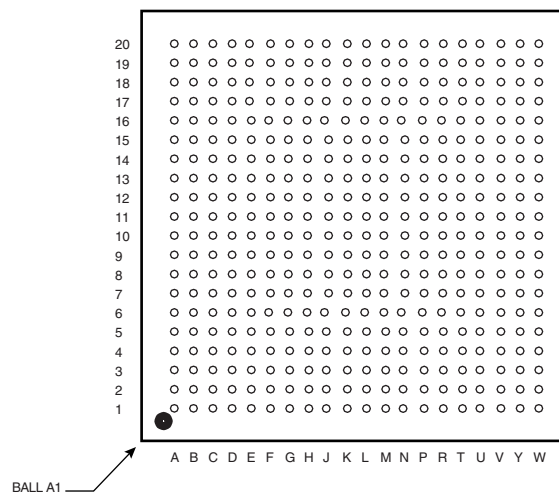
4.2   400-ball BGA Package Pinout

Table 4-1.   AT91CAP9S500A/AT91CAP9S250A Pinout for 400-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PC5	F1	PA3	L1	PA22	T1	PD22
A2	PC3	F2	PA4	L2	PA25	T2	PD23
A3	PC2	F3	PA8	L3	PA29	T3	PD30
A4	PC1	F4	PA5	L4	PA31	T4	VDDCORE
A5	PC0	F5	PA6	L5	PD6	T5	SDDRCS
A6	BMS	F6	VDDIOM	L6	GNDIO	T6	DQS0
A7	NRST	F7	VDDIOP0	L7	GNDCORE	T7	D4
A8	GNDCORE	F8	PC24	L8	PA18	T8	D11
A9	PB18	F9	NC	L9	GNDTHERMAL	T9	D14
A10	PB17	F10	VDDCORE	L10	GNDTHERMAL	T10	SDA10
A11	PB14	F11	GNDIO	L11	GNDTHERMAL	T11	VDDCORE
A12	PB15	F12	PB23	L12	GNDTHERMAL	T12	MPIOA0
A13	GNDANA	F13	PB6	L13	GNDCORE	T13	MPIOA9
A14	PB26	F14	NC	L14	GNDIO	T14	GNDIO
A15	VDDIOP0	F15	NC	L15	VDDCORE	T15	MPIOA25
A16	GNDIO	F16	NC	L16	MPIOB28	T16	MPIOA24
A17	FSDP	F17	GNDPLL	L17	MPIOB32	T17	MPIOA29
A18	FSDM	F18	WKUP0	L18	MPIOB34	T18	MPIOB3
A19	HSDP	F19	SHDW	L19	MPIOB31	T19	MPIOB17
A20	HSDM	F20	PLLRCA	L20	MPIOB29	T20	MPIOB18
B1	PC17	G1	PA7	M1	PA26	U1	PD25
B2	PC16	G2	PA10	M2	PA30	U2	PD31
B3	PC14	G3	PA11	M3	PD11	U3	BCCLK
B4	PC11	G4	PA9	M4	PD12	U4	A0
B5	PC10	G5	PA12	M5	PD13	U5	D0
B6	PC9	G6	PD10	M6	PD15	U6	D1
B7	TDO	G7	GNDIO	M7	GNDCORE	U7	NWR1
B8	TCK	G8	GNDCORE	M8	PA28	U8	DQS1
B9	PB20	G9	VDDIOP0	M9	GNDTHERMAL	U9	A7
B10	PB19	G10	PC8	M10	GNDTHERMAL	U10	A13
B11	PB13	G11	PB25	M11	GNDTHERMAL	U11	A20
B12	ADVREF	G12	PB21	M12	GNDTHERMAL	U12	GNDIO
B13	PB16	G13	PB8	M13	NRD	U13	MPIOA4
B14	PB27	G14	PB0	M14	MPIOB26	U14	MPIOA11
B15	PB24	G15	PB2	M15	GNDIO	U15	MPIOA16
B16	HDMA	G16	NC	M16	MPIOB16	U16	VDDMPIOA
B17	VDDIOP0	G17	VDDPLL	M17	GNDCORE	U17	MPIOA23

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
B18	GNDIO	G18	GNDCORE	M18	MPIOB27	U18	MPIOA28
B19	VDDUTMII	G19	TST	M19	MPIOB25	U19	MPIOB6
B20	GNDUTMII	G20	PLLRCB	M20	MPIOB24	U20	MPIOB9
C1	PC23	H1	PA13	N1	PD7	V1	PD26
C2	PC22	H2	PA14	N2	PD8	V2	RAS
C3	PC21	H3	PD0	N3	PD16	V3	SDCKE
C4	PC20	H4	PA15	N4	PD19	V4	D3
C5	PC18	H5	PD1	N5	PD20	V5	VDDIOM
C6	PC15	H6	VDDIOP1	N6	PD29	V6	D5
C7	PC12	H7	VDDCORE	N7	GNDIO	V7	D9
C8	PC6	H8	GNDIO	N8	VDDIOM	V8	D15
C9	NTRST	H9	GNDIO	N9	NCS1	V9	A11
C10	TDI	H10	PB10	N10	VDDCORE	V10	GNDCORE
C11	VDDANA	H11	PB4	N11	A3	V11	A22
C12	PB12	H12	VDDMPIOB	N12	A6	V12	MPIOA1
C13	PB29	H13	JTAGSEL	N13	VDDCORE	V13	MPIOA6
C14	PB9	H14	GNDCORE	N14	MPIOB11	V14	MPIOA10
C15	PB7	H15	GNDPLL	N15	MPIOB13	V15	MPIOA13
C16	HDPA	H16	NC	N16	MPIOB12	V16	MPIOA17
C17	HDPB	H17	VDDCORE	N17	MPIOB14	V17	MPIOA20
C18	VDDUPLL	H18	MPIOB44	N18	MPIOB15	V18	MPIOA27
C19	VDDUTMIC	H19	XOUT32	N19	MPIOB22	V19	MPIOB5
C20	VBG	H20	XIN32	N20	MPIOB23	V20	VDDMPIOB
D1	PC29	J1	PD3	P1	PD9	W1	SDWE
D2	PC28	J2	PD2	P2	PD14	W2	OWAIT
D3	PC27	J3	PD5	P3	PD18	W3	NANDWE
D4	PC26	J4	PA17	P4	PD27	W4	GNDIO
D5	PC25	J5	PA19	P5	PD28	W5	D6
D6	PC19	J6	VDDIOP0	P6	VDDIOM	W6	A2
D7	NANDOE	J7	PA16	P7	NWR3	W7	A5
D8	PC7	J8	GNDCORE	P8	D8	W8	A14
D9	GNDIO	J9	GNDTHERMAL	P9	D10	W9	A17
D10	TMS	J10	GNDTHERMAL	P10	GNDIO	W10	A19
D11	NC	J11	GNDTHERMAL	P11	A9	W11	NWR0
D12	PB31	J12	GNDTHERMAL	P12	A12	W12	MPIOA2
D13	PB22	J13	GNDIO	P13	NC	W13	MPIOA5
D14	VDDCORE	J14	GNDBU	P14	MPIOB8	W14	MPIOA8
D15	PB3	J15	GNDBU	P15	MPIOB0	W15	MPIOA12

Table 4-1. AT91CAP9S500A/AT91CAP9S250A Pinout for 400-ball BGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
D16	PB1	J16	MPIOB42	P16	MPIOB1	W16	MPIOA15
D17	HDMB	J17	MPIOB39	P17	MPIOB7	W17	MPIOA21
D18	PLLRCU	J18	MPIOB43	P18	MPIOB10	W18	MPIOA22
D19	GNDUTMIC	J19	MPIOB41	P19	MPIOB21	W19	GNDIO
D20	GNDUPLL	J20	GNDIO	P20	VDDMPIOB	W20	VDDCORE
E1	PC30	K1	PD4	R1	PD21	Y1	SDCK
E2	PA2	K2	PA21	R2	PD17	Y2	SDCKN
E3	PA1	K3	PA24	R3	PD24	Y3	A1
E4	PA0	K4	PA27	R4	CAS	Y4	GNDCORE
E5	PC31	K5	PA23	R5	VDDCORE	Y5	A4
E6	GNDIO	K6	GNDIO	R6	D2	Y6	A8
E7	VDDCORE	K7	PA20	R7	D7	Y7	A10
E8	PC13	K8	VDDCORE	R8	VDDIOM	Y8	A15
E9	PC4	K9	GNDTHERMAL	R9	D13	Y9	A18
E10	RTCK	K10	GNDTHERMAL	R10	D12	Y10	A21
E11	VDDIOP0	K11	GNDTHERMAL	R11	VDDIOM	Y11	NCS0
E12	PB30	K12	GNDTHERMAL	R12	A16	Y12	MPIOA3
E13	PB28	K13	GNDCORE	R13	VDDIOM	Y13	MPIOA7
E14	PB11	K14	MPIOB33	R14	NC	Y14	VDDMPIOA
E15	PB5	K15	MPIOB30	R15	NC	Y15	MPIOA14
E16	NC	K16	MPIOB35	R16	NC	Y16	MPIOA18
E17	VDDPLL	K17	MPIOB38	R17	MPIOB2	Y17	MPIOA19
E18	VDDBU	K18	MPIOB40	R18	MPIOB4	Y18	MPIOA26
E19	XIN	K19	MPIOB37	R19	MPIOB19	Y19	MPIOA30
E20	XOUT	K20	MPIOB36	R20	MPIOB20	Y20	MPIOA31

5. Power Considerations

5.1 Power Supplies

The AT91CAP9S500A/AT91CAP9S250A has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage range between1.08V and 1.32V, 1.2V nominal.

- VDDIOM pins: Power the External Bus Interface; voltage ranges between 1.65V and 1.95V (1.8V nominal) or between 3.0V and 3.6V (3.3V nominal).

- VDDIOP0 pins: Power the Peripherals I/O lines and the USB transceivers; voltage range between 3.0V and 3.6V, 3.3V nominal.

- VDDIOP1 pins: Power the Peripherals I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.

- VDDIOMPA pins: Power the MP Block I/O A lines; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDIOMPB pins: Power the dedicated MP Block I/O B lines; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage range between 1.08V and 1.32V, 1.2V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges between 3.0V to 3.6V, 3.3V nominal.
- VDDUTMII pin: Powers the UTMI+ interface; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDUTMIC pin: Powers the UTMI+ core; voltage ranges between 1.08V and 1.32V, 1.2V nominal.
- VDDUPLL pin: Powers the USB PLL cell; voltage ranges between 1.08V and 1.32V, 1.2V nominal.
- VDDANA pin: Powers the ADC cell; voltage ranges between 3.0V and 3.6V, 3.3V nominal.

The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GNDIO are common to VDDIOM, VDDIOP0, VDDIOP1, VDDIOMPA and VDDIOMPB pin power supplies. Separated ground pins are provided for VDDCORE, VDDBU, VDDPLL, VDDUTMII, VDDUTMIC, VDDUPLL and VDDANA. These ground pins are, respectively, GNDBU, GNDOSC, GNDPLL, GNDUTMII, GNDUTMIC, GNDUPLL and GNDANA.

Special GNDTHERMAL ground balls are thermally coupled with package substrate.

5.2 Power Consumption

The AT91CAP9S500A/AT91CAP9S250A consumes about 700 µA (TBC) of static current on VDDCORE at 25°C. This static current may go up to 7 mA (TBC) if the temperature increases to 85°C.

On VDDBU, the current does not exceed 3 µA (TBC) @25°C, but can rise at up to 20 µA (TBC) @85°C.

For dynamic power consumption, the AT91CAP9S500A/AT91CAP9S250A consumes a maximum of 90 mA (TBC) on VDDCORE at typical conditions (1.2V, 25°C, processor running full-performance algorithm).

5.3 Programmable I/O Lines Power Supplies

The power supply pins VDDIOM, VDDMPIOA and VDDMPIOB accept two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The target maximum speed is 100 MHz on the pin DDR/SDR and MPIOA or MPIOB pins loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V. The other signals (control, address and data signals) do not go over 50 MHz.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. Obviously, the device cannot reach its maximum speed if the voltage supplied to the pins is 1.8V only. The user must make sure to program the EBI voltage range before getting the device out of its Slow Clock Mode.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3 "Reset Pins" on page 15.

All the JTAG signals are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells that manage the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 90 kΩ minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines which are managed by the PIO Controllers integrate a programmable pull-up resistor of 90 kΩ minimum. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those multiplexed with the External Bus Interface signals that must be enabled as Peripheral at reset. This is indicated in the column "Reset State" of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The SHDN pin is an output only, which is driven by the Shutdown Controller only at low level. It can be tied high with an external pull-up resistor at VDDBU only.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
    - ARM High-performance 32-bit Instruction Set
    - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
    - Instruction Fetch (F)
    - Instruction Decode (D)
    - Execute (E)
    - Data Memory (M)
    - Register Write (W)
- 16-Kbyte Data Cache, 16-Kbyte Instruction Cache
    - Virtually-addressed 4-way Associative Cache
    - Eight words per line
    - Write-through and Write-back Operation
    - Pseudo-random or Round-robin Replacement
- Write Buffer
    - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
    - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
    - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
    - Access Permission for Sections
    - Access Permission for large pages and small pages can be specified separately for each quarter of the page
    - 16 embedded domains
- Bus Interface Unit (BIU)
    - Arbitrates and Schedules AHB Requests
    - Separate Masters for both instruction and data access providing complete Matrix system flexibility
    - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
    - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 12-layer Matrix, handling requests from 12 masters
- Programmable Arbitration strategy
    - Fixed-priority Arbitration

– Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master

• Burst Management

– Breaking with Slot Cycle Limit Support

– Undefined Burst Length Support

• One Address Decoder provided per Master

– Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap

• Boot Mode Select

– Non-volatile Boot Memory can be internal or external

– Selection is made by BMS pin sampled at reset

• Remap Command

– Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory

– Allows Handling of Dynamic Exception Vectors

7.3 Matrix Masters

The Bus Matrix of the AT91CAP9S500A/AT91CAP9S250A manages twelve Masters and thus each master can perform an access concurrently with the others, assuming that the slave it accesses is available.

Each Master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decoding.

Table 7-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	Peripheral DMA Controller
Master 3	LCD Controller
Master 4	USB High Speed Device Controller
Master 5	Image Sensor Interface
Master 6	DMA Controller
Master 7	Ethernet MAC
Master 8	OHCI USB Host Controller
Master 9	MP Block Master 0
Master 10	MP Block Master 1
Master 11	MP Block Master 2

7.4 Matrix Slaves

The Bus Matrix of the AT91CAP9S500A/AT91CAP9S250A manages ten Slaves. Each Slave has its own arbiter, thus permitting a different arbitration per Slave to be programmed.

The LCD Controller, the DMA Controller, the USB Host and the USB OTG have a user interface mapped as a Slave of the Matrix. They share the same layer, as programming them does not require a high bandwidth.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM 32 Kbytes
Slave 1	MP Block Slave 0 (MP Block Internal Memories)
Slave 2	Internal ROM
	LCD Controller User Interface
	DMA Controller User Interface
	USB High Speed Device Interface
	OHCI USB Host Interface
Slave 3	MP Block Slave 1 (MP Block Internal Memories)
Slave 4	External Bus Interface
Slave 5	DDR Controller Port 2
Slave 6	DDR Controller Port 3
Slave 7	MP Block Slave 2 (MP Block External Chip Selects)
Slave 8	MP Block Slave 3 (MP Block Internal Peripherals)
Slave 9	Internal Peripherals for AT91CAP9

7.5 Master-to-Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown "-" in .

Table 7-3. AT91CAP9S500A/AT91CAP9S250A Masters to Slaves Access

	Master	0	1	2	3	4	5	6	7	8	9	10	11
	Slave	ARM926 Instruction	ARM926 Data	Peripheral DMA Ctrl	LCDCtrl	USB High Speed Device Ctrl	Image Sensor Interface	DMA Ctrl	Ethernet MAC	OHCI USB Host Ctrl	MP Block Master 0	MP Block Master 1	MP Block Master 2
0	Internal SRAM 32 Kbytes	X	X	X	X	X	X	X	X	X	X	X	X
1	MP Block Slave 0	X	X	X	X	X	X	X	X	X	X	X	X
2	Internal ROM	X	X	X	X	X	X	X	X	X	X	X	X
	LCD Controller User Interface	X	X	-	-	-	-	-	-	-	X	X	X
	USB High Speed Device Interface	X	X	-	-	-	-	X	-	-	X	X	X
	OHCI USB Host Interface	X	X	-	-	-	-	-	-	-	X	X	X
3	MPBlock Slave 1	X	X	X	X	X	X	X	X	X	X	X	X
4	External Bus Interface	X	X	X	X	X	X	X	X	X	X	X	X
-													
-	DDR Port 0	X	-	-	-	-	-	-	-	-	-	-	-
5	DDR Port 1	-	X	-	-	-	-	-	-	-	-	-	-
6	DDR Port 2			X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]
	DDR Port 3			X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]
7	MPBlock Slave 2	X	X	X	X	X	X	X	X	X	X	X	X
8	MPBlock Slave 3	X	X	X	X	X	X	X	X	X	X	X	X
9	Internal Peripherals	X	X	X	-	-	-	X	-	-	X	X	X

Note: 1. DDR Port 2 or Port 3 is selectable for each master through the Matrix Remap Control Register.

7.6 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-two Channels
  - Two for each USART
  - Two for the Debug Unit
  - One for the TWI
  - One for the ADC Controller
  - Two for the AC97 Controller
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for the each Multimedia Card Interface

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

- DBGU Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- AC97 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC1 Transmit Channel
- SSC0 Transmit Channel
- DBGU Receive Channel
- TWI Transmit/Receive Channel
- ADC Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- AC97 Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC1 Receive Channel
- SSC0 Receive Channel
- MCI1 Transmit/Receive Channel
- MCI0 Transmit/Receive Channel

7.7 DMA Controller

- Acting as one Matrix Master

- Embeds 4 unidirectional channels with programmable priority
- Address Generation
  - Source / destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
- Channel Buffering
  - 8-word FIFO
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support
- Transfer Initiation
  - Support four External DMA Requests and four Internal DMA request from the MP Block
  - Support for Software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
  - Programmable Interrupt generation on DMA Transfer completion Block Transfer completion, Single/Multiple transaction completion or Error condition

7.8 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91CAP9S500A/AT91CAP9S250A Memory Mapping

Address Memory Space		
0x0000 0000	Internal Memories	256M Bytes
0x0FFF FFFF / 0x1000 0000	EBI Chip Select 0	256M Bytes
0x1FFF FFFF / 0x2000 0000	EBI Chip Select 1/ EBI BCRAMC	256M Bytes
0x2FFF FFFF / 0x3000 0000	EBI Chip Select 2	256M Bytes
0x3FFF FFFF / 0x4000 0000	EBI Chip Select 3/ NANDFlash	256M Bytes
0x4FFF FFFF / 0x5000 0000	EBI Chip Select 4/ Compact Flash Slot 0	256M Bytes
0x5FFF FFFF / 0x6000 0000	EBI Chip Select 5/ Compact Flash Slot 1	256M Bytes
0x6FFF FFFF / 0x7000 0000	EBI DDRSDRC	256M Bytes
0x7FFF FFFF / 0x8000 0000	MPB SLAVE2 Chip Select 0	256M Bytes
0x8FFF FFFF / 0x9000 0000	MPB SLAVE 2 Chip Select 1	256M Bytes
0x9FFF FFFF / 0xA000 0000	MPB SLAVE 2 Chip Select 2	256M Bytes
0xAFFF FFFF / 0xB000 0000	MPB SLAVE 2 Chip Select 3	256M Bytes
0xBFFF FFFF / 0xC000 0000	Undefined (Abort)	768M Bytes
0xEFFF FFFF / 0xF000 0000	Undefined (Abort)	208M Bytes
0xFCFF FFFF / 0xFD00 0000	MPB SLAVE3	16M Bytes
0xFE00 0000	MPB SLAVE3	16M Bytes
0xFF00 0000	Internal Peripherals	16M Bytes
0xFFFF FFFF		

Internal Memory Mapping

0x0000 0000	Boot Memory (1)	
0x0010 0000	SRAM	
0x0020 0000	MPB SLAVE0	
0x0030 0000	MPB SLAVE0	
0x0040 0000	ROM	
0x0050 0000	LCDC	
0x0060 0000	UDPHS	
0x0070 0000	USB HOST	
0x0080 0000	MPB SLAVE1	
0x0090 0000	MPB SLAVE1	
0x00A0 0000	MPB SLAVE1	
0x00B0 0000	MPB SLAVE1	

Notes :
(1) Can be ROM, EBI_NCS0 or SRAM depending on BMS and REMAP

Peripheral Mapping

0xFF00 0000	Reserved	16K Bytes
0xFFF7 8000	UDPHS	16K Bytes
0xFFF7 C000	TCO, TC1, TC2	16K Bytes
0xFFF8 0000	MCI0	16K Bytes
0xFFF8 4000	MCI1	16K Bytes
0xFFF8 8000	TWI	16K Bytes
0xFFF8 C000	USART0	16K Bytes
0xFFF9 0000	USART1	16K Bytes
0xFFF9 4000	USART2	16K Bytes
0xFFF9 8000	SSC0	16K Bytes
0xFFF9 C000	SSC1	16K Bytes
0xFFFA 0000	AC97C	16K Bytes
0xFFFA 4000	SPI0	16K Bytes
0xFFFA 8000	SPI1	16K Bytes
0xFFFA C000	CAN0	16K Bytes
0xFFFB 0000	Reserved	16K Bytes
0xFFFB 4000	Reserved	16K Bytes
0xFFFB 8000	PWMC	16K Bytes
0xFFFB C000	EMAC	16K Bytes
0xFFFC 0000	ADCC	16K Bytes
0xFFFC 4000	ISI	16K Bytes
0xFFFC 8000	Reserved	16K Bytes
0xFFFC C000	Reserved	16K Bytes
0xFFFF C000	SYSC	16K Bytes
0xFFFF FFFF		

System Controller Mapping

0xFFFF C000	Reserved	
0xFFFF E200	ECC	512 Bytes
0xFFFF E400	BCRAMC	512 Bytes
0xFFFF E600	DDRSDRC	512 bytes
0xFFFF E800	SMC	512 Bytes
0xFFFF EA00	MATRIX	512 Bytes
0xFFFF EB10	CCFG	
0xFFFF EC00	DMA	512 Bytes
0xFFFF EE00	DBGU	512 Bytes
0xFFFF F000	AIC	512 bytes
0xFFFF F200	PIOA	512 bytes
0xFFFF F400	PIOB	512 Bytes
0xFFFF F600	PIOC	512 bytes
0xFFFF F800	PIOD	512 bytes
0xFFFF FA00	Reserved	512 bytes
0xFFFF FC00	PMC	256 Bytes
0xFFFF FD00	RSTC	16 Bytes
0xFFFF FD10	SHDC	16 Bytes
0xFFFF FD20	RTT	16 Bytes
0xFFFF FD30	PIT	16 Bytes
0xFFFF FD40	WDT	16 Bytes
0xFFFF FD50	GPBR	16 Bytes
0xFFFF FD60	Reserved	
0xFFFF FFFF		

A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High-performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS5 and EBI_SDDRCS. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The banks 8 to 11 are directed to MP Block (Slave 2) and may be used to address external memories. The bank 15 is split into three parts, one reserved for the peripherals that provides access to the Advanced Peripheral Bus (APB), the two others are directed to MP Block (Slave 3) and may provide access to the MP Block APB or to other AHB peripherals.

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot and one after remap. Refer to Table 8-1, "Internal Memory Mapping," on page 23 for details.

8.1 Embedded Memories

- 32 Kbyte ROM
    - Single Cycle Access at full matrix speed
- 32 Kbyte Fast SRAM
    - Single Cycle Access at full matrix speed
- 20 Kbyte MP Block Fast Dual Port RAM (ten 512x36 DPR instances)
    - Used as Dual Port RAM completely managed by MP Block
- 32 Kbyte MP Block Fast Single Port RAM (eight 512x72 SPR instances)
    - Used as Single Port RAM completely managed by MP Block

8.1.1 Internal Memory Mapping

Table 8-1 summarizes the Internal Memory Mapping, depending on the Remap status and the BMS state at reset.

Table 8-1. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 0	BMS = 1	
0x0000 0000	ROM	EBI_NCS0	SRAM
0x0010 0000	SRAM		
0x0020 0000	MP Block Slave 0 (hsel[0])		
0x0030 0000	MP Block Slave 0 (hsel[1])		
0x0040 0000	ROM		

Table 8-1. Internal Memory Mapping (Continued)

0x0050 0000	LCD Controller User Interface
0x0060 0000	USB High Speed Device Interface
0x0070 0000	OHCI USB Host User Interface
0x0080 0000	MP Block Slave 1 (hsel[0])
0x0090 0000	MP Block Slave 1 (hsel[1])
0x00A0 0000	MP Block Slave 1 (hsel[2])
0x00B0 0000	MP Block Slave 1 (hsel[3])

8.1.1.1 Internal 32 Kbyte Fast SRAM

The AT91CAP9S500A/AT91CAP9S250A integrates a 32 Kbyte SRAM, mapped at address 0x0010 0000,which is accessible from the AHB bus. This SRAM is single cycle accessible at full matrix speed.

8.1.1.2 Boot Memory

The AT91CAP9S500A/AT91CAP9S250A Matrix manages a boot memory which depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved at this effect.

If BMS is detected at 1, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface. The default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows to boot on a 16-bit non-volatile memory.

If BMS is detected at 0, the boot memory is the embedded ROM.

8.1.2 Boot Program

- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI DataFlash® connected on NPCS0 of the SPI0
- Boot Uploader in case no valid program is detected in external NVM and supporting several communication media
  - Serial communication on a DBGU
  - USB Bulk Device Port
  - External Memories Mapping

The external memories are accessed through the External Bus Interface. Each Chip Select lines has a 256 Mbyte memory area assigned.

8.2 External Memories

The external memories are accessed through the External Bus Interfaces. Each Chip Select line has a 256 Mbyte memory area assigned.

Refer to .

8.2.1 External Bus Interface

The AT91CAP9S500A/AT91CAP9S250A features one External Bus Interface to offer high bandwidth to the system and to prevent any bottleneck while accessing the external memories.

- Optimized for Application Memory Space support
- Integrates three External Memory Controllers:
  - Static Memory Controller
  - 4-port DDR/SDRAM Controller
  - Burst/CellularRAM Controller
  - ECC Controller for NAND Flash
- Additional logic for NAND Flash and CompactFlash
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 Mbytes linear per chip select)
- Up to 6 chips selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - Burst/CellularRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
- One dedicated chip select:
  - DDR/SDRAM Controller on NCS6

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

8.2.3 DDR/SDRAM Controller

- Supported devices:
  - Standard and Low Power SDRAM (Mobile SDRAM)
  - Mobile DDR
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks

– SDRAM with 16- or 32-bit Data Path

– Mobile DDR with four Internal Banks

– Mobile DDR with 16-bit Data Path

• Programming facilities

– Word, half-word, byte access

– Automatic page break when Memory Boundary has been reached

– Multibank Ping-pong Access

– Timing parameters specified by software

– Automatic refresh operation, refresh rate is programmable

– Multiport (4 Ports)

• Energy-saving capabilities

– Self-refresh, power down and deep power down modes supported

• Error detection

– Refresh Error Interrupt

• DDR/SDRAM Power-up Initialization by software

• SDRAM CAS Latency of 1, 2 and 3 supported

• DDR CAS latency of 3 supported

• Auto Precharge Command not used

8.2.4   Burst Cellular RAM Controller

• Supported devices:

– Synchronous Cellular RAM version 1.0, 1.5 and 2.0

• Numerous configurations supported

– 64K, 128K, 256K, 512K Row Address Memory Parts

– Cellular RAM with 16- or 32-bit Data Path

• Programming facilities

– Word, half-word, byte access

– Automatic page break when Memory Boundary has been reached

– Timing parameters specified by software

– Only Continuous read or write burst supported

• Energy-saving capabilities

– Standby and Deep Power Down (DPD) modes supported

– Low Power features (PASR/TCSR) supported

• Cellular RAM Power-up Initialization by hardware

• Cellular RAM CAS latency of 2 and 3 supported (Version 1.0)

• Cellular RAM CAS latency of 2, 3, 4, 5 and 6 supported (Version 1.5 and 2.0)

• Cellular RAM variable or fixed latency supported (Version 1.5 and 2.0)

• Multiplexed address/data bus supported (Version 2.0)

• Asynchronous and Page mode not supported.

8.2.5   Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by trigging on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

9.   System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that allow configuration of the Matrix and a set of registers for the chip configuration. The chip configuration registers are used to configure:

- EBI chip select assignment and voltage range for external memories
- MP Block

The System Controller peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of System Controller are mapped on the top of the address space. This allows all the registers of the System Controller to be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instructions have an indexing mode of ± 4 Kbytes.

Figure 9-1 on page 28 shows the System Controller block diagram.

Figure 8-1 on page 22 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 System Controller Block Diagram

Figure 9-1. AT91CAP9S500A/AT91CAP9S250A System Controller Block Diagram
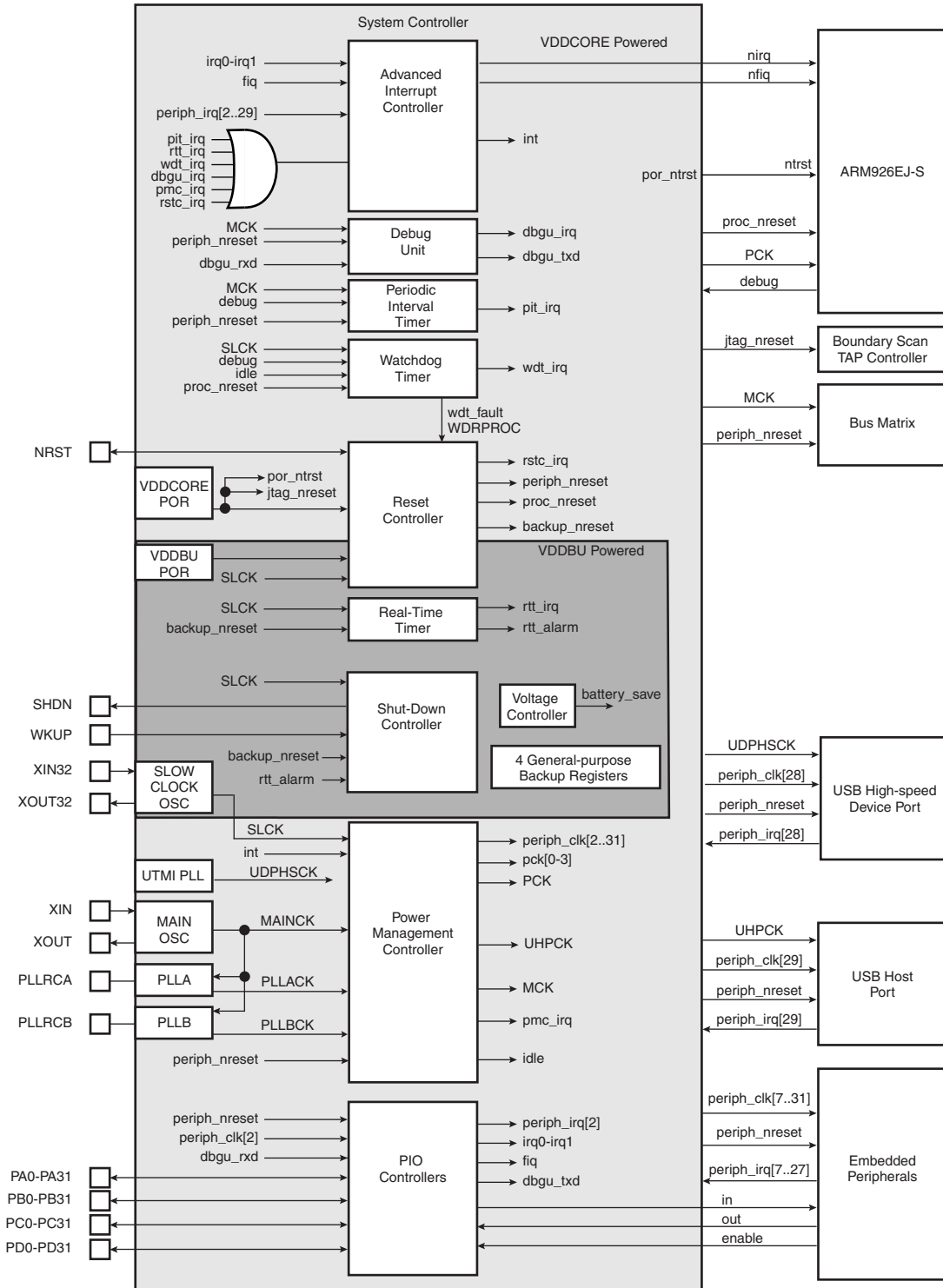
9.2 Reset Controller

- Based on two Power-on-Reset cells
  - One on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

9.3 Shutdown Controller

- Shutdown and Wake-Up logic
  - Software programmable assertion of the SHDN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

9.4 Clock Generator

- Embeds the low power 32,768 Hz Slow Clock Oscillator
  - Provides the permanent Slow Clock SLCK to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 8 to 16 MHz crystals
  - 12 MHz crystal is required for USB High-Speed Device
- Embeds 2 PLLs
  - Output 80 to 200 MHz clocks
  - Integrates an input divider to increase output accuracy
  - 1 MHz minimum input frequency

Figure 9-2. Clock Generator Block Diagram
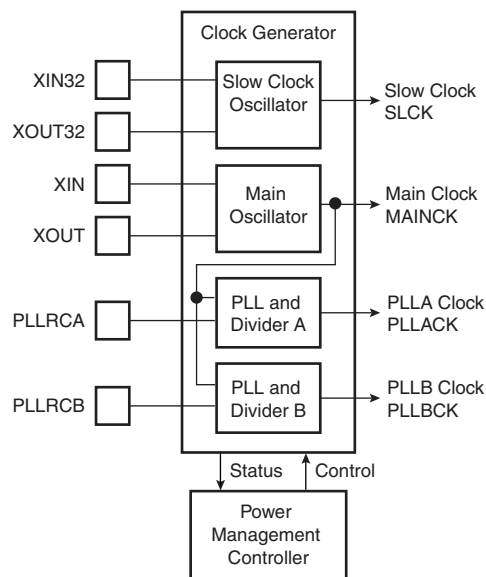
9.5 Power Management Controller

- Provides:
    - the Processor Clock PCK
    - the Master Clock MCK, in particular to the Matrix and the memory interfaces
    - the USB High-speed Device Clock UDPHSCK
    - the USB Host Clock UHPCK
    - independent peripheral clocks, typically at the frequency of MCK
    - four programmable clock outputs: PCK0 to PCK3
- Five flexible operating modes:
    - Normal Mode, processor and peripherals running at a programmable frequency
    - Idle Mode, processor stopped waiting for an interrupt
    - Slow Clock Mode, processor and peripherals running at low frequency
    - Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
    - Backup Mode, Main Power Supplies off, VDDBU powered by a battery

Figure 9-3. AT91CAP9S500A/AT91CAP9S250A Power Management Controller Block Diagram
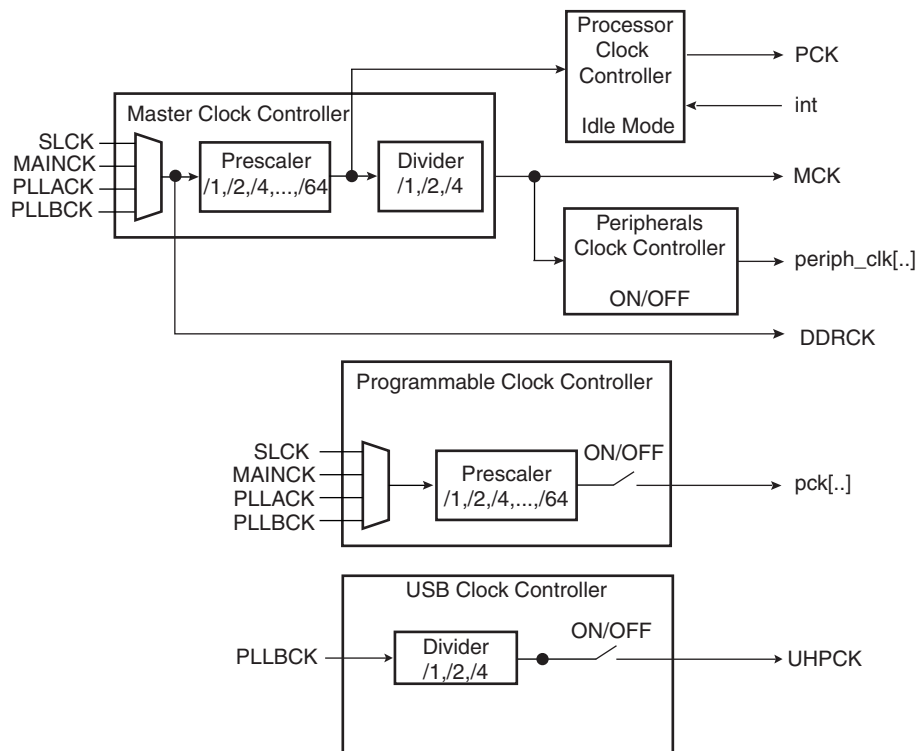
9.6 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real-time OS or Linux/WinCE compliant tick generator

9.7   Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

9.8   Real-time Timer

- Two Real-time Timers, allowing backup of time with different accuracies
    - 32-bit Free-running back-up Counter
    - Integrates a 16-bit programmable prescaler running on the embedded 32,768 Hz oscillator
    - Alarm Register to generate a wake-up of the system through the Shutdown Controller

9.9   General-Purpose Backed-up Registers

- Four 32-bit backup general-purpose registers

9.10   Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
    - Source 0 is reserved for the Fast Interrupt Input (FIQ)
    - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
    - Programmable Edge-triggered or Level-sensitive Internal Sources
    - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- Four External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
    - Drives the Normal Interrupt of the processor
    - Handles priority of the interrupt sources 1 to 31
    - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
    - Optimizes Interrupt Service Routine Branch and Execution
    - One 32-bit Vector Register per interrupt source
    - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
    - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
    - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.11   Debug Unit

- Composed of two functions
    - Two-pin UART
    - Debug Communication Channel (DCC) support

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.12 Chip Identification

- Chip ID: 0x039A03A0
- JTAG ID: 0x05B1B03F
- ARM926 TAP ID: 0x0792603F

9.13 PIO Controllers

- 4 PIO Controllers, PIOA to PIOD, controlling a total of 128 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
  - PIOD has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

10. Peripherals

10.1 User Interface

The peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFFA 0000 and 0xFFFC FFFF. Each user peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 22.

10.2 Identifiers

The AT91CAP9S500A/AT91CAP9S250A embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the AT91CAP9S500A/AT91CAP9S250A. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91CAP9S500A/AT91CAP9S250A Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller Interrupt	
2	PIOA-D	Parallel I/O Controller A to D	
3	MPB0	MP Block Peripheral 0	
4	MPB1	MP Block Peripheral 1	
5	MPB2	MP Block Peripheral 2	
6	MPB3	MP Block Peripheral 3	
7	MPB4	MP Block Peripheral 4	
8	US0	USART 0	
9	US1	USART 1	
10	US2	USART 2	
11	MCI0	Multimedia Card Interface 0	
12	MCI1	Multimedia Card Interface 1	
13	CAN	CAN Controller	
14	TWI	Two-Wire Interface	
15	SPI0	Serial Peripheral Interface 0	
16	SPI1	Serial Peripheral Interface 1	
17	SSC0	Synchronous Serial Controller 0	
18	SSC1	Synchronous Serial Controller 1	
19	AC97	AC97 Controller	
20	TC0, TC1, TC2	Timer/Counter 0, 1 and 2	
21	PWMC	Pulse Width Modulation Controller	
22	EMAC	Ethernet MAC	
23	Reserved	Reserved	

Table 10-1. AT91CAP9S500A/AT91CAP9S250A Peripheral Identifiers (Continued)

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
24	ADCC	ADC Controller	
25	ISI	Image Sensor Interface	
26	LCDC	LCD Controller	
27	DMA	DMA Controller	
28	UDPHS	USB High Speed Device Port	
29	UHP	USB Host Port	
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

10.2.1 Peripheral Interrupts and Clock Control

10.2.1.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the DDR/SDRAM Controller
- the BCRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller
- the MP Block

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.2.1.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ1, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.2.1.3 Timer Counter Interrupts

The three Timer Counter channels interrupt signals are OR-wired together to provide the interrupt source 19 of the Advanced Interrupt Controller. This forces the programmer to read all Timer Counter status registers before branching the right Interrupt Service Routine.

The Timer Counter channels clocks cannot be deactivated independently. Switching off the clock of the Peripheral 19 disables the clock of the 3 channels.

10.3   Peripherals Signals Multiplexing on I/O Lines

The AT91CAP9S500A/AT91CAP9S250A features 4 PIO controllers, PIOA, PIOB, PIOC and PIOD, that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns "Function" and "Comments" have been inserted in this table for the user's own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only may be duplicated within both tables.

The column "Reset State" indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the "Reset State" column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

	PIO Controller A				Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PA0	MCI0_D0	SPI0_MISO		I/O	VDDIOP0		
PA1	MCI0_CD	SPI0_MOSI		I/O	VDDIOP0		
PA2	MCI0_CK	SPI0_SPCK		I/O	VDDIOP0		
PA3	MCI0_D1	SPI0_NPCS1		I/O	VDDIOP0		
PA4	MCI0_D2	SPI0_NPCS2		I/O	VDDIOP0		
PA5	MCI0_D3	SPI0_NPCS0		I/O	VDDIOP0		
PA6	AC97FS			I/O	VDDIOP0		
PA7	AC97CK			I/O	VDDIOP0		
PA8	AC97TX			I/O	VDDIOP0		
PA9	AC97RX			I/O	VDDIOP0		
PA10	IRQ0	PWM1		I/O	VDDIOP0		
PA11	DMARQ0	PWM3		I/O	VDDIOP0		
PA12	CANTX	PCK0		I/O	VDDIOP0		
PA13	CANRX			I/O	VDDIOP0		
PA14	TCLK2	IRQ1		I/O	VDDIOP0		
PA15	DMARQ3	PCK2		I/O	VDDIOP0		
PA16	MCI1_CK	ISI_D0		I/O	VDDIOP1		
PA17	MCI1_CD	ISI_D1		I/O	VDDIOP1		
PA18	MCI1_D0	ISI_D2		I/O	VDDIOP1		
PA19	MCI1_D1	ISI_D3		I/O	VDDIOP1		
PA20	MCI1_D2	ISI_D4		I/O	VDDIOP1		
PA21	MCI1_D3	ISI_D5		I/O	VDDIOP1		
PA22	TXD0	ISI_D6		I/O	VDDIOP1		
PA23	RXD0	ISI_D7		I/O	VDDIOP1		
PA24	RTS0	ISI_PCK		I/O	VDDIOP1		
PA25	CTS0	ISI_HSYNC		I/O	VDDIOP1		
PA26	SCK0	ISI_VSYNC		I/O	VDDIOP1		
PA27	PCK1	ISI_MCK		I/O	VDDIOP1		
PA28	SPI0_NPCS3	ISI_D8		I/O	VDDIOP1		
PA29	TIOA0	ISI_D9		I/O	VDDIOP1		
PA30	TIOB0	ISI_D10		I/O	VDDIOP1		
PA31	DMARQ1	ISI_D11		I/O	VDDIOP1		

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

	PIO Controller B				Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PB0	TF0			I/O	VDDIOP0		
PB1	TK0			I/O	VDDIOP0		
PB2	TD0			I/O	VDDIOP0		
PB3	RD0			I/O	VDDIOP0		
PB4	RK0	TWD		I/O	VDDIOP0		
PB5	RF0	TWCK		I/O	VDDIOP0		
PB6	TF1	TIOA1		I/O	VDDIOP0		
PB7	TK1	TIOB1		I/O	VDDIOP0		
PB8	TD1	PWM2		I/O	VDDIOP0		
PB9	RD1	LCDCC		I/O	VDDIOP0		
PB10	RK1	PCK1		I/O	VDDIOP0		
PB11	RF1			I/O	VDDIOP0		
PB12	SPI1_MISO			I/O	VDDIOP0		
PB13	SPI1_MOSI		AD0	I/O	VDDIOP0		
PB14	SPI1_SPCK		AD1	I/O	VDDIOP0		
PB15	SPI1_NPCS0		AD2	I/O	VDDIOP0		
PB16	SPI1_NPCS1		AD3	I/O	VDDIOP0		
PB17	SPI1_NPCS2		AD4	I/O	VDDIOP0		
PB18	SPI1_NPCS3		AD5	I/O	VDDIOP0		
PB19	PWM0		AD6	I/O	VDDIOP0		
PB20	PWM1		AD7	I/O	VDDIOP0		
PB21	ETXCK/EREFCK	TIOA2		I/O	VDDIOP0		
PB22	ERXDV	TIOB2		I/O	VDDIOP0		
PB23	ETX0	PCK3		I/O	VDDIOP0		
PB24	ETX1			I/O	VDDIOP0		
PB25	ERX0			I/O	VDDIOP0		
PB26	ERX1			I/O	VDDIOP0		
PB27	ERXER			I/O	VDDIOP0		
PB28	ETXEN	TCLK0		I/O	VDDIOP0		
PB29	EMDC	PWM3		I/O	VDDIOP0		
PB30	EMDIO			I/O	VDDIOP0		
PB31	ADTRIG	EF100		I/O	VDDIOP0		

10.3.3 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

	PIO Controller C				Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PC0	LCDVSYNC			I/O	VDDIOP0		
PC1	LCDHSYNC			I/O	VDDIOP0		
PC2	LCDDOTCK			I/O	VDDIOP0		
PC3	LCDDEN	PWM1		I/O	VDDIOP0		
PC4	LCDD0	LCDD3		I/O	VDDIOP0		
PC5	LCDD1	LCDD4		I/O	VDDIOP0		
PC6	LCDD2	LCDD5		I/O	VDDIOP0		
PC7	LCDD3	LCDD6		I/O	VDDIOP0		
PC8	LCDD4	LCDD7		I/O	VDDIOP0		
PC9	LCDD5	LCDD10		I/O	VDDIOP0		
PC10	LCDD6	LCDD11		I/O	VDDIOP0		
PC11	LCDD7	LCDD12		I/O	VDDIOP0		
PC12	LCDD8	LCDD13		I/O	VDDIOP0		
PC13	LCDD9	LCDD14		I/O	VDDIOP0		
PC14	LCDD10	LCDD15		I/O	VDDIOP0		
PC15	LCDD11	LCDD19		I/O	VDDIOP0		
PC16	LCDD12	LCDD20		I/O	VDDIOP0		
PC17	LCDD13	LCDD21		I/O	VDDIOP0		
PC18	LCDD14	LCDD22		I/O	VDDIOP0		
PC19	LCDD15	LCDD23		I/O	VDDIOP0		
PC20	LCDD16	ETX2		I/O	VDDIOP0		
PC21	LCDD17	ETX3		I/O	VDDIOP0		
PC22	LCDD18	ERX2		I/O	VDDIOP0		
PC23	LCDD19	ERX3		I/O	VDDIOP0		
PC24	LCDD20	ETXER		I/O	VDDIOP0		
PC25	LCDD21	ECRS		I/O	VDDIOP0		
PC26	LCDD22	ECOL		I/O	VDDIOP0		
PC27	LCDD23	ERXCK		I/O	VDDIOP0		
PC28	PWM0	TCLK1		I/O	VDDIOP0		
PC29	PCK0	PWM2		I/O	VDDIOP0		
PC30	DRXD			I/O	VDDIOP0		
PC31	DTXD			I/O	VDDIOP0		

10.3.4 PIO Controller D Multiplexing

Table 10-5. Multiplexing on PIO Controller D

	PIO Controller D				Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PD0	TXD1	SPI0_NPCS2		I/O	VDDIOP0		
PD1	RXD1	SPI0_NPCS3		I/O	VDDIOP0		
PD2	TXD2	SPI1_NPCS2		I/O	VDDIOP0		
PD3	RXD2	SPI1_NPCS3		I/O	VDDIOP0		
PD4	FIQ			I/O	VDDIOP0		
PD5	DMARQ2	RTS2		I/O	VDDIOP0		
PD6	NWAIT	CTS2		I/O	VDDIOM		
PD7	NCS4/CFCS0	RTS1		I/O	VDDIOM		
PD8	NCS5/CFCS1	CTS1		I/O	VDDIOM		
PD9	CFCE1	SCK2		I/O	VDDIOM		
PD10	CFCE2	SCK1		I/O	VDDIOM		
PD11	NCS2			I/O	VDDIOM		
PD12	A23			A23	VDDIOM		
PD13	A24			A24	VDDIOM		
PD14	A25/CFRNW			A25	VDDIOM		
PD15	NCS3/NANDCS			I/O	VDDIOM		
PD16	D16			I/O	VDDIOM		
PD17	D17			I/O	VDDIOM		
PD18	D18			I/O	VDDIOM		
PD19	D19			I/O	VDDIOM		
PD20	D20			I/O	VDDIOM		
PD21	D21			I/O	VDDIOM		
PD22	D22			I/O	VDDIOM		
PD23	D23			I/O	VDDIOM		
PD24	D24			I/O	VDDIOM		
PD25	D25			I/O	VDDIOM		
PD26	D26			I/O	VDDIOM		
PD27	D27			I/O	VDDIOM		
PD28	D28			I/O	VDDIOM		
PD29	D29			I/O	VDDIOM		
PD30	D30			I/O	VDDIOM		
PD31	D31			I/O	VDDIOM		

10.4 Embedded Peripherals

10.4.1 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.4.2 Two-wire Interface

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

10.4.3 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit

- IrDA modulation and demodulation
    - Communication at up to 115.2 Kbps
- Test Modes
    - Remote Loopback, Local Loopback, Automatic Echo

10.4.4   Synchronous Serial Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.4.5   AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
    - One RX and one TX channel dedicated to the AC97 Analog Front end control
    - One RX and one TX channel for data transfers, associated with a PDC
    - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length
    - Variable sampling rate AC97 Codec Interface (48KHz and below)

10.4.6   Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
    - Frequency Measurement
    - Event Counting
    - Interval Measurement
    - Pulse Generation
    - Delay Timing
    - Pulse Width Modulation
    - Up/down Capabilities
- Each channel is user-configurable and contains:
    - Three external clock inputs
    - Five internal clock inputs
    - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.4.7 Pulse Width Modulation Controller

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
    - A Modulo n counter providing eleven clocks
    - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
    - Independent Enable Disable Commands
    - Independent Clock Selection
    - Independent Period and Duty Cycle, with Double Bufferization
    - Programmable selection of the output waveform polarity
    - Programmable center or left aligned output waveform

10.4.8 Multimedia Card Interface

- 2 double-channel Multimedia Card Interface, allowing concurrent transfers with 2 cards
- Compatibility with MultiMedia Card Specification Version 3.31
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.0.
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- Each MCI has one slot supporting
    - One MultiMediaCard bus (up to 30 cards) or
    - One SD Memory Card
    - One SDIO Card
- Support for stream, block and multi-block data read and write

10.4.9 CAN Controller

- Fully compliant with 16-mailbox CAN 2.0A and 2.0B CAN Controllers
- Bit rates up to 1Mbit/s.
- Object-oriented mailboxes, each with the following properties:
    - CAN Specification 2.0 Part A or 2.0 Part B Programmable for Each Message
    - Object Configurable as receive (with overwrite or not) or transmit
    - Local Tag and Mask Filters up to 29-bit Identifier/Channel
    - 32 bits access to Data registers for each mailbox data object
    - Uses a 16-bit time stamp on receive and transmit message
    - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
    - 16-bit internal timer for Time Stamping and Network synchronization
    - Programmable reception buffer length up to 16 mailbox object
    - Priority Management between transmission mailboxes
    - Autobaud and listening mode
    - Low power mode and programmable wake-up on bus activity or by the application
    - Data, Remote, Error and Overload Frame handling

10.4.10 USB Host Port

- Compliance with OHCI Rev 1.0 Specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-speed 1.5 Mbps and Full-speed 12 Mbps devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the Matrix
- Internal DMA Controller, operating as a Master on Bus Matrix

10.4.11 USB High Speed Device Port

- USB V2.0 high-speed compliant, 480 MBits per second
- Embedded USB V2.0 UTMI+ high-speed transceiver
- Embedded 4K-byte dual-port RAM for endpoints
- Embedded 6 channels DMA controller
- Suspend/Resume logic
- Up to 2 or 3 banks for isochronous and bulk endpoints
- Seven endpoints:
    - Endpoint 0: 64 bytes, 1 bank mode
    - Endpoint 1 & 2: 512 bytes, 2 banks mode, HS isochronous capable
    - Endpoint 3 & 4: 64 bytes, 3 banks mode
    - Endpoint 5 & 6: 1024 bytes, 3 banks mode, HS isochronous capable

10.4.12 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D-DMA Controller for management of virtual Frame Buffer
    - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering

10.4.13 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability

- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- Internal DMA Controller, operating as a Master on Bus Matrix
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

10.4.14 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats
- Preview scaler to generate smaller size image
- Programmable frame capture rate
- Internal DMA Controller, operating as a Master on Bus Matrix

11. Metal Programmable Block

The Metal Programmable Block (MPBlock) is connected to internal resources as the AHB bus or interrupts and to external resources as dedicated I/O pads or UTMI+ core.

The MPBlock may be used to implement the Advanced High-speed Bus (AHB) or Advanced Peripheral Bus (APB) custom peripherals. The MPBlock adds approximately 500K or 250K gates of standard cell custom logic to the AT91CAP9S500A/AT91CAP9S250A base design.

Figure 11-1 shows the MPBlock and its connections to internal or external resources.

Figure 11-1. MPBlock Connectivity
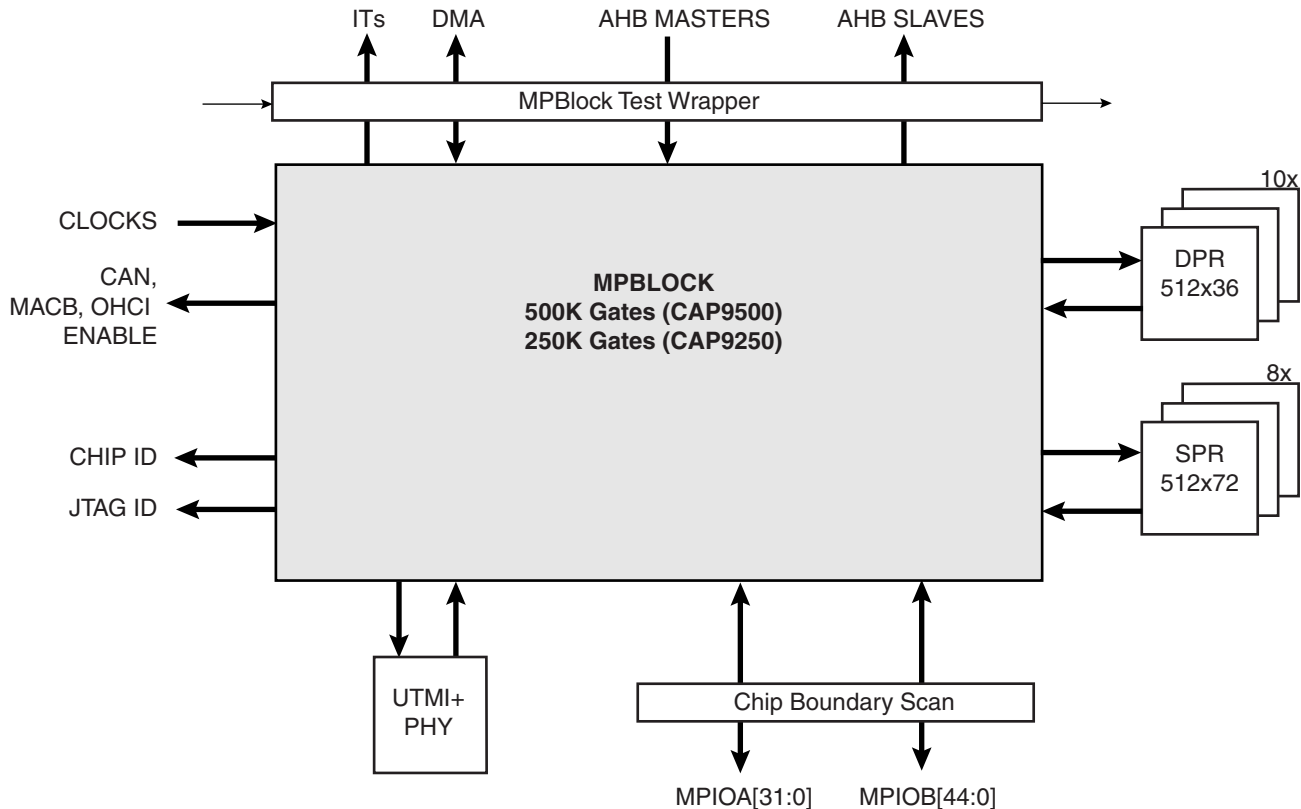
11.1 Internal Connectivity

In order to connect the MPBlock custom peripheral to the AT91CAP9S500A/AT91CAP9S250A base design, the following connections are made.

11.1.1 Clocks

The MPBlock receives the following clocks:

- 32,768 Hz Slow Clock
- 8 to 16 MHz Main Oscillator Clock
- PLLA Clock
- PLLB Clock
- 48 MHz USB Clock
- 12 MHz USB Clock

- 30 or 60 MHz UTMI+ USB Clock

- MCK System Clock

- DDRCK Dual Rate System Clock

- PCK Processor Clock

- 5 Gated Peripherals Clock (for AHB and/or APB peripherals) corresponding to Peripheral ID 3 to 7

11.1.2 AHB Master Buses

The MPBlock may implement up to three AHB masters, each having a dedicated AHB master bus connected to the Bus Matrix.

11.1.3 AHB Slave Buses

The MPBlock receives four different AHB slave buses coming from the Bus Matrix. Each bus has two or four select signals that can implement up to 12 AHB slaves.

11.1.4 Interrupts

The MPBlock is connected to 5 dedicated interrupt lines corresponding to Peripheral ID 3 to 9.

It is also connected to two other interrupt lines (through OR gate) corresponding to Peripheral ID 1 and 2

11.1.5 DMA Channels

The MPBlock is connected to 4 DMA hardware handshaking interfaces, allowing it to implement up to 4 DMA enabled peripherals.

11.1.6 Peripheral DMA Channels

The MPBlock is not connected to the Peripheral DMA Controller. In order to implement Peripheral DMA Controller (PDC) enabled APB peripherals, a PDC and an AHB-to-APB Bridge must be integrated into the MPBlock using one AHB master and one AHB slave bus.

11.1.7 MPBlock Single Port RAMs

The MPBlock is connected to eight instances of 512x72 High-Speed Single Port RAMs.

The MPBlock has control over all memory connections.

11.1.8 MPBlock Dual Port RAMs

The MPBlock is connected to ten instances of 512x36 High-Speed Dual Port RAMs.

The MPBlock has control over all memory connections.

11.1.9 Optional Peripherals Enable

The MPBlock drives the enable of the optional peripherals, and so can enable or disable any of the optional peripherals.

11.2 External Connectivity

The MPBlock is connected to the following external resources.

11.2.1 Dedicated I/O Lines

The MPBlock is directly connected to 77 (32 MPIOA and 45 MPIOB lines) dedicated I/O Pads with the following features:

- Supply/Drive control pin (needed for high-speed or low voltage interfaces)
- Pull-up control pin
- Supported logic levels include:
    - LVCMOS33 at 100 MHz maximum frequency
    - LVCMOS25 at 50 MHz maximum frequency
    - LVCMOS18 at 100 MHz maximum frequency

Only 32 dedicated I/O pins are available in the TFBGA324 package.

11.2.2 UTMI+ Transceiver

The MPBlock may be connected to the UTMI+ transceiver. As only one UTMI+ transceiver is available, the USB High-speed Device and the MPBlock do not have access to the UTMI+ at the same time. However, a dual role Master-Slave USB High-Speed may be implemented by using the USB High-speed Device and integrating a High-speed Host in the MPBlock as the switching between both is generated inside the MPBlock.

11.3 Prototyping Solution

In order to prototype the final custom design, a Prototyping Platform version of the AT91CAP9S500A/AT91CAP9S250A design has been created. The platform maps APB and AHB masters or slaves into the FPGA located outside the chip with the following features and restrictions:

- AT91CAP9S500A/AT91CAP9S250A to FPGA interface is provided to prototype AHB masters and slave into the external FPGA exactly as if it were in MPBlock.
- Prototyped AHB Masters
    - Prototyped AHB Masters have access to AT91CAP9S500A/AT91CAP9S250A slave resources.
    - Prototyped AHB Masters have access to MPBlock (FPGA) slave resources.
- Prototyped AHB Slaves
    - Prototyped AHB Slaves may be accessed from AT91CAP9S500A/AT91CAP9S250A master resources.
    - Prototyped AHB Slaves may be accessed from MPBlock (FPGA) resources.
- Prototyped APB Slaves
    - APB bus must be created locally in the FPGA by implementing AHB to APB bridge. Peripheral DMA controller may also be necessary to implement locally in the FPGA in order to prototype PDC enabled APB peripherals.

Figure 11-2 shows a typical prototyping solution.

Figure 11-2. Typical Prototyping Solution

CAP9500
CAP9250

MASTERS

ARM926EJ-S

EBI

Bus Matrix

4-channel DMA

Metal Programmable Block
500K Gates (CAP9500)
250K Gates (CAP9250)

FPGA Interface

MPIOA[31:0]   MPIOB[44:0]

FPGA

CAP9500/CAP9250 FPGA Interface
Local AHB Matrix

AHB MASTER
DPR

AHB 2 APB BRIDGE

PDC

RAM

AHB MASTER
DPR

AHB SLAVE

APB

DPR
APB SLAVE

APB SLAVE

MPBlock
Emulation Area
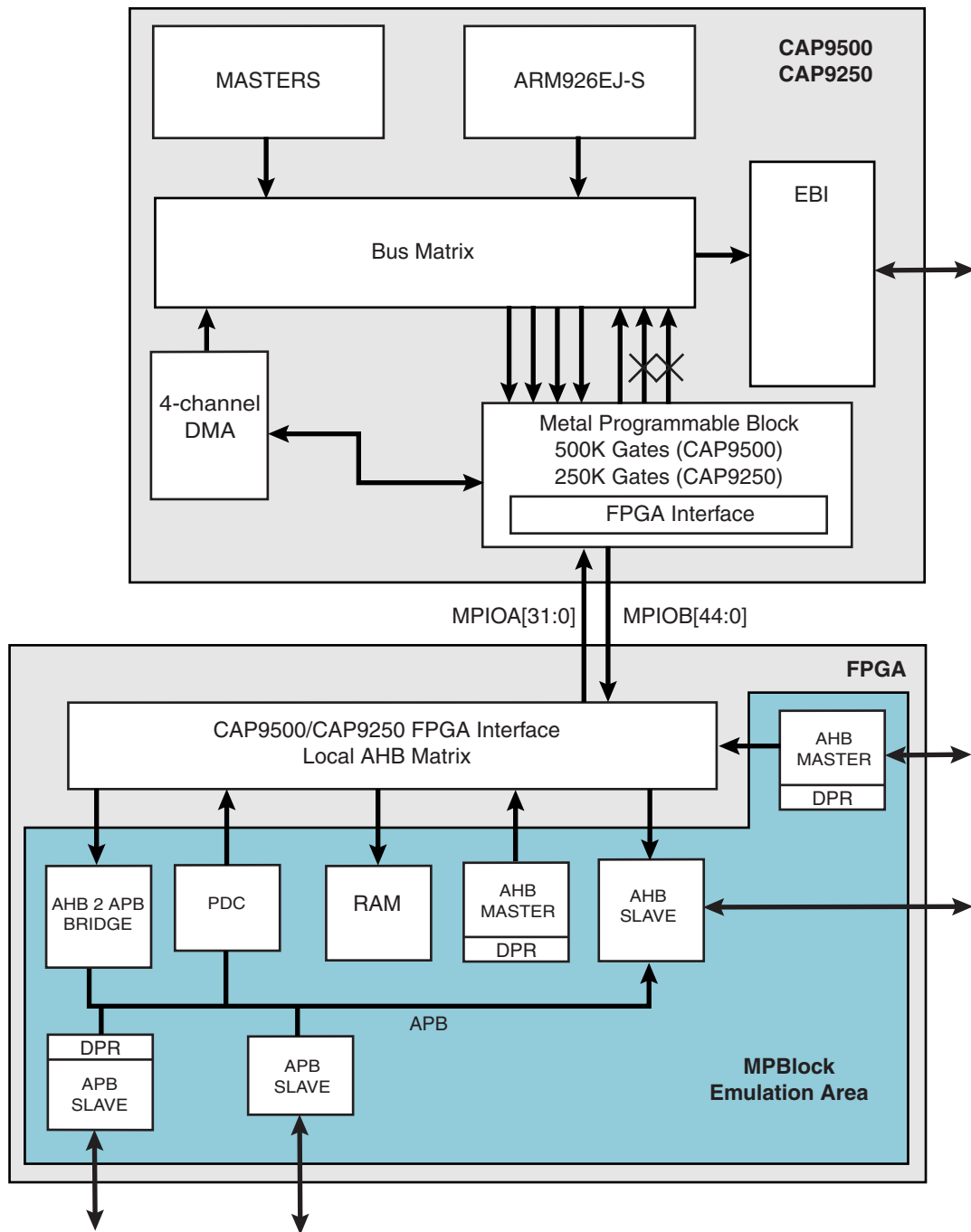
12. Package Drawing

Figure 12-1. 400-ball BGA Package Drawing
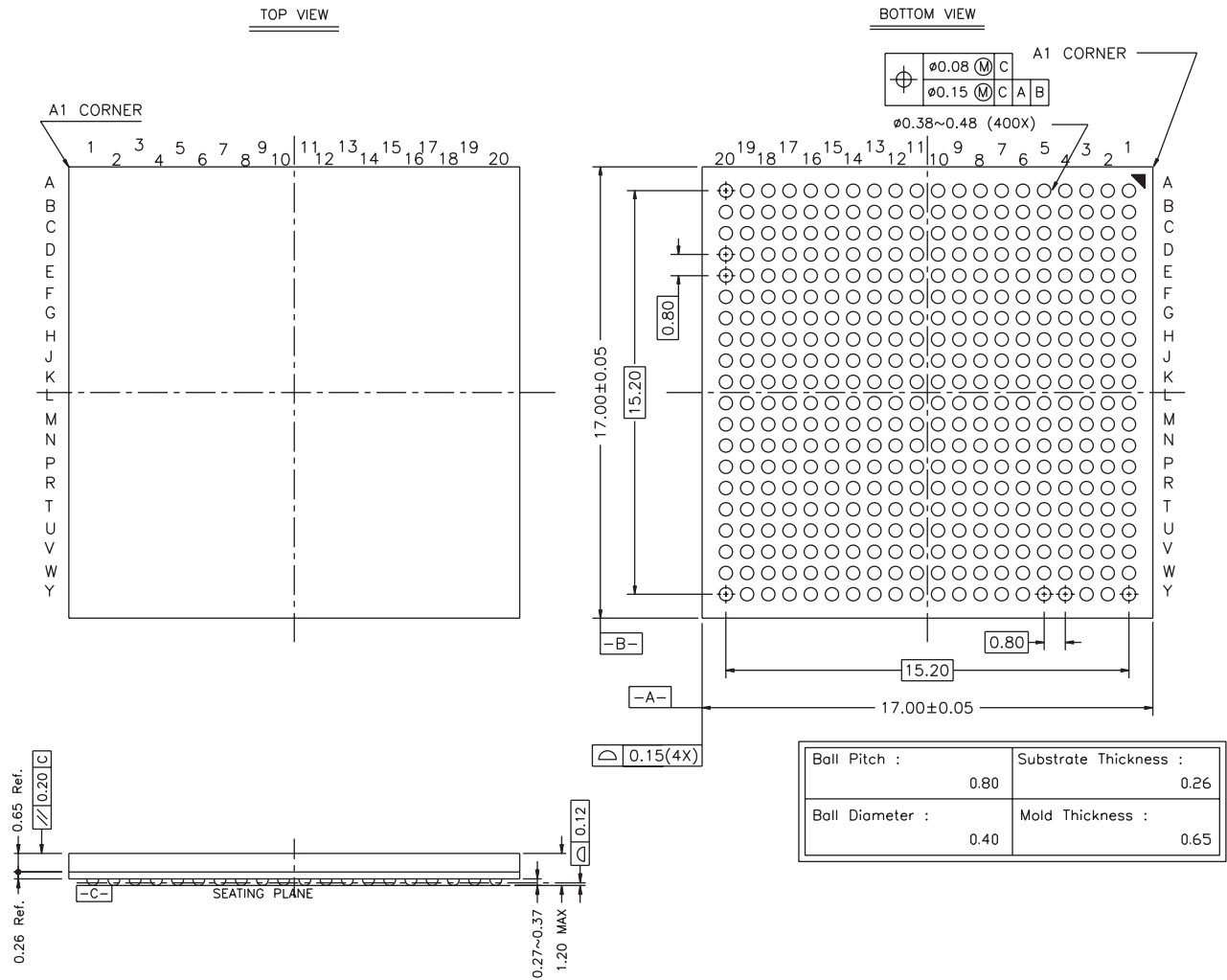
13. Ordering Information

Table 13-1. CAP9 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91CAPS250A-CJ	BGA400	RoHS Compliant	Industrial -40°C to 85°C
AT91CAPS9500A-CJ			

14. Revision History

Table 14-1.

Document Ref.	Comments	Change Request Ref.
6264AS	First issue.	

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