

DATA SHEET

74ALVT16501

**2.5V/3.3V 18-bit universal bus
transceiver (3-State)**

Product specification
Supersedes data of 1997 May 01
IC23 Data Handbook

1998 Feb 13

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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FEATURES

- 18-bit bidirectional bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL and LVTTTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 400V per Machine Model

DESCRIPTION

The 74ALVT16501 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and \overline{OEBA}), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses \overline{OEBA} , LEBA and CPBA. The output enables are complimentary (OEAB is active High, and \overline{OEBA} is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$	1.9 2.5	1.4 1.8	ns
C_{IN}	Input capacitance (Control pins)	$V_I = 0\text{V}$ or V_{CC}	4	4	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O} = 0\text{V}$ or V_{CC}	8	8	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ALVT16501 DL	AV16501 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ALVT16501 DGG	AV16501 DGG	SOT364-1

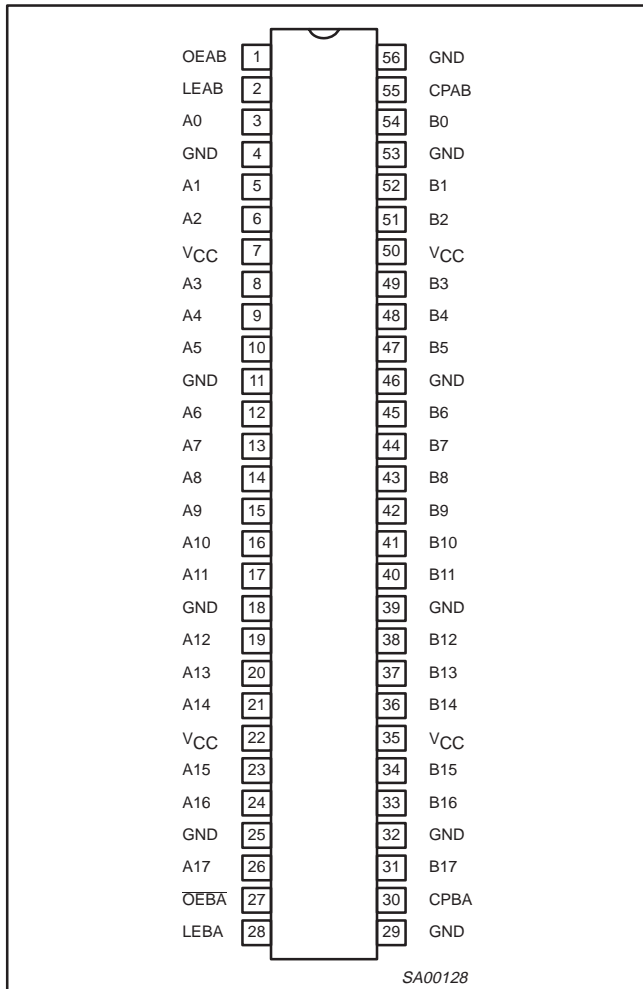
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	\overline{OEBA}	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53, 29, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

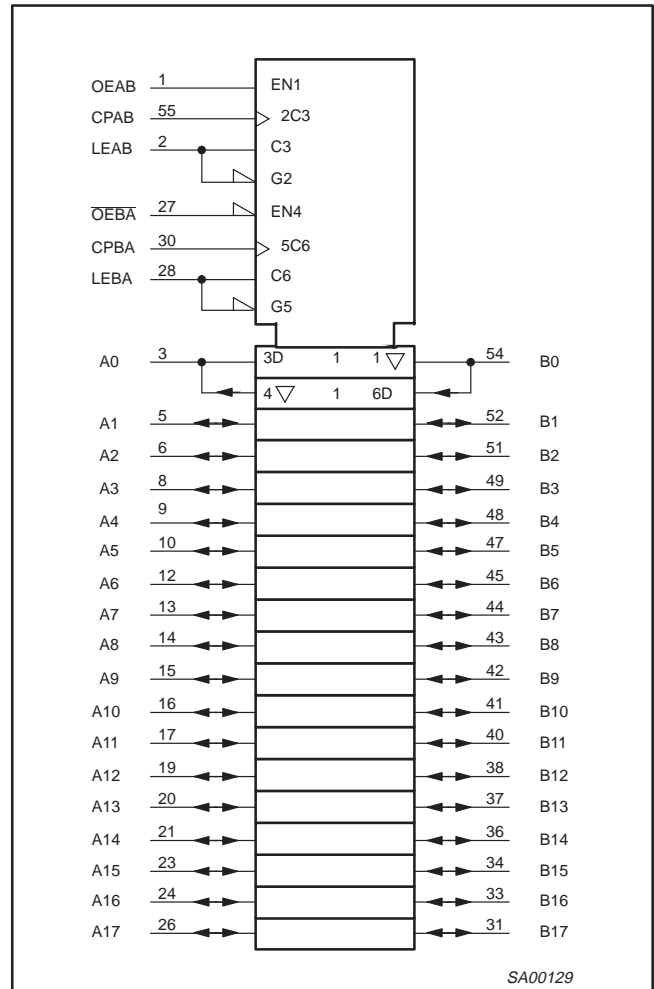
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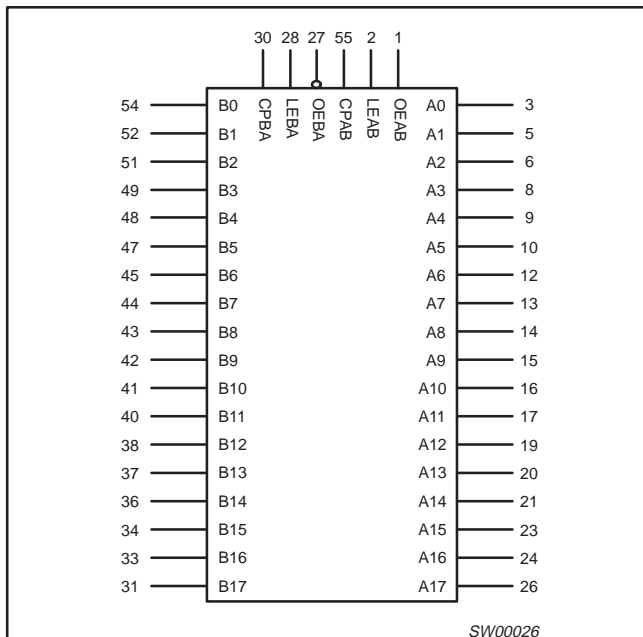
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



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FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

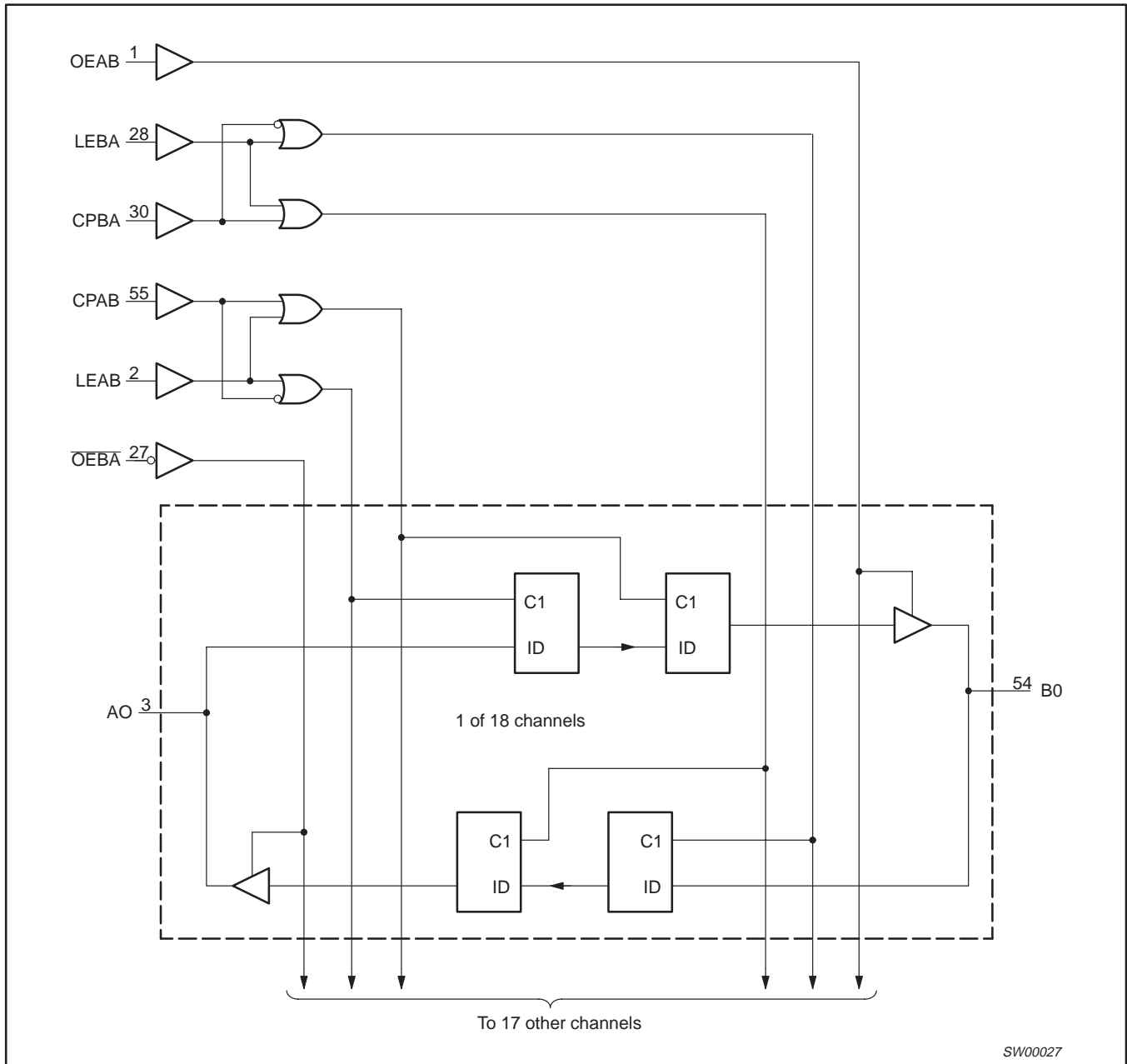
NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CPBA.

- H = High voltage level
- h = High voltage level one set-up time prior to the Enable or Clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Enable or Clock transition
- NC= No Change
- X = Don't care
- Z = High Impedence "off" state
- ↓ = High-to-Low Enable or Clock transition

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LOGIC DIAGRAM



2.5V/3.3V 18-bit universal bus transceiver (3-State)

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ABSOLUTE MAXIMUM RATINGS 1, 2

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		-8		-32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3V \pm 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100 μ A	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100 μ A		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	\pm 1	μ A
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴	0.1	20	
		V _{CC} = 3.6V; V _I = V _{CC}		0.5	10	
		V _{CC} = 3.6V; V _I = 0V		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	\pm 100	μ A
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V	75	130		μ A
		V _{CC} = 3V; V _I = 2.0V	-75	-140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	\pm 500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	μ A
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} \leq 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1.0	\pm 100	μ A
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.06	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		3.5	5	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.06	0.1	
Δ I _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V \pm 0.3V a transition time of 100 μ sec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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AC CHARACTERISTICS (3.3V ± 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{\text{CC}} = 3.3\text{V} \pm 0.3\text{V}$			
			MIN	TYP ¹	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.4 1.8	3.4 3.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	1.5 1.5	2.1 2.7	3.4 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	1.9 2.7	3.2 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.0 1.4	3.1 3.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	2.0 2.0	2.7 2.5	4.2 4.0	ns

NOTE:1. All typical values are at $V_{\text{CC}} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{\text{CC}} = 3.3\text{V} \pm 0.3\text{V}$		
			MIN	TYP	
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup time, High or Low An to CPAB or Bn to CPBA	4	2.0 2.0	0.5 0.7	ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold time, High or Low An to CPAB or Bn to CPBA	4	1.0 1.0	-0.6 -0.3	ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup time, High or Low An to LEAB or Bn to LEBA	4	1.0 1.0	-0.6 -0.1	ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.0 1.5	0.1 0.6	ns
$t_{\text{W(H)}}$ $t_{\text{W(L)}}$	Pulse width, High or Low CPAB or CPBA	1	2.0 2.0		ns
$t_{\text{W(H)}}$	LEAB or LEBA pulse width, High	3	1.5		ns

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2			V
		V _{CC} = 2.3V; I _{OH} = -8mA	1.8			
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100μA		0.07	0.2	V
		V _{CC} = 2.3V; I _{OL} = 24mA		0.3	0.5	
		V _{CC} = 2.3V; I _{OL} = 8mA			0.4	
V _{RST}	Power-up output low voltage ⁷	V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 2.7V; V _I = V _{CC} or GND	Control pins	0.1	±1	μA
		V _{CC} = 0 or 2.7V; V _I = 5.5V		0.1	10	
		V _{CC} = 2.7V; V _I = V _{CC}	Data pins ⁴	0.1	1	
		V _{CC} = 2.7V; V _I = 0		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA
I _{HOLD}	Bus Hold current Data inputs ⁶	V _{CC} = 2.3V; V _I = 0.7V		90		μA
		V _{CC} = 2.3V; V _I = 1.7V		-75		
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.3V		5	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care		4	100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		2.5	4.5	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.01	0.4	mA

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP ¹	MAX	
f_{MAX}	Maximum clock frequency	1	150			MHz
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.0 1.0	1.9 2.5	3.0 3.8	ns
t_{PLH} t_{PHL}	Propagation delay Clock Low or High LEAB to Bn or LEBA to An	3	2.0 2.0	3.0 3.5	4.5 5.4	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	2.9 3.7	4.9 5.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.5 1.5	3.1 2.1	4.5 2.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	3.0 2.4	4.2 3.6	ns

NOTE:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.**AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

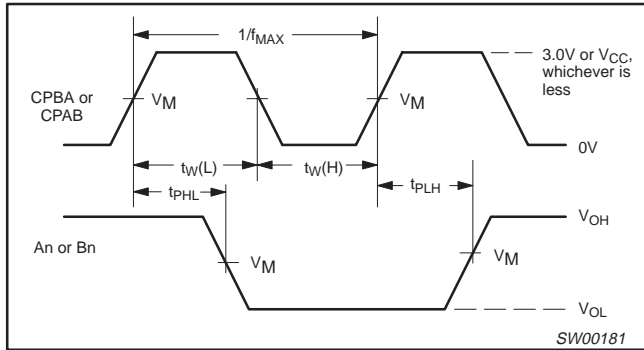
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 2.5V \pm 0.2V$		
			MIN	TYP	
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup time, High or Low An to CPAB or Bn to CPBA	4	1.9 2.5	0.4 1.2	ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold time, High or Low An to CPAB or Bn to CPBA	4	0 1.0	-1.2 -0.4	ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup time, High or Low An to LEAB or Bn to LEBA	4	0 1.0	-1.0 -0.5	ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold time, High or Low An to LEAB or Bn to LEBA	4	1.0 2.0	-0.5 1.0	ns
$t_{\text{W(H)}}$ $t_{\text{W(L)}}$	Pulse width, High or Low CPAB or CPBA	1	3.0 3.0		ns
$t_{\text{W(H)}}$	LEAB or LEBA pulse width, High	3	1.5		ns

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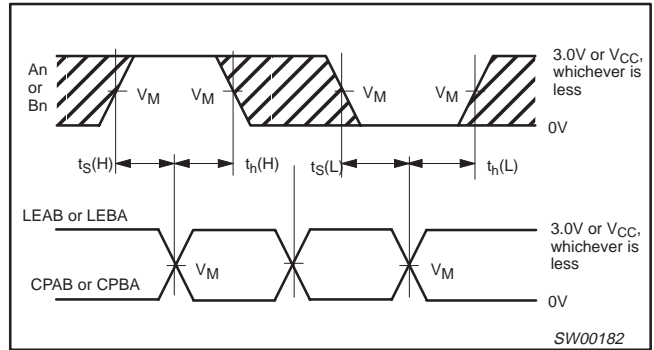
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AC WAVEFORMS

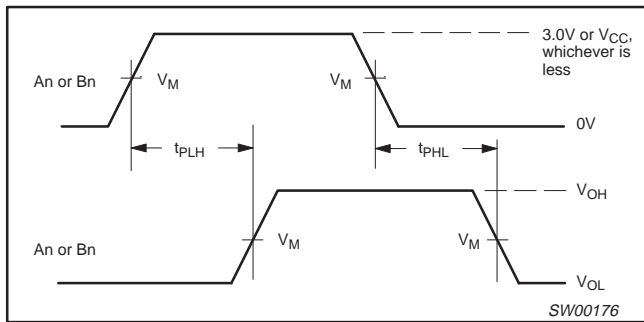
$V_M = 1.5V$ at $V_{CC} \geq 3.0V$, $V_M = V_{CC}/2$ at $V_{CC} \leq 2.7V$
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 3.0V$, $V_X = V_{OL} + 0.150V$ at $V_{CC} \leq 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 3.0V$, $V_Y = V_{OH} - 0.150V$ at $V_{CC} \leq 2.7V$



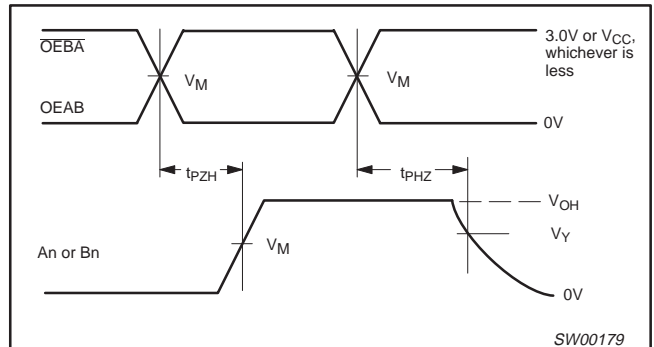
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



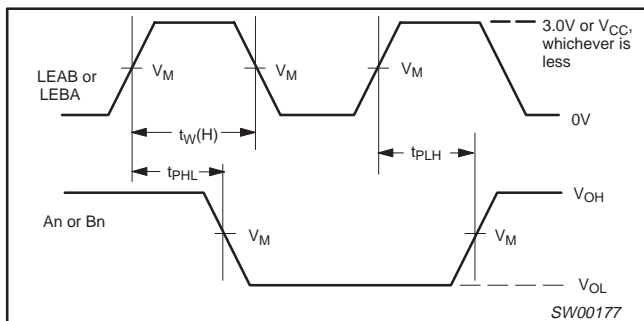
Waveform 4. Data Setup and Hold Times



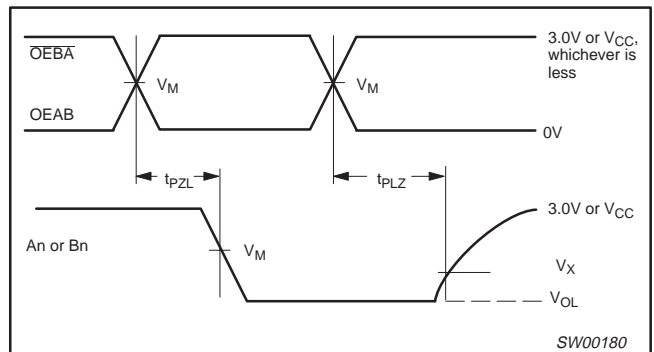
Waveform 2. Propagation Delay, Transparent Mode



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width

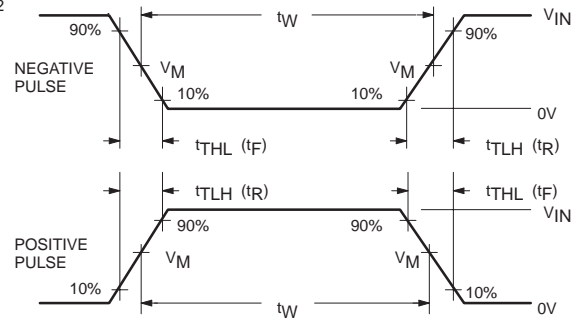
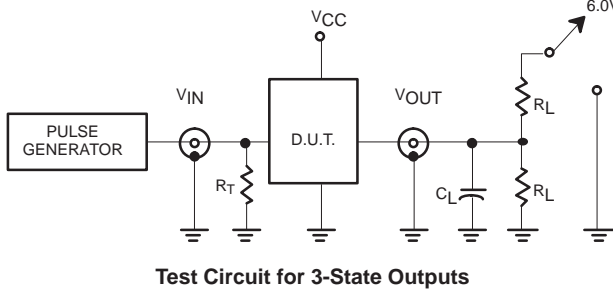


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

2.5V/3.3V 18-bit universal bus transceiver (3-State)

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TEST CIRCUIT



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

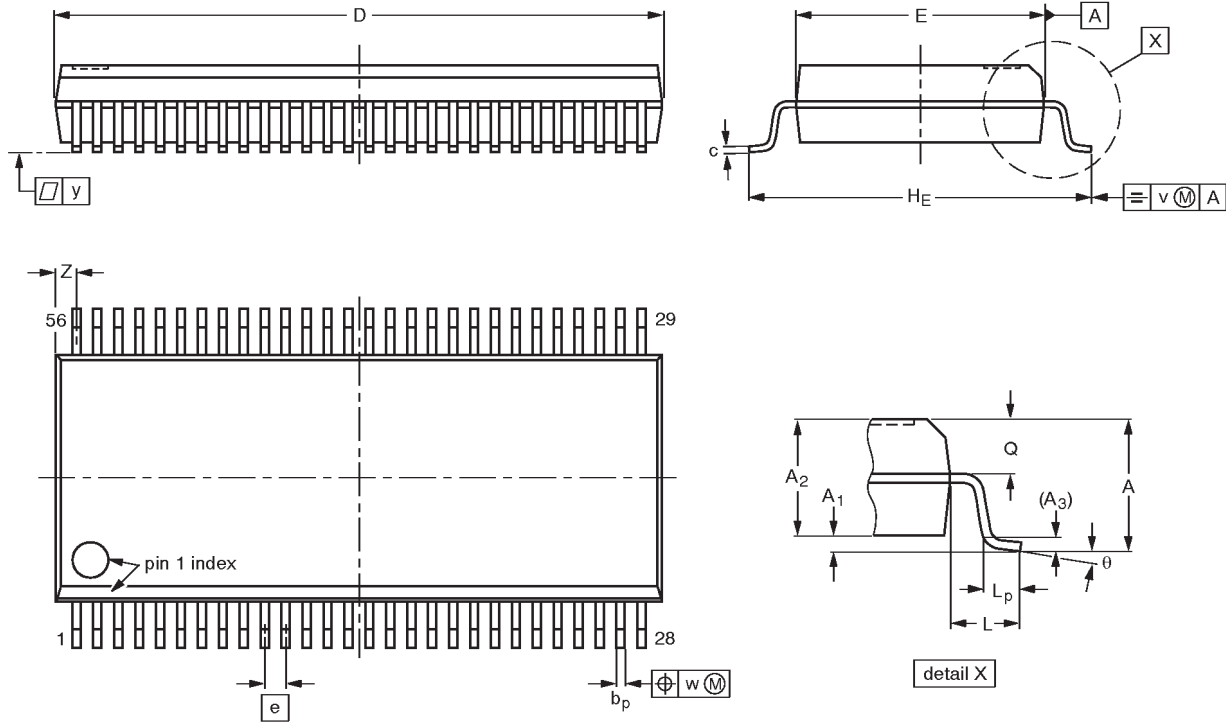
SW00220

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16501

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

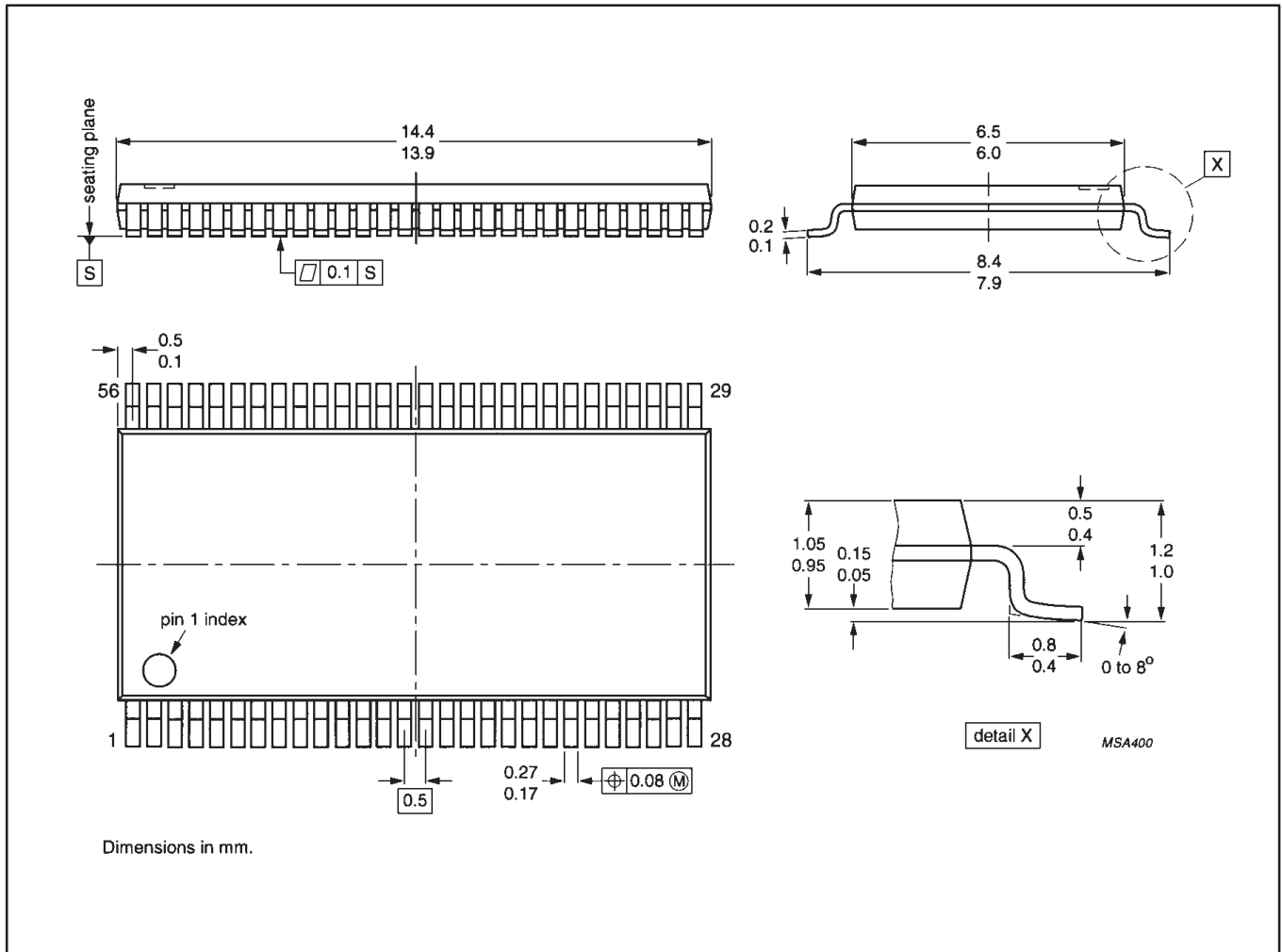
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16501

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16501

NOTES

2.5V/3.3V 18-bit universal bus transceiver (3-State)

74ALVT16501

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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