



STB160NF3LL

N-channel 30V - 0.0028Ω - 160A - D²PAK
STripFET™ III Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB160NF3LL	30V	<0.0033Ω	160A ⁽¹⁾

1. Value limited by wire bonding

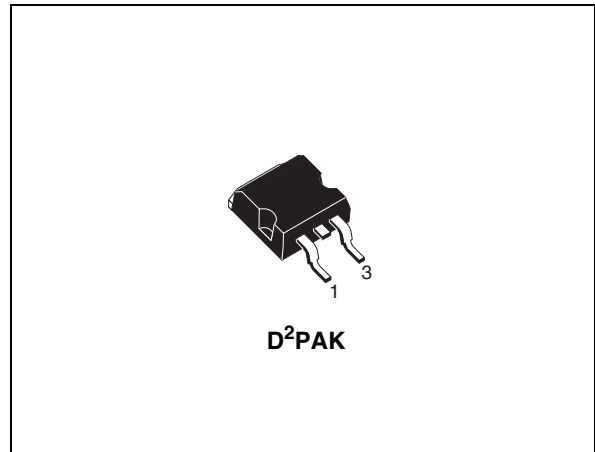
- 100% avalanche tested
- Ultra low on-resistance
- Logic level device
- Low threshold drive

Description

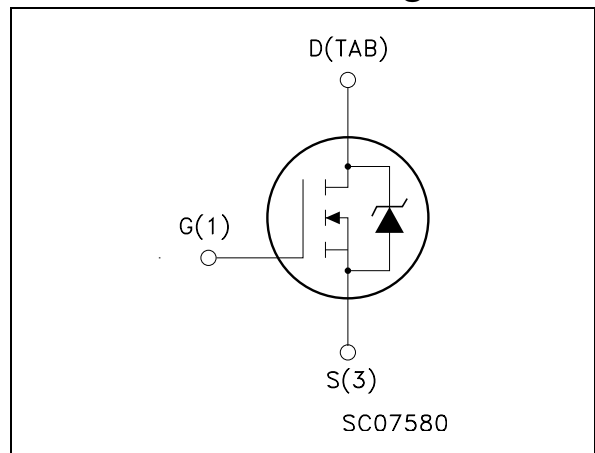
The STB100NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter applications where high efficiency is to be achieved.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB160NF3LL	B160NF3LL	D ² PAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	30	V
V_{GS}	Gate- source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	160	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	640	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating Factor	2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery avalanche energy	2	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.2	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 60\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting $T_j = 25^\circ\text{C}$, $I_D = 30\text{A}$, $V_{DD} = 15\text{V}$

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose ⁽¹⁾	300	$^\circ\text{C}$

1. for $t \leq 10\text{sec}$. 1.6mm from case

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20\text{V}$ $V_{DS} = 20\text{V}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 80\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 80\text{A}$		0.0028 0.0035	0.0033 0.0048	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 80\text{A}$		110		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		5500 1700 300		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 15\text{V}$, $I_D = 80\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see Figure 13)		50 350 150 130		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 24\text{V}$, $I_D = 160\text{A}$, $V_{GS} = 4.5\text{V}$, $R_G = 4.7\Omega$ (see Figure 14)		80 30 45	110	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				160 640	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 160A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 160A$, $di/dt = 100A/\mu s$, $V_{DD} = 20V$, $T_j = 150^\circ C$ (see Figure 15)		100 250 6		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

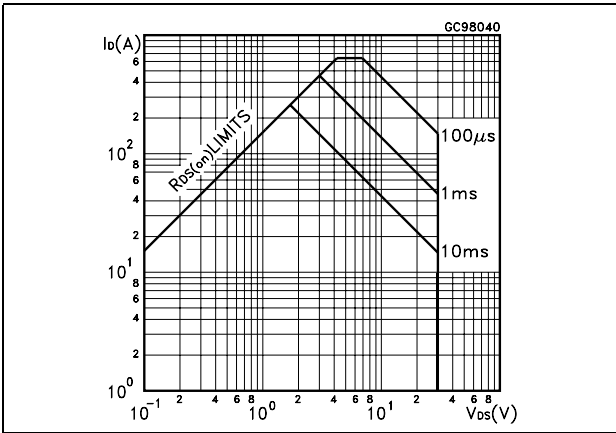


Figure 2. Thermal impedance

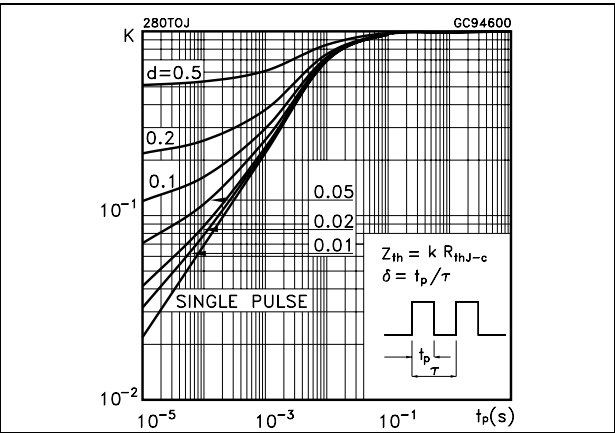


Figure 3. Output characteristics

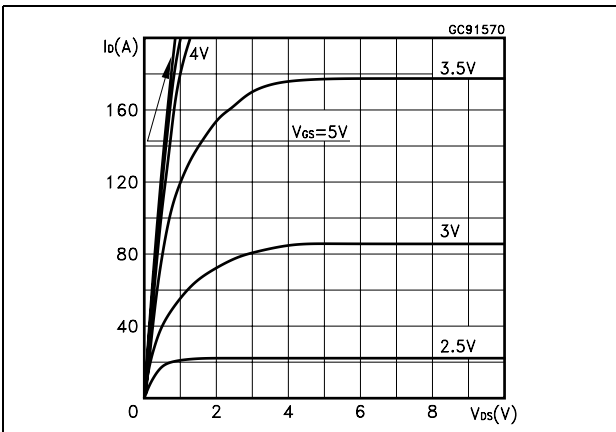


Figure 4. Transfer characteristics

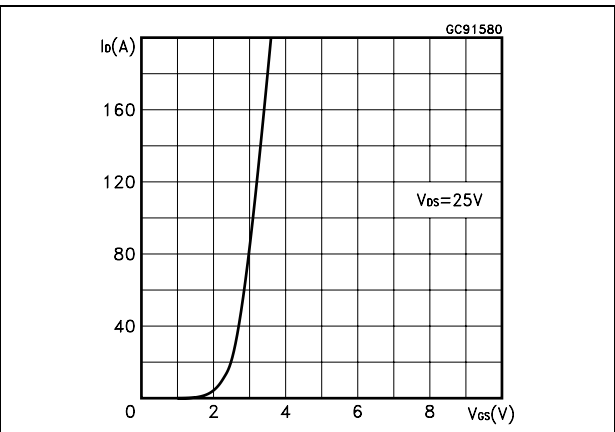


Figure 5. Transconductance

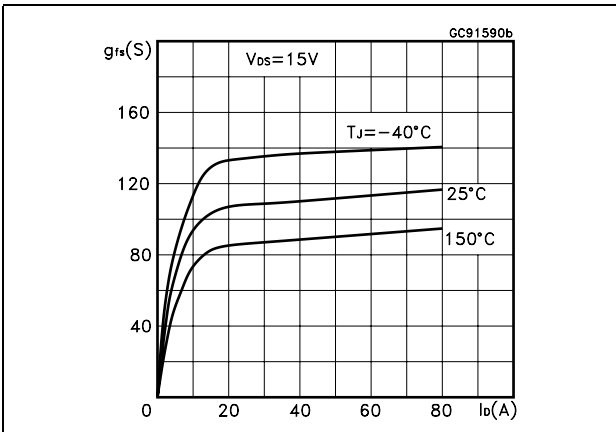


Figure 6. Static drain-source on resistance

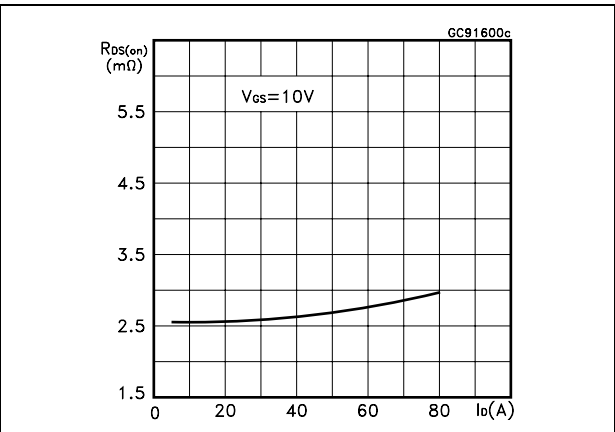


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

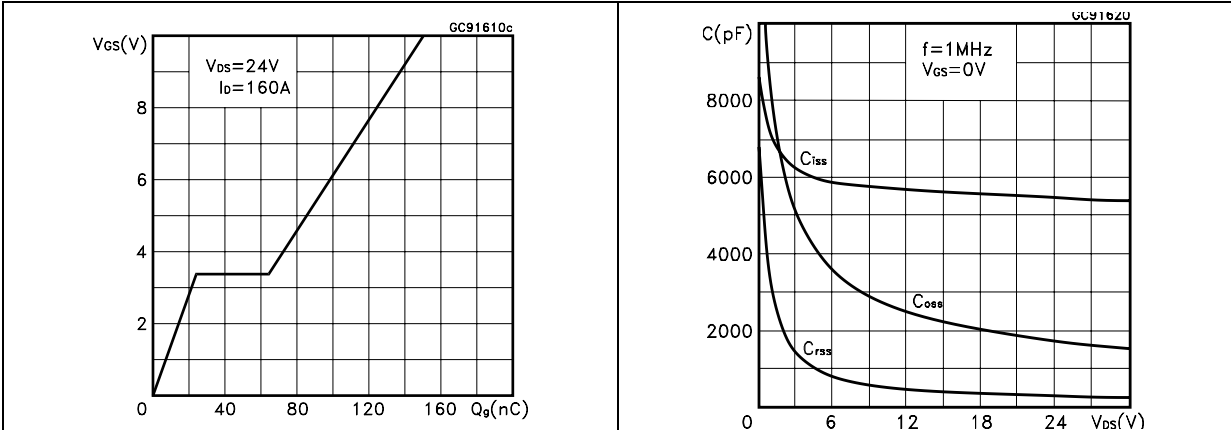


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

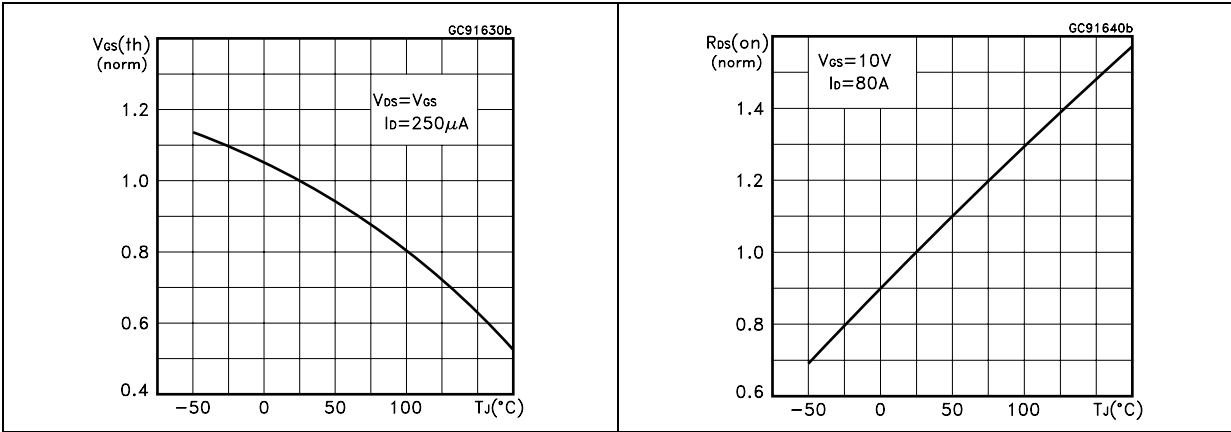
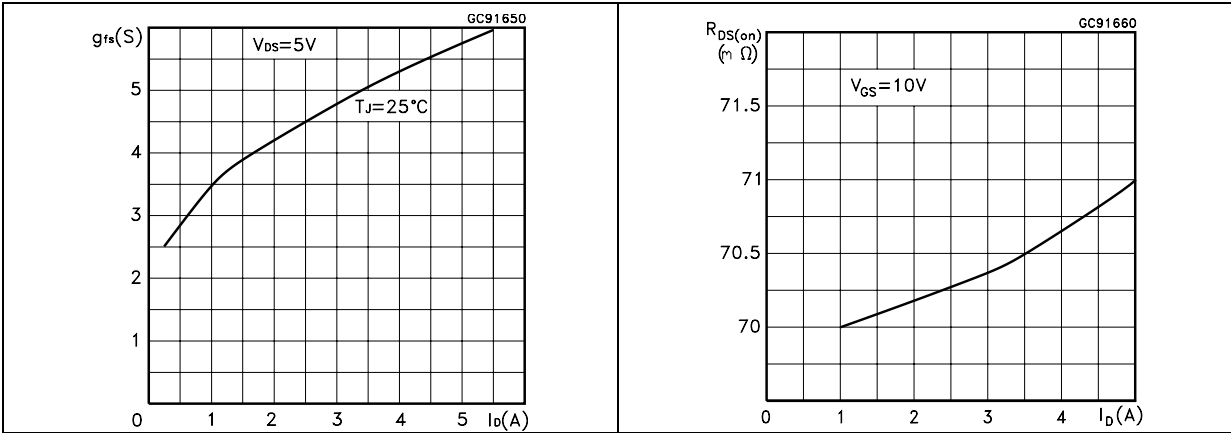


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized B_{VDS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

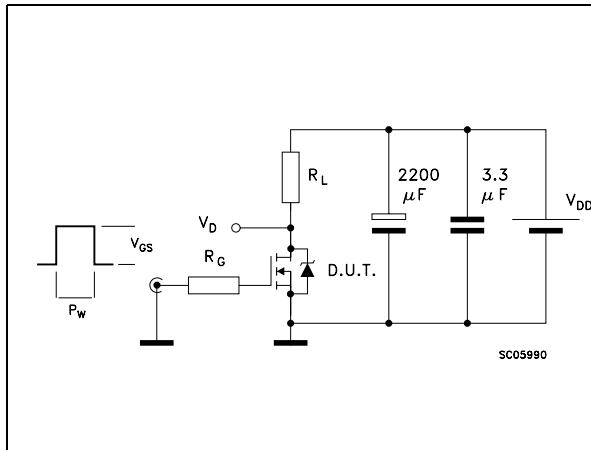


Figure 14. Gate charge test circuit

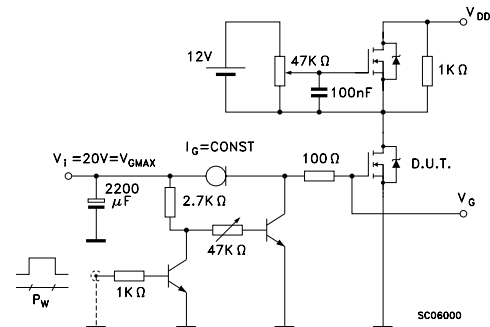


Figure 15. Test circuit for inductive load switching and diode recovery times

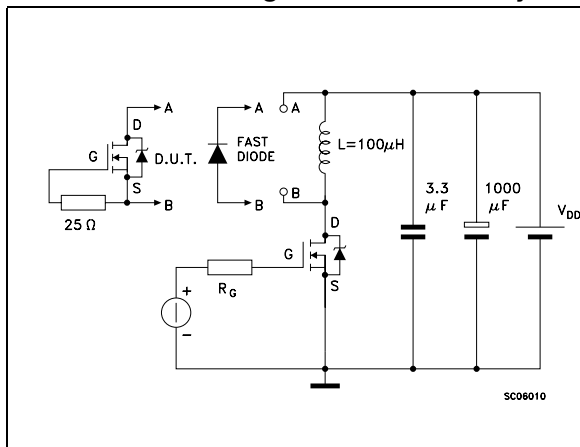


Figure 16. Unclamped Inductive load test circuit

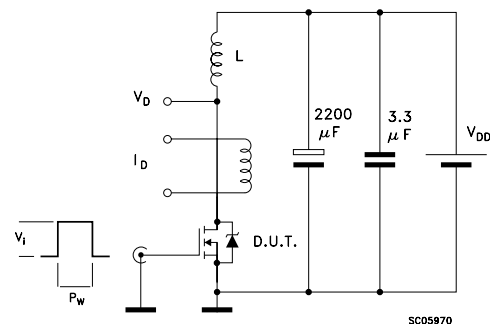


Figure 17. Unclamped inductive waveform

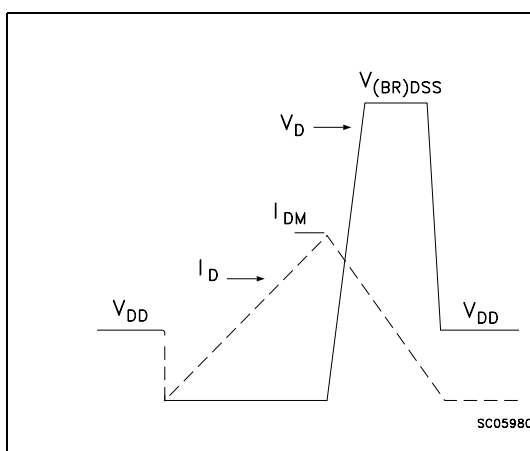
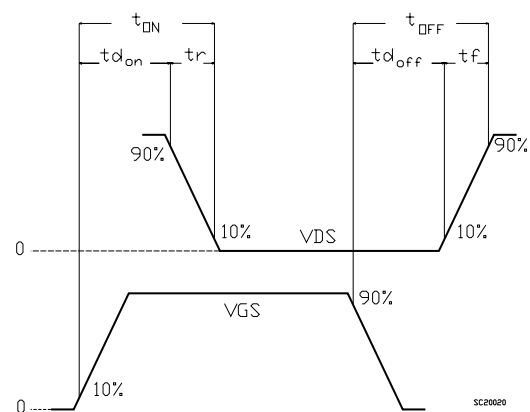


Figure 18. Switching time waveform

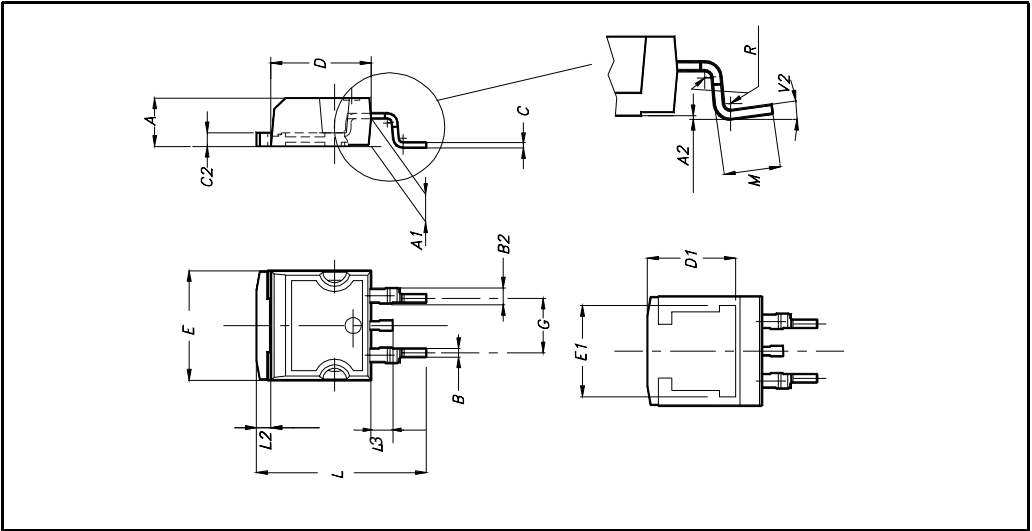


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

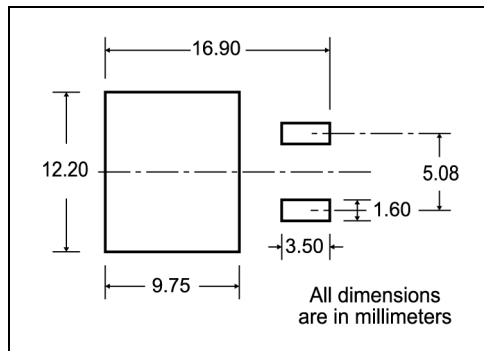
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

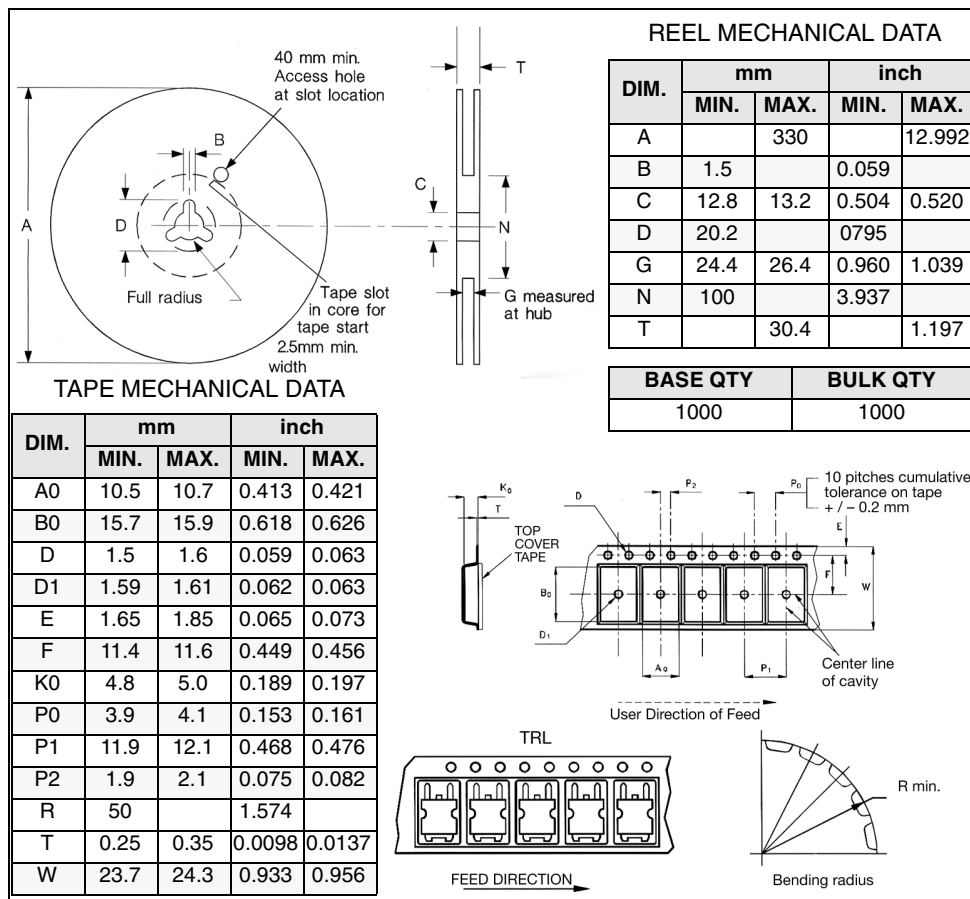


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2005	1	Preliminary document
19-Jun-2006	2	New template, no content change

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