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BCA6000ETL

Advance Information

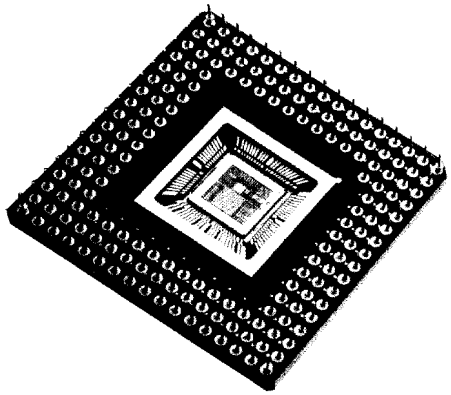
BCA6000ETL BiMOS ARRAY

This specification defines design and performance requirements for the BCA6000ETL, first in a new generation of high performance TTL, ECL, and CMOS-compatible BiMOS semicustom arrays. The BCA6000ETL is built with epitaxial NPN transistors using polysilicon, oxide walled emitters for the switching and current drive of bipolar combined with the use of silicon-gate CMOS having silicided source, drain and gate for characteristic MOSFET power dissipation and enhanced speed characteristics. The logic power of over 6000 equivalent 2-input NAND gates is available for VLSI applications.

- Logic Function Specified by User (Three Unique Masks)
- Interfaces CMOS, TTL, MECL 10K/10KH and ECL 100K
- Input Receiver Delays: — 1.0 ns Typ CMOS
  — 1.3 ns Typ TTL
  — 3.0 ns Typ ECL
- Output Driver Delays: — 3.0 ns Typ CMOS (@ 50 pF)
  — 3.5 ns Typ TTL (8.0 mA @ 50 pF)
  — 1.1 ns Typ ECL (50 Ω)
- Internal Gate Delay: — 0.8 ns Typ (2-input NAND)
- Flexible I/O Structure: ECL, TTL or CMOS
  Receivers, Drivers or Bidirectional
- Supported by Complete CAD Development System

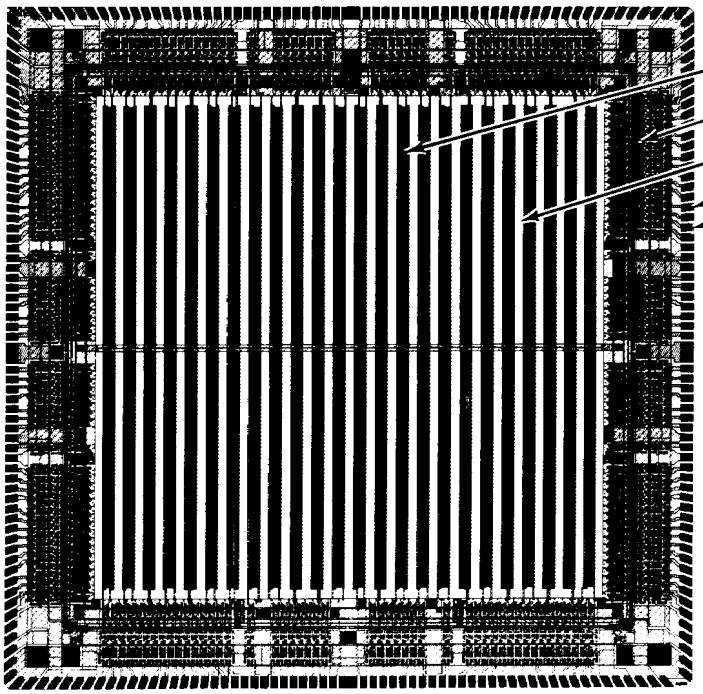
HIGH PERFORMANCE BiMOS
TTL-ECL-CMOS
COMPATIBLE

MACROCELL ARRAY



169-Pin
Pin Grid Array Package

FIGURE 1 — BCA6000ETL MACROCELL ARRAY LAYOUT



Package Options	I/O Pins
254 PGA	202*
224 PGA	178
193 PGA	148
169 PGA	130
132 PGA	102

*TAB bonding

ADI1392

PRODUCT DESCRIPTION

The BCA6000ETL Macrocell Array is an 800 picosecond, 6000 equivalent gate density semicustom array which combines the low power dissipation and packing density of 2-micron CMOS with the high drive and performance of oxide isolated 3-micron bipolar on the same silicon using Motorola's Low Voltage/High Speed BiMOS process. Basic features of the BCA6000ETL are listed in Table 1. The array is composed of two types of cells: Internal cells for logic realization and I/O (periphery) cells for array access and signal level translation. Macrocells are similar to standard logic integrated circuit packages. A library of macrocells provides a selection of over 70 fully specified logic functions (macros), similar to an IC data book. These macros take the form of standard logic elements such as D, JK, or T type flip flops, decoders, multiplexers or many other predefined functions.

The BiMOS macros utilize CMOS components to realize the needed logic, then employ a pair of bipolar transistors in a push-pull arrangement to provide the output drive for enhanced performance. The BCA6000ETL is made up of 3072 Internal cells each containing 10 NMOS, 5 PMOS and 2 bipolar NPN devices as shown in Figure 3. Figure 2 shows the advantage of BiMOS over conventional 2-micron CMOS under various loading conditions.

All signals coming onto or going off the array pass through an I/O cell. The I/O cells provide receiver, output driver, tri-state driver and bidirectional ports interfacing to CMOS, TTL or ECL external logic. CMOS ports have 2.5 volt input thresholds and outputs that drive rail to rail. ECL is provided in both true MECL 10KH, 100K levels (0 V to −5.2 V) and pseudo ECL level compatibility (+5.0 V to 0.0 V). TTL inputs are offered in "true" bipolar type, high impedance "MOS type," and "Schottky BiMOS type" to allow designers the choice of exact TTL thresholds, reduced input currents in high fan out circuits, or extremely fast propagation delays respectively. TTL outputs provide 8.0 to 24 mA of drive per single cell and 48 mA to 72 mA by paralleling two or three output cells together.

Over 1400 routing channels (582 first layer metal and 896 second layer metal) are available to interconnect macro functions and I/O pins. Power, ground and bias supply lines are not shown in Figure 1.

These interconnects are automatically accomplished by the CAD system. The illustration shows only the free channels that are used by the designer to interconnect the cells in the array. The channels in the horizontal direction are accomplished on second layer metal. Note that the second layer metal can be placed over the cell without interfering with the macro in that cell since all macros are interconnected on first layer metal. The second layer metal is separated from the first layer by a dielectric isolation. Metal runs on the chip have little effect on delay times because of the bipolar drive between macros. Connections between first and second layer metal are accomplished with VIAs. The interconnecting of cells on the array can be compared to routing lines on a two-sided PC board.

Motorola's MCA-CAD (Macrocell Array — Computer Aided Design) system is the engineering design interface between Motorola and customers developing LSI array circuits (MCA options). Customers can either use terminals at their own geographic location or access CAD software at a Motorola Regional CAD Design Center, in both cases, over phone lines or data comm network. The CAD software contains programs to assist in each stage of option design and to catch syntactical errors or design violations during the design procedure rather than at test.

FIGURE 2 — AVERAGE GATE DELAY versus LOADING

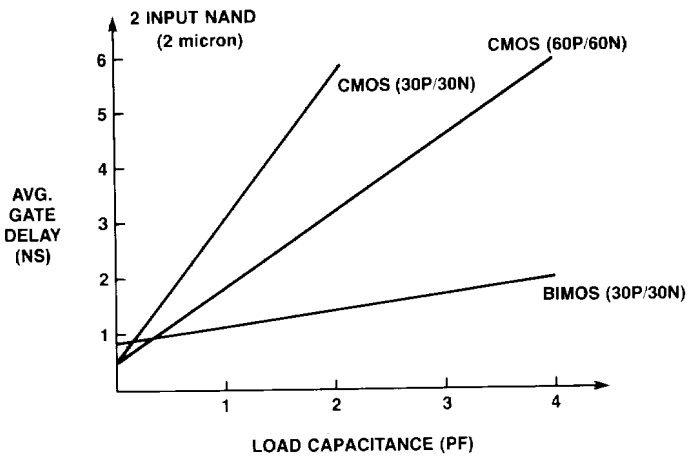


FIGURE 3 — BCA6000ETL INTERNAL CELL

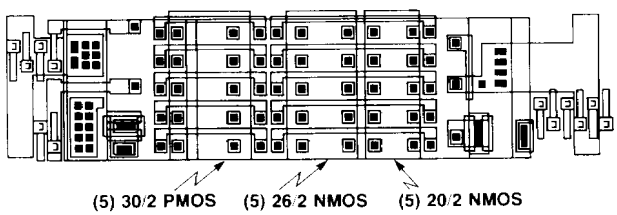


TABLE 1 — BASIC BCA6000ETL ARRAY FEATURES

1. Interfaces with all TTL-level-compatible logic; CMOS 2.5 V threshold logic; MECL 10K and 10KH logic and ECL 100K temperature compensated products.
2. 3274 total cells: 3072 Internal cells, 202 Input/Output (I/O) cells.
3. Logic density: 6144 equivalent 2-input NAND gates @ 2 gates per Internal cell up to 8192 equivalent gates if D flip-flops are used (8 gates per flop).
4. Die size: 396 mils x 396 mils.
5. AC Power dissipation: 1.7 watts typical @ 50 MHz — all TTL I/O.
   4.6 watts typical @ 50 MHz — mixed ECL/TTL mode.
6. Power per gate: 22 μW per MHz typical with 0.8 pF load.
7. Internal gate delay: 0.8 ns typical with Fan Out = 1 and no metal.
   1.1 ns typical with F.O. = 2 and 2 mm of metal.
8. CMOS Input buffer delay: 1.0 ns typical.
   TTL Input buffer delay: 1.3 ns typical.
   ECL Input buffer delay: 3.0 ns typical.
9. CMOS Output buffer delay: 3.0 ns typical (@ 50 pF).
   TTL Output buffer delay: 3.5 ns typical (sinking 8.0 mA @ 50 pF load).
   ECL Output buffer delay: 1.1 ns typical (50 ohms).
10. TTL Output drives up to 72 mA are available with multiple cells.
11. ECL edge speed: 0.4 ns minimum from 20 to 80% points.
12. Ambient temperature range: 0°C to 70°C.
13. Voltage compensated: −5.2 Vdc ± 5% (ECL); +5.0 Vdc ± 10% (TTL and CMOS)
14. Temperature compensated 100K ECL is also available: −4.5 Vdc ± 0.3 V
15. Ceramic 132, 169, 193, and 224 Pin-Grid Array packages.
16. Non hermetic glass epoxy 254 Pin-Grid Array packages.

CMOS DECODING WITH BIPOLAR PUSH-PULL DRIVE

The limitation on transistor device size required for efficient CMOS cell layout combined with the need to parallel or series connect devices when implementing various logic functions can result in large variations between rising and falling edge speeds and significant delay degradation when connected to normal interconnect loads. Motorola's BiMOS circuits are designed with bipolar push-pull devices which isolate the CMOS circuits from loading allowing the unit load degradation to be very small (275 ps per pF) and essentially the same for all circuit functions. The actual logic inherent in the macro is implemented with CMOS. To illustrate the mixture of bipolar with CMOS Figure 4 compares the implementation of a 2-input NAND in both CMOS and BiMOS technologies.

Macro functions more involved than simple combinatorial gates are implemented in the same manner, with the logic realized entirely in CMOS except for those logic segments that need to drive other macros. These segments incorporate the bipolar transistors necessary for enhanced drive, as well as the additional CMOS transistors that serve to enhance the switching speed of the bipolar outputs (similar to the enhancement seen in the 2-input NAND example). Figure 5 illustrates the logic diagram of a D flip-flop with asynchronous set and reset.

FIGURE 4 — CMOS/BiMOS 2-INPUT NAND COMPARISON

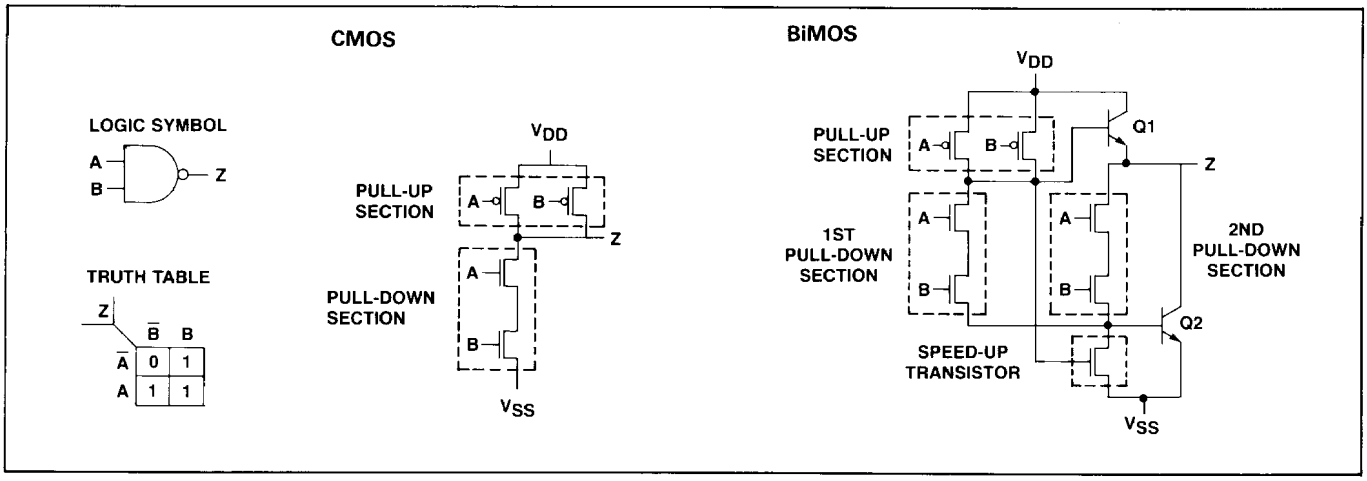
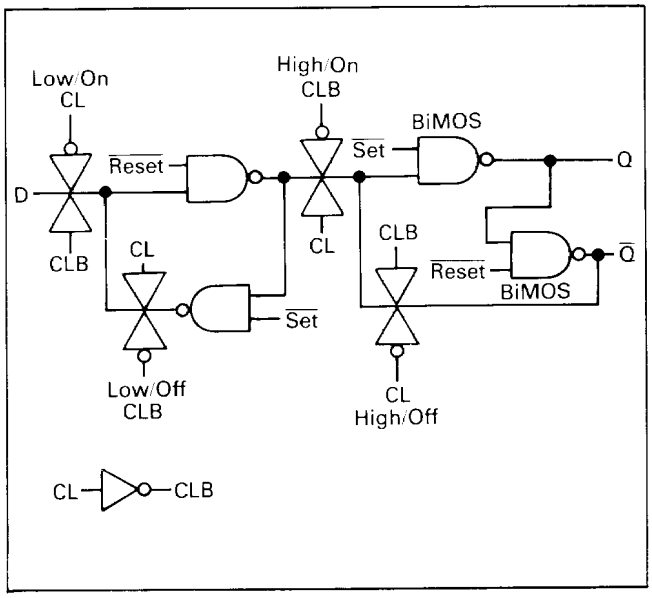


FIGURE 5 — D FLIP-FLOP WITH ASYNCHRONOUS SET AND RESET

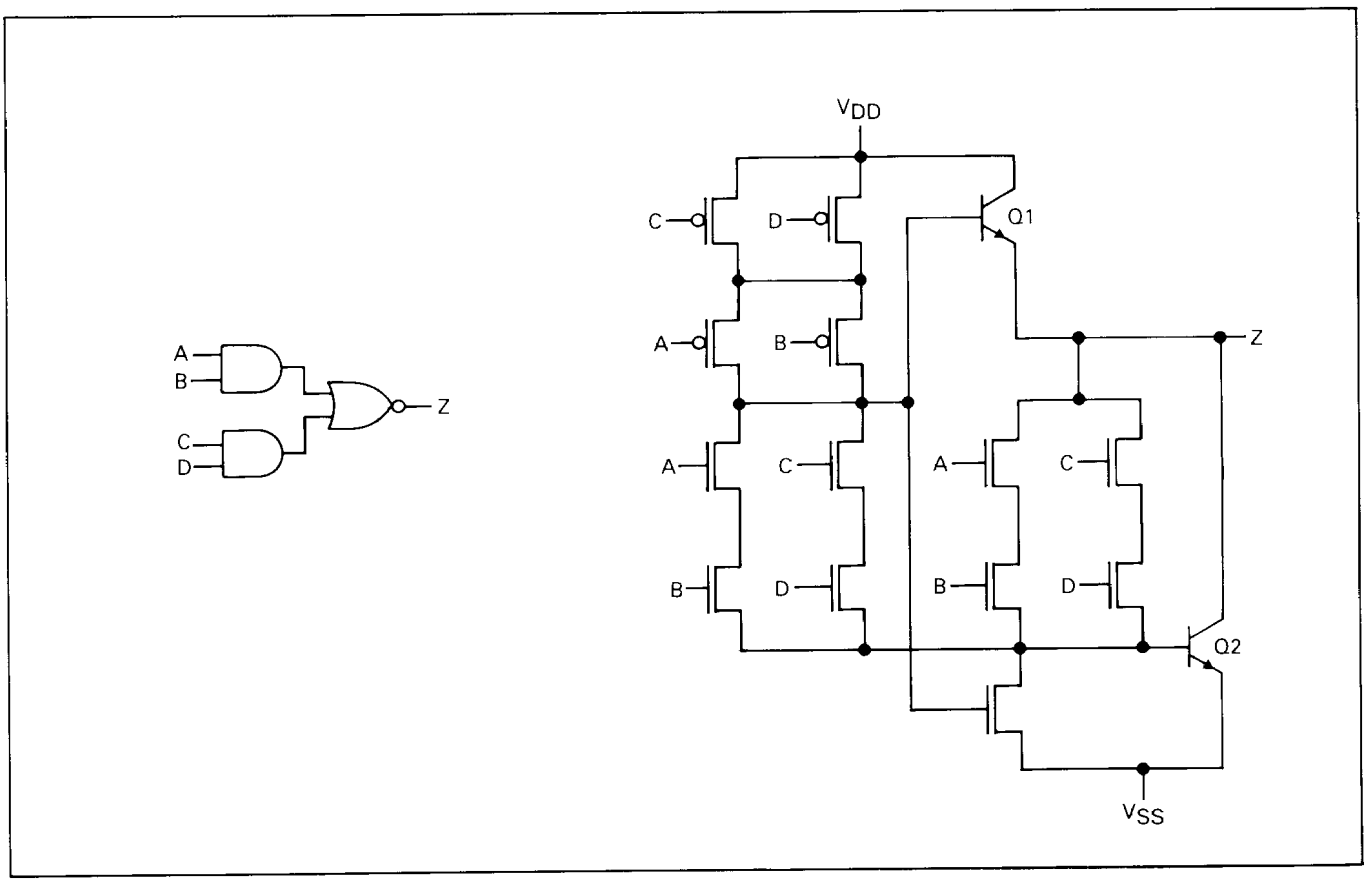


ROUTING CONSIDERATIONS

Automatic routing between macros is enhanced with the provision of at least two routing channels always available over each Internal cell to provide routing across the columns of Internal cells (256 "pass throughs"). If a macro is not implemented in a primary cell site, seven pass throughs become available. Implementation of a macro at an Internal cell site will consume between 1 and 5 pass through channels. Between the 24 columns of Internal cells there are 22 to 24 vertical routing tracks. The routing channels in the vertical direction, as well as macro internal connections, are accomplished on first layer metal, while the routing channels in the horizontal direction are accomplished on second layer metal. Note that the second layer metal can be placed over the cell without interfering with the macro in that cell since all macros are formed on first layer metal.

The efficient sizing of the Internal cell as well as efficiency of intramacro routing is substantiated by the fact that the majority of BiMOS library functions use more than 80% of the cell's transistors. One example of 100 percent utilization of the components is seen with function B002: 2-2ANDS into 2NOR (Figure 6).

FIGURE 6 — MACRO B002:
2 2-INPUT ANDS INTO 2-INPUT NOR



BiMOS PERFORMANCE COMPARISON

CMOS technology has been extensively investigated for applications in VLSI systems because of its low power consumption and high noise immunity. However, the limited drive capability of CMOS circuits degrades performance in VLSI systems where signals frequently must drive large parasitic capacitances. On the other hand, bipolar circuits can drive capacitive loads with much less speed degradation; but the large-scale integration of high performance bipolar circuits is limited by power dissipation. To achieve high performance in VLSI densities the two technologies were combined into BiMOS. Table (2) compares performance features of three array technologies offered by Motorola. All three (CMOS, Bipolar, BiMOS) are TTL compatible and incorporate similar 2-micron CMOS and oxide isolated bipolar processes. Each array has unique advantages for certain applications. Note that the degradation in performance of BiMOS per unit load is approximately 20% that of CMOS and identical to bipolar. In each of these technologies 250 mils of routing metal represents approximately 1.0 pF of load. The same 1.0 pF of load is also approximated by 8 inputs (Fan Out = 8) in BiMOS.

TABLE 2 — BCA6000ETL — MCA2900ETL — HCA62A50 ARRAY COMPARISONS

FEATURE	HCA62A50	MCA2900ETL	BCA6000ETL
Technology	CMOS	Bipolar	BiMOS
#Primary Cells	1656	130 Major, 72 ECL Output, 70 TTL I/O	3072
#Equivalent Gates	4968	2958	6144
I/O Cells			
# Input Only	—	30 TTL, 72 ECL	—
# Output Only	—	—	—
Max # Bidirectional	120 @ 4.0 mA	40 TTL, 48 ECL	202 TTL @ 8 mA; 32 ECL @ 50, 25 Ω
Max #Input or Output	120	40 TTL, 48 ECL	202
• I/O Compatibility	CMOS/TTL	TTL/ECL (10KH and 100K)	CMOS/TTL/ECL (10KH and 100K)
• Basic Gate Delay (Typical) and	1.8 ns	0.7 ns	0.8 ns
Delay Degradation per Unit Load	1610 ps/pF	275 ps/pF	275 ps/pF
• Input Buffer Delay (Typ)	3.7 ns @ 1.0 pF	1.1 ns TTL	1.3 ns TTL/1.0 ns CMOS
		ECL buffer not required	3.0 ns ECL
• Output Buffer Delay (Typ)	6.0 ns (4.0 mA @ 50 pF)	3.2 ns TTL (8.0 mA @ 50 pF)	3.5 ns CMOS (@ 50 pF)
		0.5 ns ECL (50 Ω @ 50 pF)	3.5 ns TTL (8.0 mA @ 50 pF)
			1.1 ns ECL (50 Ohms)
• Output Drive	4.0 to 24 mA	8.0 mA TTL	8.0 mA to 72 mA TTL
• I/O Switching Speed (Max)	25 MHz	250 MHz ECL or TTL IN	150 MHz TTL
		70 MHz TTL OUT	100 MHz ECL
		250 MHz ECL OUT	200 MHz CMOS
• Power	22 μW/MHz @ 0.6 pF	4.0 Watts Typ	22 μW/MHz @ 0.8 pF
• Die Size (Mils)	293 x 293	291 x 291	396 x 396

BiMOS AT MOTOROLA

BiMOS technology was first described in published literature in the late 1960's as more of a technical curiosity rather than a specific product announcement. The first product introductions were a series of op-amps (based on metal gate BiPMOS and BiCMOS technology), display drivers and then smart power products several years later.

An optimized BiMOS technology can approach ECL switching speed at a fraction of the power dissipation. Development of an acceptable BiMOS process requires resolving device trade-offs such as voltage, density, speed, and complexity versus yield. This results in various process technology considerations such as the starting material/epitaxy, isolation technique, extrinsic parasitics/profiles, and mask steps versus process steps. Because of the diversity of applications possible, a family of BiMOS technologies, rather than one, is necessary.

Motorola has developed three major categories of BiMOS technologies to address the different product needs of display drivers, regulators, and digital/analog VLSI circuits. These technologies can be classified as high voltage, medium voltage/power and low voltage/high speed. The low voltage/high speed process is the foundation for Motorola's new generation of BiMOS Macrocell Arrays.

LOW VOLTAGE/HIGH SPEED BiMOS PROCESS

Retaining the individual benefits of CMOS and advanced bipolar technologies when building both on the same silicon means minimizing compromises in each device's performance without unduly increasing process complexity. Motorola minimizes performance tradeoffs by merging critical process modules, and reconciles conflicting requirements by decoupling them with a minimum number of additional process steps. This is accomplished using a 2-micron "twin tub" CMOS process coupled to an N+ buried layer/P-Epi (Figure 7).

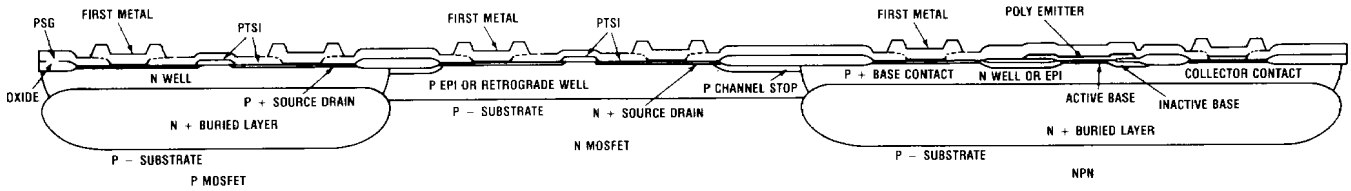
An N+ buried layer is used underneath the NPN transistors to enhance performance and below the PMOS to reduce latchup susceptibility. While the NMOS is built in the P-epi, an N-well is diffused into the N+ buried layer to serve as the foundation (tubs) for both PMOS and NPN transistors. A platinum silicide layer reduces the sheet resistance of the single-crystal and polysilicon regions, forming Schottky diodes in the lightly doped epitaxial regions. A two layer metallization with polyimide interlayer is employed. First and second layer metal uses a 4-micron and 5-micron pitch respectively.

Advanced bipolar performance is realized with a thin epitaxial NPN transistor fabricated by use of a very shallow polysilicon emitter, oxide-walled on all four sides. Silicided sources, drains, and gates are used to enhance MOSFET performance. Latchup is eliminated by combining the thin epi layer with a retrograde-type P-well, effectively shunting the parasitic well and substrate resistances that are major contributors to latchup.

CMOS I/O Compatibility

All inputs can be interfaced to CMOS logic levels with true CMOS 2.5 V thresholds. There are also high impedance "MOS Type" TTL inputs having TTL compatible thresholds of 1.5 volts. The MOS type TTL input is used when an off chip TTL signal needs to drive a large number of different array input pins. In addition to reduced loading the MOS type TTL input cells consume 0.1 mW

FIGURE 7 — CROSS SECTION OF LOW VOLTAGE/HIGH SPEED BiMOS PROCESS



- **2-MICRON "TWIN TUB" CMOS COUPLED TO N+ BURIED LAYER/P-EPI PROCESS**
- **OXIDE ISOLATED POLYSILICON EMITTER NPN BIPOLAR TRANSISTORS**
- **2-LAYER METAL WITH POLYIMIDE ISOLATION**

SPECIAL DESIGN FEATURES

Flexible I/O Structure

There are 202 cells around the periphery of the MCA6000ETL, each dedicated to providing an I/O link between a package pin and the internal logic of the chip. Each I/O cell may be personalized into a CMOS input or output or bidirectional, ECL input or output, or TTL input or output or bidirectional port (Figure 8). Up to 32 of these cells can be designated as either 25 or 50 ohm ECL cutoff, 25/50 ohm ECL bidirectional, or 24 mA TTL outputs. Any of the 202 cells can be designated as TTL 8.0 mA, totem pole or open collector, output or tri-state or bidirectional. All ECL inputs/outputs could be chosen as either 50 ohm 10KH or 100K. All TTL inputs can be selected as either "true" bipolar type, when existing TTL input characteristics are demanded, high-impedance MOS type when reduced currents are desired, or "Schottky BiMOS type" when a worst case propagation delay of only 1.5 ns is needed. The Output cells can also be selected as 48 mA, 64 mA or 72 mA drivers by paralleling adjacent cells internally and reducing the number of outputs accordingly.

All 202 I/O cells are accessible by use of a 254 pin grid array package (PGA). Smaller 132, 169, 193, and 224 PGA packages can be selected when not more than 102, 130, 148, and 178 signal lines are needed respectively. Maximum simultaneous switching limits are provided by implementing an Internal cell ground (V_{SS}) separate from a mixed ECL and TTL ground (V_{SSO}), and a TTL translator circuit supply (V_{DD}) separate from the TTL output only supply (V_{DDO}). Figure 9 illustrates the separation of power supply rails when ECL and TTL I/O are used (true mixed mode operation). TTL power pins for I/O cells are tied together at board level to a single +5.0 V supply. Simultaneous switching limits allow 8 outputs per side, 32 outputs in total, of any output choice, to switch simultaneously. It should be noted that while there are 202 potential drivers available, power and current density considerations set a realistic limit of 384 mA sink current on any one side of the array when the drivers are sinking current.

FIGURE 8 — BCA6000ETL I/O FLEXIBILITY

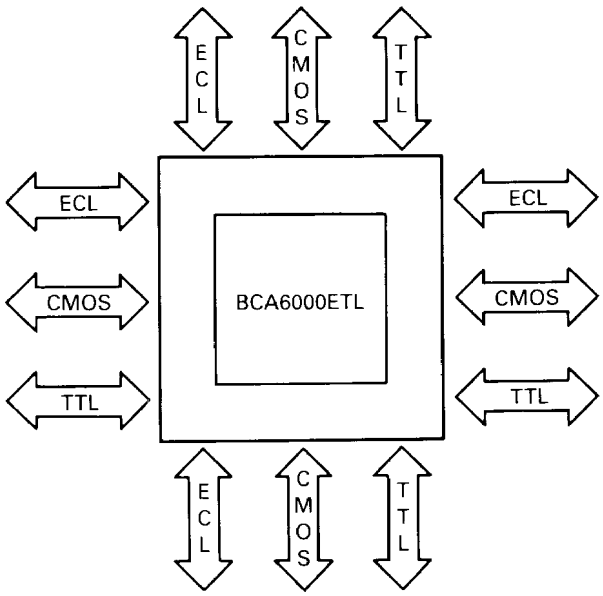
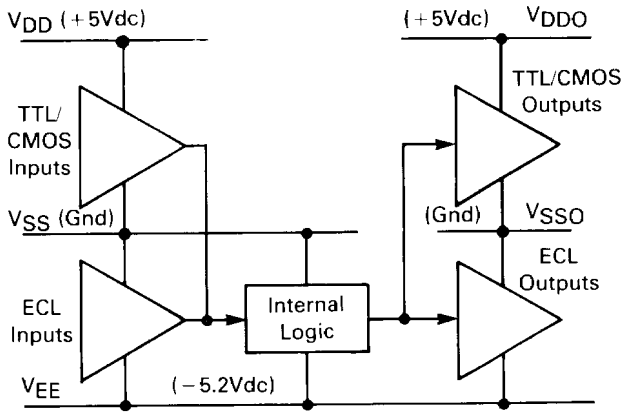


FIGURE 9 — EXAMPLE OF MIXED MODE POWER SUPPLY RAILS



of power compared to 4.0 mW for standard TTL. CMOS outputs provide increased noise margins by having LOW and HIGH levels equal to V_{SSO} and V_{DDO} levels.

High Drive TTL Outputs

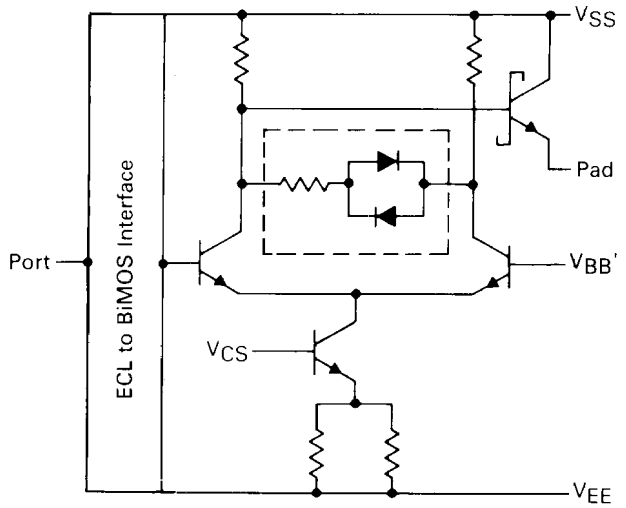
TTL outputs are available in output only, bidirectional, or tri-statable, open collector and active pull-up configurations. The normal sink current in these configurations is 8 mA or 24 mA. There is a restriction of 32 on the number of cells available for sinking 24 mA. Higher drives of 48 mA, 64 mA or 72 mA are obtained by paralleling output cells internal to the array. This reduces the number of output lines available on 254 pin packages but is not likely to present any limitation in smaller packages.

ECL 100K Option

The MCA6000ETL array is offered with an ECL 100K option that features approximately constant output levels over temperature.

This option is specified (standard ECL 100K specifications) with a guaranteed dc noise margin of 130 mV over ambient temperature variations of 0°–70°C and a $V_{EE} = -4.5 \pm 0.30$ volts. Figure 10 shows the temperature compensation network for 50 ohm outputs.

FIGURE 10 — ECL 100K OUTPUT TEMPERATURE COMPENSATION NETWORK



MACROCELL LIBRARY — Internal and I/O Cells

This chip consists of a combination of I/O cells (peripheral) and Internal cells as shown in Figure 1. Each cell contains a fixed array of unconnected transistors and resistors, and all Macrocell Array chips are built from a standard semiconductor diffusion set. That is, all chips are identical, and can be prefabricated up to the metallization step. The Macrocell Design Library contains over 70 logic functions called macros. A macro (sometimes called macrocell) is a first-layer metal interconnection pattern that interconnects the components (transistors and resistors) of a specific logic function. The CAD system contains the required first layer metallization pattern for each macro as well as the I/O ports.

Only the Internal cell can realize logic. The I/O cells serve only as appropriate logic level translation (input/output) configurations. One or more Internal cells are utilized to realize a chosen macro, depending on the complexity of the macro's logic. For example, a 4-input NAND would consume one Internal cell, whereas a D flip-flop would utilize two Internal cells. There are 3072 Internal cells available to the designer. A list of macrocell functions currently stored in the library is shown in Table 3.

Estimated worst case propagation delays are specified for $V_{DD} = 4.5$ Vdc, a maximum junction temperature of T_J max = 115°C, worst case input edge rates, and worst case processing. All outputs are loaded with a fan-out of 1 unit load. The estimated worst case setup, hold, and recovery times are also listed for all flip-flops and latches.

TABLE 3 — BCA6000ETL MACROCELL LIBRARY

Macro	Description
500 SERIES — I/O MACROS ECL AND TTL ENVIRONMENT	
B501	CMOS Input
B503	TTL Input (Bipolar Type)
B505	CMOS Output
B506	TTL 8 mA Output (Totem-Pole)
B507	CMOS Output, Tristate
B508	TTL 8 mA Output, Tristate (Totem-Pole)
B509	CMOS Bidirectional (CMOS Input, CMOS Output)
B511	TTL Bidirectional, 8 mA (Bipolar Type Input, Totem-Pole)
B513	CMOS Output (Open-Drain)
B514	TTL 8 mA Output (Open-Coll.)
B515	CMOS Output, Tristate (Open-Drain)
B516	TTL 8 mA Output, Tristate (Open-Coll.)
B517	CMOS Bidirectional (CMOS Input, CMOS Open-Drain)
B519	TTL Bidirectional, 8 mA (Bipolar Type Input, Open-Coll.)
B522	TTL 24 mA Output (Totem-Pole)
B524	TTL 24 mA Output, Tristate (Totem-Pole)
B527	TTL Bidirectional, 24 mA (Bipolar Type Input, Totem-Pole)
B530	TTL 24 mA Output (Open-Coll.)
B532	TTL 24 mA Output, Tristate (Open-Coll.)
B535	TTL Bidirectional, 24 mA (Bipolar Type Input, Open-Coll.)
B537	ECL Input (True)
B538	ECL Output, 50 Ohms, 10K (True)
B539	ECL Output, 50 Ohms, 100K (True)
B540	ECL Output, 25 Ohms, Cutoff (True)
B541	ECL Output, 50 Ohms, Cutoff (True)
B542	ECL Bidirectional Output, 25 Ohms (True)
B543	ECL Bidirectional Output, 50 Ohms (True)
700 SERIES — I/O MACROS TTL ONLY ENVIRONMENT	
B701	CMOS Input
B702	TTL Input (Schottky BiMOS Type)
B703	TTL Input (Bipolar Type)
B704	TTL Input (MOS Type)
B705	CMOS Output
B706	TTL 8 mA Output (Totem-Pole)
B707	CMOS Output, Tristate
B708	TTL 8 mA Output, Tristate (Totem-Pole)

TABLE 3 — BCA6000ETL MACROCELL LIBRARY (Continued)

Macro	Description
700 SERIES — I/O MACROS TTL ONLY ENVIRONMENT (Cont'd.)	
B709	CMOS Bidirectional (CMOS Input, CMOS Output)
B710	TTL Bidirectional, 8 mA (Schottky BiMOS Input, Totem-Pole)
B711	TTL Bidirectional, 8 mA (Bipolar Type Input, Totem-Pole)
B712	TTL Bidirectional, 8 mA (MOS Input, Totem-Pole)
B713	CMOS Output (Open-Drain)
B714	TTL 8 mA Output (Open-Coll.)
B715	CMOS Output, Tristate (Open-Drain)
B716	TTL 8 mA Output, Tristate (Open-Coll.)
B717	CMOS Bidirectional (CMOS Input, CMOS Open-Drain)
B718	TTL Bidirectional, 8 mA (Schottky BiMOS Input, Open-Coll.)
B719	TTL Bidirectional, 8 mA (Bipolar Type Input, Open-Coll.)
B720	TTL Bidirectional, 8 mA (MOS Input, Open-Coll.)
B722	TTL 24 mA Output (Totem-Pole)
B724	TTL 24 mA Ouput, Tristate (Totem-Pole)
B726	TTL Bidirectional, 24 mA (Schottky BiMOS Input, Totem-Pole)
B727	TTL Bidirectional, 24 mA (Bipolar Type Input, Totem-Pole)
B728	TTL Bidirectional, 24 mA (MOS Type Input, Totem-Pole)
B730	TTL 24 mA Output (Open-Coll.)
B732	TTL 24 mA Output, Tristate (Open-Coll.)
B734	TTL Bidirectional, 24 mA (Schottky BiMOS Input, Open-Coll.)
B735	TTL Bidirectional, 24 mA (Bipolar Type Input, Open-Coll.)
B736	TTL Bidirectional, 24 mA (MOS Type Input, Open-Coll.)
B737	ECL Input (Pseudo)
B738	ECL Output, 50 Ohms, 10K (Pseudo)
B739	ECL Ouput, 50 Ohms, 100K (Pseudo)
INTERNAL CELL MACROS	
B001	2AND into 3NOR
B002	2 2ANDS into 2NOR
B003	2OR into 3NAND
B004	2 2ORS into 2NAND
B005	Inverting 2 or 3 Majority
B006	2AND into 2NOR
B007	2OR into 2NAND
B008	Exclusive 2NOR
B009	3-Input Exclusive NOR
B010	Exclusive 2OR
B011	2AND, 2NOR into 2NOR
B012	3-Input Exclusive OR
B013	2OR, 2NAND into 2NAND
B014	Single Inverter
B015	2NAND
B016	3NAND
B017	4NAND
B018	6NAND
B019	8NAND
B020	2NOR
B021	3NOR
B022	4NOR

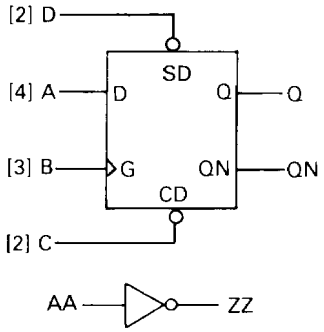
Macro	Description
INTERNAL CELL MACROS	
B023	6NOR
B024	8NOR
B025	Tristate Internal Buffer
B026	Inverting Tristate Internal Buffer
B027	Inverting Power Buffer
B028	Inverting Clock Driver
B030	D-Latch Gated
B031	D-Latch Gated (Gate Active Low)
B032	D-Latch Gated, Clear Direct (Gate Active High)
B033	D-Latch Gated, Clear Direct (Gate Active Low)
B034	SR-Latch with Separate Gated Inputs, SD, RD
B035	SR-Latch with Common Gated Inputs, SD, RD
B036	D-Latch with Scan Test Inputs (LSSD)
B037	D-Latch into D-Latch with Scan Inputs (LSSD)
B039	DFF
B040	DFF with Scan Test Inputs
B041	DFF with Clear Direct
B042	DFF with Scan Test Inputs, Clear Direct
B043	DFF with Clear Direct and Added Tristate Output
B044	DFF with Clear Direct, Set Direct
B045	DFF with Scan Test Inputs Clear Direct, Set Direct
B046	DFF with Set Direct
B047	DFF with Scan Test Inputs, Set Direct
B048	DFF without Buffered Clocks
B049	DFF without Buffered Clocks, with Scan Test Inputs
B050	DFF without Buffered Clocks, with Clear Direct
B051	DFF without Buffered Clocks, with Scan Test Inputs, Clear Direct
B052	DFF without Buffered Clocks, with Clear Direct, Set Direct
B053	DFF without Buffered Clocks, with Scan Test Inputs, Clear Direct, Set Direct
B054	DFF without Buffered Clocks, with Set Direct
B055	DFF without Buffered Clocks, with Scan Test Inputs, Set Direct
B057	JKFF
B058	JKFF with Scan Test Inputs
B059	JKFF with Clear Direct
B060	JKFF with Scan Test Inputs, Clear Direct
B061	JKFF with Clear Direct, Set Direct
B062	JKFF with Scan Test Inputs, Clear Direct, Set Direct
B063	Toggle FF without Buffered Clocks, with Clear Direct
B064	Toggle Flip-Flop without Buffered Clocks, with Clear Direct, Set Direct
B065	Toggle Flip-Flop without Buffered Clocks, with Set Direct
B066	Inverting Gate Multiplexer
B067	1 to 2 Transmission Gate Multiplexer, Inverting Output
B068	4 Bit Inverting MUX
B069	8 Bit Inverting MUX
B071	Half Adder
B072	Full Adder
B073	2 Bit Magnitude Comparator
B074	Two Phase Clock Generator, Unbuffered, Hi Underlap Hi Drive
B075	Two Phase Clock Generator, Unbuffered, Lo Underlap Hi Drive

FIGURE 11 — EXAMPLES OF INTERNAL CELL MACROS

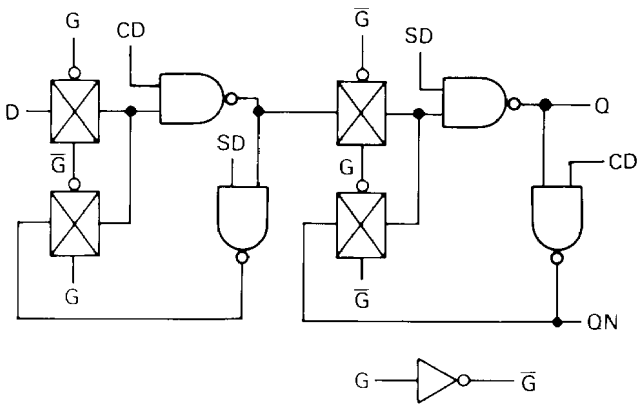
*Nanoseconds per Unit Load; **Nanoseconds per transition; ***Refer to B014 for full inverter specifications
Numbers in [ ] represent Input Loads e.g. [2] is 2 unit loads; absence of number implies an Input Load value of 1.

B044 — 4 INTERNAL CELLS
DFF WITH CLEAR DIRECT,
SET DIRECT (plus Inverter***)

$SUBU
Q QN ZZ / A B C D AA



LOGIC EQUIVALENT



	Min CD/SD Pulse Width	
	G = 0	G = 1
B044	4.3 ns	3.9 ns

	t_{pd} (CD → ↓ Q)		t_{pd} (CD → ↑ Q)	CD Recovery
	G = 0	G = 1		
B044	5.4 ns	7.0 ns	3.2 ns	1.6 ns

	t_{pd} (SD → ↑ Q)	t_{pd} (SD → ↓ QN)	SD Recovery
B044	3.2 ns	4.9 ns	0 ns

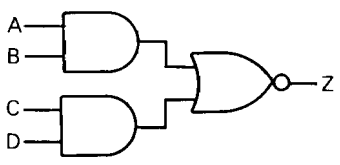
	WORST CASE											
	B → Q				B → QN							
	FO = 1		Fan-out Factor*		FO = 1		Fan-out Factor*					
	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	Set-up Time	Hold Time	Min Neg. Clock p.w.	Min Pos. Clock p.w.
B044	2.7 ns	3.4 ns	0.028	0.048	5.0 ns	3.9 ns	0.038	0.032	2.5 ns	1.4 ns	3.9 ns	4.3 ns

MAX FREQUENCY = 1/4.2 ns / EE

B002 — 1 INTERNAL CELL
2 2ANDS INTO 2NOR

$SUBU
Z / A B C D

LOGIC EQUIVALENT



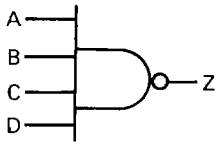
WORST CASE				Output Edge Rate**	
FO = 1		Fan-out Factor*			
t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}
4.6 ns	1.4 ns	0.041	0.029	9.0	5.0

$Z = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$

B017 — 1 INTERNAL CELL
4NAND

$SUBU
Z / A B C D

LOGIC EQUIVALENT



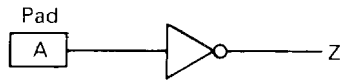
WORST CASE				Output Edge Rate**	
FO = 1		Fan-out Factor*			
t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}
2.8 ns	1.8 ns	0.031	0.040	4.0	5.0

$Z = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

FIGURE 12 — EXAMPLES OF INPUT/OUTPUT CELL MACROS

B703 — 1 I/O Cell
TTL Input (Bipolar Type)

$SUBU
Z / A

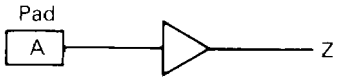


Worst Case			
FO = 1		Fan-out Factor*	
t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}
5.7 ns	3.6 ns	0.024	0.090

P_D = 5.0 mW (DC power ≐ AC power)

B704 — 1 I/O Cell
TTL Input (MOS Type)

$SUBU
Z / A

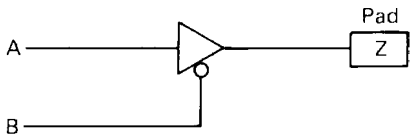


Worst Case			
FO = 1		Fan-out Factor*	
t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}
7.4 ns	7.0 ns	0.046	0.060

DC Power = 0.9 mW
AC Power = 54 μW/MHz

B708 — 1 I/O Cell
TTL 8 mA Output, Tri-State (Totem-Pole)

$SUBU
Z / A B



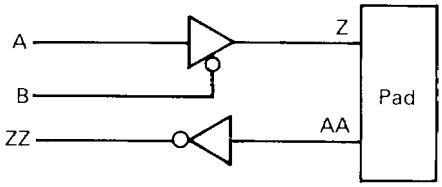
	Worst Case	
	t_{PLH}	t_{PHL}
50 pF	5.4 ns	8.3 ns
100 pF	6.6 ns	10.5 ns

t_{PLZ} = 4.4 ns t_{PHZ} = 11.5 ns
t_{PZL} = 10.9 ns t_{PZH} = 4.6 ns

P_D = 7.0 mW (DC power ≐ AC power)

B711 — 1 I/O Cell
TTL Bidirectional, 8 mA
(Bipolar Type Input, Totem-Pole)

$SUBU
Z ZZ / A B AA

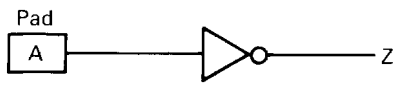


	Worst Case			
	FO = 1		Fan-out Factor*	
	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}
AA to ZZ	5.7 ns	3.6 ns	0.024	0.090
A to Z, 50 pF	6.1 ns	9.0 ns	—	—
A to Z, 100 pF	7.4 ns	11.3 ns	—	—

P_D = 12 mW (DC power ≐ AC power)

B537 — 1 I/O Cell
ECL Input

$SUBU
Z / A

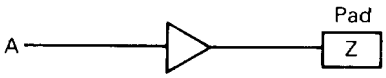


Worst Case	
t_{PHL}	t_{PLH}
6.9 ns	6.2 ns

P_D = 4.0 mW

B540 — 1 I/O Cell
ECL Output 25 Ohm Cutoff

$SUBU
Z / A



Worst Case	
t_{PHL}	t_{PLH}
1.5 ns	0.72 ns

P_D = 65 mW

DEVELOPMENT INTERFACE SYSTEM

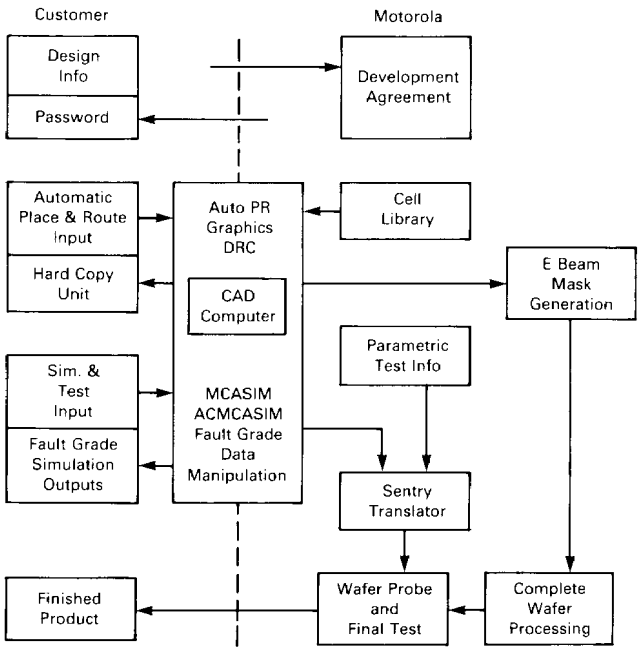
To develop a BCA6000ETL circuit, a designer first determines the logic function to be performed by each LSI circuit. Then, using remote terminals, he defines the logic to Motorola's Western Area Computer Center in Arizona. Computer programs simplify circuit design by simulating the design logic function, placing macros within the array, and automatically routing signals between the Macrocells and to the I/O package pins.

Successful implementation of a major array program such as the BCA6000ETL depends on a CAD system that accepts user design information, helps verify design accuracy and converts user data into a format compatible with semiconductor mask-making and test equipment. The Motorola CAD system accomplishes these objectives. Its data input format is easily understood and requires no special computer programming knowledge.

CAD Design Features

The CAD system can handle all design functions associated with semiconductor products, including the selection of first or second layer metal, metal widths and spacing, metal internal to Macrocells and power distribution. Macrocell Array designers use skills common to printed circuit board design, yet, with help from the CAD system, convert the equivalent of a small pc board full of SSI/MSI circuits to a high-performance custom LSI Macrocell Array device.

FIGURE 13 — MACROCELL ARRAY OPTION DEVELOPMENT FLOW



Customer	Motorola
1. Defines the circuit function. 2. Selects desired macrocells from the Motorola library. 3. Generates metal interconnect pattern on CAD. 4. Generates the test sequence on CAD.	1. Defines the Macrocell Array. 2. Designs and controls diffusion masks. 3. Develops Macrocell Array. 4. Provides CAD System to help design options. 5. Processes the circuits. 6. Tests the final product.

To help with this process, the Macrocell Array CAD system provides the following design features:

- MCASIM functional simulation
- Error checking of data input
- Fault grading to identify any untested nodes
- Auto place and route software
- AC performance simulation to verify input to output propagation delay or performance of internal paths
- Auto definition of longest delay path between selected input and output points
- CAD data base conversion to electron beam exposure mask generation
- CAD generation of Development/Production test programs
- Customer documentation for every design
- Automatic archiving of verified designs

Hardware

Macrocell array CAD software resides on IBM-compatible computer systems located in Scottsdale, Arizona at the Motorola Western Area Computer Center (WACC). CAD software is available to macrocell array customers on a time-share basis over normal telephone lines or datacomm network at 300 or 1200 baud data rates.

Recommended interface equipment:

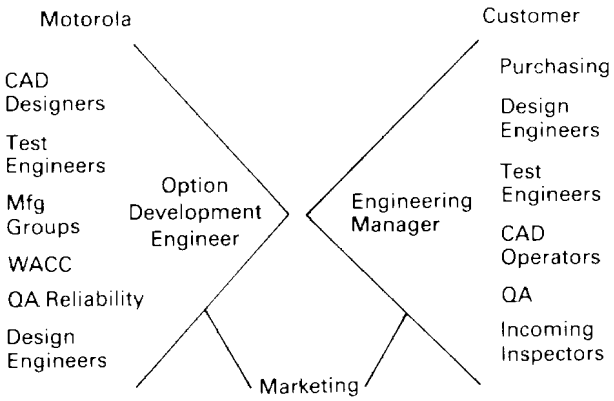
1. Tektronix 4109, 4112, 4113, 4115 or equivalent computer display terminal
2. Tektronix 4662 or 4663 interactive digital plotter (Optional)
3. 300- to 4800-baud modem
4. TTY-compatible keyboard/printer terminal
5. As a supplement to the above, engineering work stations (EWS) are available from Daisy, Mentor and others. They have a comprehensive set of software tools for Macrocell Array design using high resolution color monitors, 1-to-4 Megabytes of RAM, a 30-to-50 Megabyte Winchester hard disk, and one or two floppy disks.

The appropriate CAD interface hardware is also available through Motorola Regional CAD Service Centers.

Program Management

Upon completion of a three-day training course, each customer is assigned an option development engineer to focus all technical communications during design development. The option development engineer serves as both engineer and administrator to assure on-time shipment of fully tested prototypes.

FIGURE 14 — MACROCELL ARRAY PROGRAM MANAGER CONCEPT



Packaging

The BCA6000ETL macrocell array is offered in either the 132, 169, 193, 224, or 254 pin grid array package. Figure 15 illustrates the 169-pin grid array. The 254 pin package is non-hermetic FR4 glass epoxy construction with tape automated bonding. All others are conventional multi-layer ceramic.

The 169 PGA package has 130 I/O pins, 10 negative supply pins, 8 positive supply pins, 20 Gnd pins, and one orientation pin. All contacts are positioned in a uniform rectangular grid on 100 mil centers. Standoffs in each corner provide a 0.05 inch clearance between the PC board and the package surface. The macrocell array chip is die-attached to the (ceramic) package using a silver-glass paste which provides a better thermal coupling between the die and the ceramic than otherwise achieved using the traditional eutectic gold-silicon preforms. Hermeticity is provided with a solder-sealed Kovar lid.

The 169 PGA package is constructed with separate power and signal metallization layers to minimize lead resistance and inductance. This scheme allows multiple off-chip drivers to switch simultaneously without creating excessive inductive noise. The die is mounted in a cavity with circuit surface facing the PC board. This configuration provides a primary heat conducting surface facing away from the board which is ideally suited to conventional air-cooled environments when a heat sink is incorporated. Power dissipation within the BCA6000ETL array is highly dependent upon the choice of I/O configuration as well as the number of outputs driving current at any given time. A typical design having an I/O ratio of 2:1 or greater and incorporating an equal mix of TTL and ECL will dissipate less than 4.0 watts and not require a blown air environment. Application of a nominal heat sink will improve reliability in most instances. Similar configurations operated in an all TTL mode will not require either a heat sink or forced air to remain within 115°C max junction temperature.

TABLE 4 — I/O TRANSLATOR ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Unit	Value
Supply Voltage (V_{CC} = 0) For −4.5 V 100K option	V_{EE}	−4.5 ± 0.3	Vdc
Supply Voltage (V_{CC} = 0) For −5.2 V 10KH option	V_{EE}	−5.2 ± 5%	Vdc
Supply Voltage (V_{SS} = 0) For +5.0 V TTL and CMOS options	V_{DD}	+4.50 to +5.50	Vdc
Operating Temperature With Heat Sink and 750 lfm (ac and dc)	T_A	0 to +70	°C
Maximum Junction Temperature (Functional)	T_J	+130	°C
Maximum Junction Temperature (For ac and dc Specifications)	T_j	+115	°C
Maximum Clock Input Rise and Fall Times (20 to 80%) ECL	t_r, t_f	10	ns
Maximum Clock Input Rise and Fall Times (20 to 80%) TTL and CMOS	t_r, t_f	15	ns

ECL DC ELECTRICAL CHARACTERISTICS

Input Forcing Voltages	Parameter	MECL 10KH Compatible Spec Limits (1) Ambient Temperature 0°C	25°C	70°C	ECL 100K Compatible Spec Limits (1) Ambient Temperature 0 to 70°C	Unit
V_{IH} Max and V_{IL} Min	V_{OH} Max	−0.840	−0.810	−0.740	−0.880[4]	Vdc
	V_{OH} Min	−1.000	−0.960	−0.900	−1.025	Vdc
	V_{OL} Max	−1.650	−1.650	−1.620	−1.620	Vdc
	V_{OL} Max[2]	−1.950	−1.950	−1.950	−1.950	
	V_{OL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{OL} Min[2]	−2.020	−2.020	−2.020	−2.020	

ECL DC ELECTRICAL CHARACTERISTICS — continued

Input Forcing Voltages	Parameter	MECL 10KH Compatible Spec Limits (1) Ambient Temperature 0°C	25°C	70°C	ECL 100K Compatible Spec Limits (1) Ambient Temperature 0 to 70°C	Unit
V_{IHA} Min and V_{ILA} Max	V_{OHA} Min	−1.020	−0.980	−0.920	−1.035	Vdc
	V_{OLA} Max	−1.630	−1.630	−1.600	−1.610	Vdc
	V_{OLA} Max[2]	−1.950	−1.950	−1.950	−1.950	Vdc
V_{IH} Max	I_{INH} Max[3]	25	25	25	25	μA
	I_{INH} Max[5]	150	150	150	150	
V_{IL} Min	I_{INL} Min[6]	0.5	0.5	0.5	0.5	μA
Input Voltage Values	V_{IH} Max	−0.840	−0.810	−0.730	−0.880	Vdc
	V_{IL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{IHA} Min	−1.170	−1.130	−1.070	−1.165	Vdc
	V_{ILA} Max	−1.480	−1.480	−1.450	−1.475	Vdc

NOTES:
1. DC test limits are specified after thermal equilibrium has been established. V_{EE} = −4.5 V ± 0.3 V for the 100K or 10KH 4.5 V option. V_{EE} = −5.2 V ± 5% for the 10KH 5.2 V option. All outputs are loaded with 50 Ω to −2.0 V except the 25 Ω drivers which are loaded with 25 Ω to −2.0 V.
2. These voltage limits are for the driver output of macros with V_{OL} in the cutoff mode.
3. Per input fan-in.
4. For output macros B540 and B541, 25 ohm drivers, V_{OH} Max = −0.740 Vdc.
5. For input pulldown (≈ 50 kΩ).
6. Measured because input pulldown is always used.

CMOS DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}; TJmax: 0°C to +115°C)

Symbol	Parameter	Test Conditions	V_{DD}	25°C Typical	0°C to +70°C Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage, CMOS Input	NA	4.5	2.4	3.15	V
			5.5	2.9	3.85	
	Minimum High-Level Input Voltage MOS Type TTL Input	NA	4.5	1.6	2.0	
			5.5	1.6	2.0	
V_{IL}	Maximum Low-Level Input Voltage, CMOS Input	NA	4.5	1.8	1.35	V
			5.5	2.2	1.65	
	Maximum Low-Level Input Voltage MOS Type TTL Input	NA	4.5	1.2	0.8	
			5.5	1.2	0.8	
V_{OH}	Minimum High-Level Output Voltage, CMOS Output	I_{out} = −20 μA	4.5	4.499	4.4	V
			5.5	5.499	5.4	
V_{OL}	Maximum Low-Level Output Voltage, CMOS Output	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	4.5	0.001	0.1	V
			5.5	0.001	0.1	
I_{in} (CMOS Input)	Maximum Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	5.5	—	±10	μA
	Maximum Input Current, Pull-Down Resistor	V_{in} = V_{DD}	4.5	—	120	
			5.5	—	150	
I_{OZ} (CNOS Output)	Maximum Output Leakage Current, Three-State Output	Output = High Impedance V_{out} = V_{DD} or V_{SS}	5.5	—	±20	μA
	Maximum Output Leakage Current, Open Drain Output	Output = High Impedance V_{out} = V_{DD}	5.5	—	±20	
C_{in}	Maximum Input Capacitance		—	—	10	pF
C_{out}	Maximum Output Capacitance	Output = High Impedance	—	—	15	pF

BIPOLAR TYPE TTL DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter		LIMITS Min	Typ	Max	Units	Test Conditions	
V_{OH}*	Output High Voltage	8.0 mA Outputs	2.7	3.5	—	V	I_{OH} = −400 μA	V_{CC} = Min
V_{OH}*	Output High Voltage	24 mA Outputs	2.4	3.1	—	V	I_{OH} = −2.6 mA	V_{CC} = Min
I_{CEX}	Output Leakage Current for Open Collector Outputs				100	μA	V_{CC} = Min, V_{IN} = 5.25 V	
V_{OL}	Output Low Voltage	8.0 mA Outputs	—	0.35	0.50	V	I_{OL} = 8.0 mA	V_{CC} = Min
		24 mA Outputs	—	0.35	0.50	V	I_{OL} = 24 mA	V_{CC} = Min
V_{IH}	Input High Voltage		2.0	—	—	V		
V_{IL}	Input Low Voltage		—	—	0.80	V		
I_{IH}**	Input High Current		—	—	20	μA	V_{CC} = Max, V_{IN} = 2.4 V	
I_{IL}**	Input Low Current		—	—	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{OZH}*	Output Off Current High		—	—	20	μA	V_{CC} = Max, V_{OUT} = 2.4 V	
I_{OZL}*	Output Off Current Low		—	—	−20	μA	V_{CC} = Max, V_{OUT} = 0.4 V	
I_{OS}***	Output Short Circuit Current		−15	—	−130	mA	8.0 mA Driver	V_{CC} = Max, V_{OUT} = 0

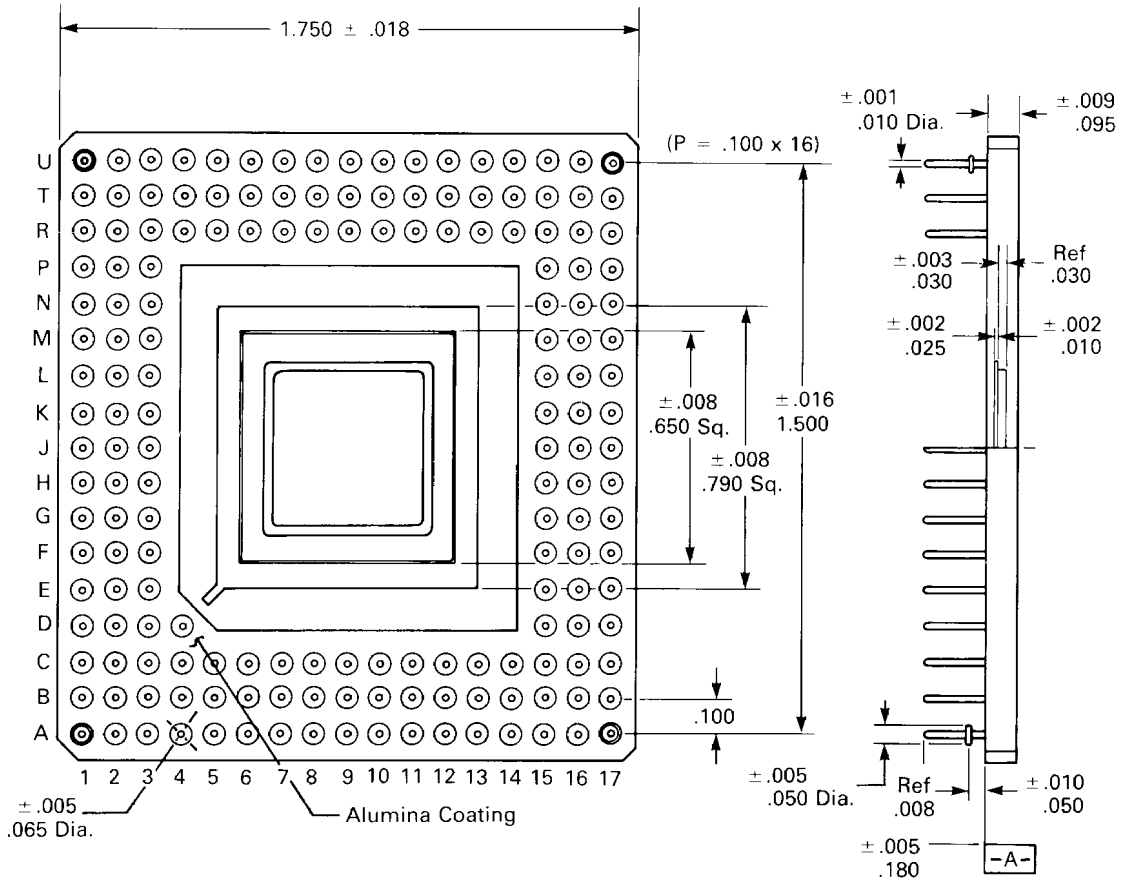
*Not applicable to open collector outputs.
**Current Per Input.
***Not more than one output should be shorted at a time. Output should not be shorted for more than one second.

SCHOTTKY BiMOS TYPE TTL DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	V_{CC}	25°C Typical	Guaranteed Limit	Unit
V_{IH} (Schottky BiMOS (Input)						V
	Minimum High-Level Input Voltage, TTL Input	NA	4.5	1.6	1.9	
			5.5	1.6	1.9	
V_{IL} (Schottky BiMOS (Input)						V
	Minimum Low-Level Input Voltage, TTL Input	NA	4.5	1.2	1.1	
			5.5	1.2	1.1	
C_{in}	Maximum Input Capacitance		—	—	10	pF
I_{IH}**	Input High Current	V_{CC} = MAX, V_{IN} = 2.4V	5.5	—	20	μA
I_{IL}**	Input Low Current	V_{CC} = MAX, V_{IN} = 0.4V	5.5	—	−700	μA

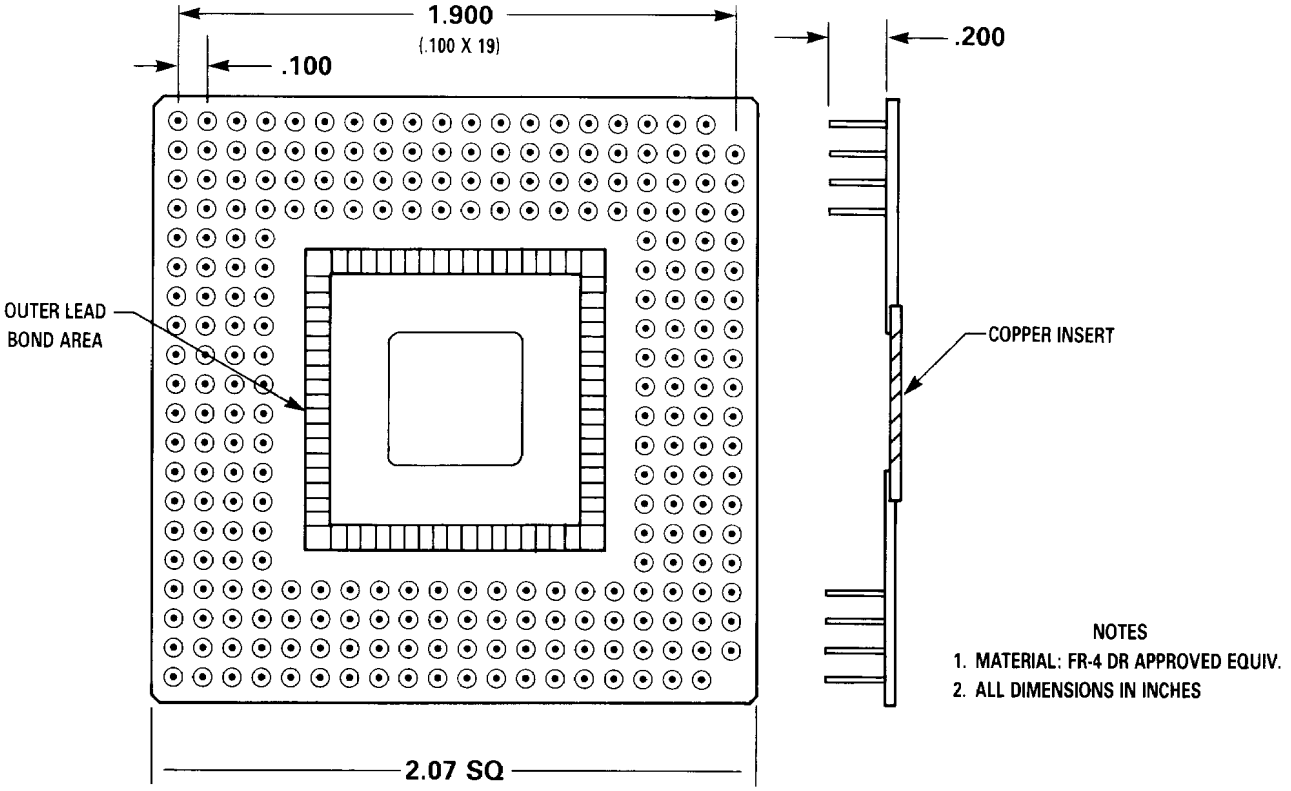
**Current Per Input

FIGURE 15 — 169-PIN-GRID-ARRAY PACKAGE DIMENSIONS



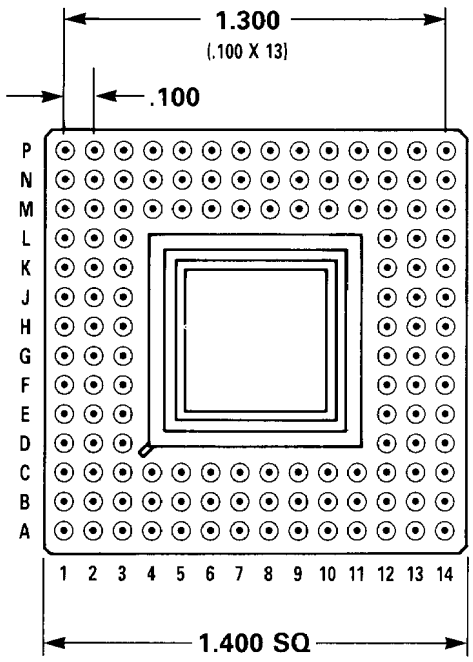
169 Pins: 130 Signal Pins, 10 Negative Supply, 8 Positive Supply, 20 Ground, 1 Orientation
V_{EE} (−4.5 V, −5.2 V) — R4, R7, R10, R14, F17, C14, C10, C7, C4, K3
V_{SS} (0.0 V ground) — R8, R11, T16, L16, D15, C11, C8, E3, H3, N3
V_{SSO} (0.0 V output) — R6, R12, R15, M16, F16, C12, C6, C3, G3, L3
V_{DD} (+5.0 V) — N15, D3
V_{DDO} (+5.0 V output) — R3, R9, J17, C15, C9, J3
Orientation Pin — D4

254 PGA



NOTES
1. MATERIAL: FR-4 DR APPROVED EQUIV.
2. ALL DIMENSIONS IN INCHES

132 PGA



193 PGA