STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT NAME	Pre-Driver For 3Phase Blushless Motor
TYPE	**BD6926FV**
FEATURES	・MOS-FET Pre-Driver ・120° phase Direct PWM input

○ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VCC	7	V
Output Current	I_{OMAX}	40 *1	mA
Input voltage	V_{IN}	0～VCC	V
AL terminal voltage	V_{AL}	7	V
AL output current	I_{ALMAX}	10	mA
FG, FG3 terminal voltage	V_{FG}	7	V
FG, FG3 output current	I_{FGMAX}	5	mA
Power dissipation	Pd	1025 *2	mW
Operating temperature range	T_{opr}	−40～+85	℃
Junction temperature	T_{jmax}	+150	℃
Storage temperature range	T_{stg}	−55～+150	℃

*1 Must not exceed Pd, ASO or Tjmax=150℃.
*2 Reduce by 8.2mW/℃ over 25℃, when mounted on a glass epoxy board (70mm×70mm×1.6mm).

○Operating Conditions (Ta=-40～+85℃)

Power Supply voltage	VCC	4.0～6.0	V

*This product is not designed for normal operation within a radio active environment.

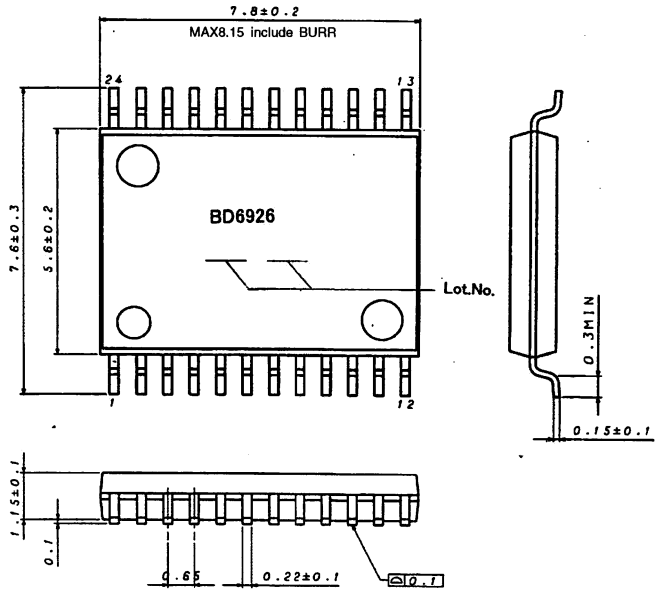
*Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

○Electrical Characteristics (Unless otherwise specified, Ta=25℃, VCC=5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<Overall>						
Circuit Current1	ICC1	2.2	4.6	7.0	mA	ST/SP=H
Circuit Current2	ICC2	—	—	10	μA	ST/SP=L
<UVLO>						
UVLO voltage	VUVLO	2.25	2.75	3.25	V	
hysteresis voltage	ΔVUVLO	0.35	0.50	0.65	V	
<ST/SP>						
ST voltage	VST	2.5	—	—	V	
SP voltage	VSP	—	—	1.0	V	
<Hall Comparator>						
Input Bias current	IHA	-3.0	-0.7	-	μA	
Common phase input voltage range	VHAR	1.0	—	3.5	V	
Input level	VINH	60	—	—	mVpp	
hysteresis voltage H	VHYSH	+8	+15	+22	mV	
hysteresis voltage L	VHYSL	-18	-11	-4	mV	
Hall maximum frequency	fHall	-	-	50	kHz	※guarantee of design
<Upper side output>						
Upper side output voltage	VHG	—	0.50	0.70	V	I=+30mA
<Lower side output>						
Lower side output voltage1	VLG1	4.00	4.50	-	V	I=-30mA
Lower side output voltage2	VLG2	—	0.50	0.70	V	I=+30mA
<Over current detection>						
Detection voltage	VTH	0.07	0.10	0.13	V	
Input voltage range	VIN	0.0	—	VCC	V	
Input bias current	IIB	-5.0	-0.9	-0.1	μA	
<Frequency for lock protection>						
Triangle wave peak	VLDCL	1.38	1.72	2.06	V	
Triangle wave bottom	VLDCP	0.8	1.0	1.2	V	
Charge current	ILDC	2.30	3.65	5.00	μA	
Lock detection output voltage	VALL	0.10	0.30	0.50	V	I_{AL}=10mA
Lock detection output leak current	IALL	—	0	10	μA	
<PWM input>						
ON voltage	VPWMON	2.5	—	—	V	
OFF voltage	VPWMOF	—	—	1.0	V	
PWM frequency	fPWM	10	20	100	kHz	※guarantee of design
<FG(3) output>						
Output voltage	VFG(3)L	0.10	0.30	0.50	V	I_{FG}=5mA
Output leak current	IFG(3)L	—	0	10	μA	
<Hall Bias>						
Output voltage	VHBL	0.60	0.87	1.20	V	I_{HB}=10mA
Output leak current	IHBL	—	0	10	μA	
<CW/CCW>						
CW voltage	VF	—	—	1.0	V	
CCW voltage	VR	2.5	—	—	V	
<Short Brake>						
ON voltage	VSBON	2.5	—	—	V	
OFF voltage	VSBOFF	—	—	1.0	V	

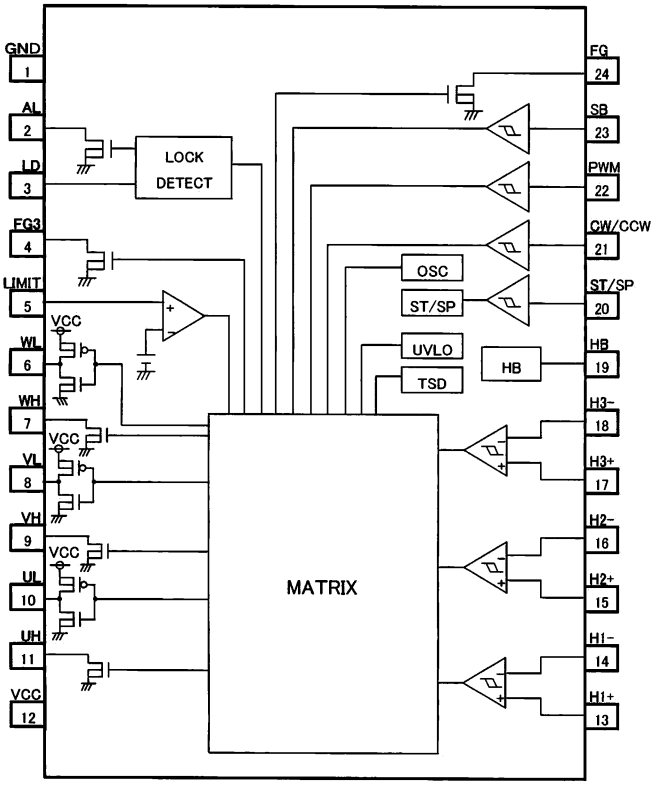
* Design target value (No total shipped devices are fully tested.)

●PHYSICAL DIMENSIONS・MARKING



SSOP-B24 (UNIT:mm)

● BLOCK DIAGRAM



●Pin No, Pin Name, Function

PIN No	Pin name	Function
1	GND	GND
2	AL	Lock detection pin
3	LD	Lock protection pin
4	FG3	FG(Composition of 3phase)pin
5	LIMIT	Current limit pin
6	WL	Output WL pin
7	WH	Output WH pin
8	VL	Output VL pin
9	VH	Output VH pin
10	UL	Output UL pin
11	UH	Output UH pin
12	VCC	Power supply pin
13	H1+	Hall input H1+ pin
14	H1-	Hall input H1- pin
15	H2+	Hall input H2+ pin
16	H2-	Hall input H2- pin
17	H3+	Hall input H3+ pin
18	H3-	Hall input H3- pin
19	HB	Hall bias pin
20	ST/SP	Start/Stop pin
21	CW/CCW	CW/CCW pin
22	PWM	PWM input pin
23	SB	Short brake pin
24	FG	FG(Composition of 1phase)pin

* Refer to the Technical Note about the details of the application.

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage (VCC) or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

(2) Power Supply and Ground Wiring

The motor ground PGND pin is not connected to the IC GND pin. Separate the large-current PGND from the signal GND, and make one common ground point at a single reference point. These configurations will eliminate ground fluctuation between power sections and signal sections of the circuit. An overshooting, undershooting, or oscillation, on the power supply line, can occur due to instantaneous load fluctuations, which in turn, is due to a slow response of the power supply to instantaneous response. Fluctuating voltage on the power supply and ground lines may damage the device. Be sure to connect a bypass filter capacitor (1μF to 100μF) as close as possible to the IC between the power supply and ground pins. Check that the selected capacitance will not have an adverse influence on any characteristics, such as a drop in the electrolytic capacitor value that can occur at low temperatures. If it is necessary, add zener diode protection. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

(4) Thermal design

Use a proper thermal design that allows for a sufficient margin of the power dissipation (Pd) at actual operating conditions.

(5) Pin short and wrong direction assembly of the device.

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

(6) Avoiding strong magnetic field

Malfunction may occur if the IC is used around a strong magnetic field.

(7) ASO

Ensure that the output transistors of the motor driver are not driven under excess conditions of the absolute maximum ratings and ASO.

(8) TSD (Thermal Shut Down) circuit

If the junction temperature (Tjmax) reaches 175°C (Typ.), the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysteresis of approximately 25°C (Typ.). The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.

(9) Testing an application board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

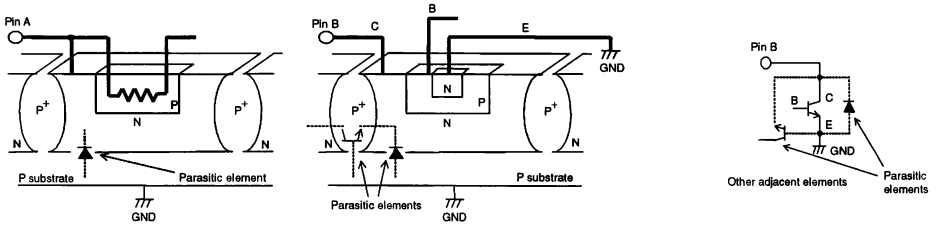
(10) Regarding the input pin of the IC

This monolithic IC contains P^+ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.

Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic elements operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



Example of Simple IC Architecture

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