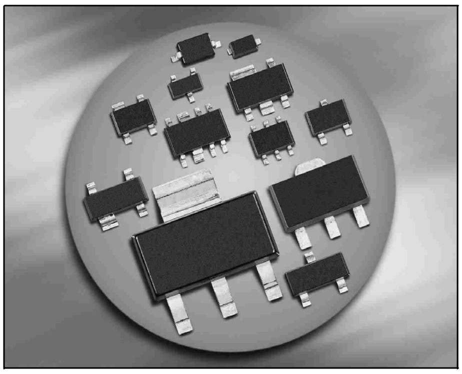
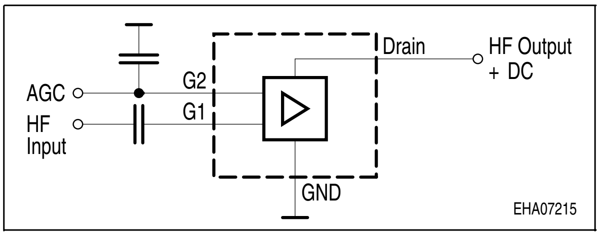
Silicon N-Channel MOSFET Tetrode



- For low noise, high gain controlled input stages up to 1 GHz
- Operating voltage 5V
- Integrated biasing network



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BF1005	SOT143	1=S	2=D	3=G2	4=G1	-	-	MZs
BF1005R	SOT143R	1=D	2=S	3=G1	4=G2	-	-	MZs
BF1005W*	SOT343	1=D	2=S	3=G1	4=G2	-	-	MZ

* on request only

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation	P_{tot}		mW
$T_S \leq 76$ °C, BF1005, BF1005R		200	
$T_S \leq 94$ °C, BF1005W		200	
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Note:
It is not recommended to apply external DC-voltage on Gate 1 in active mode.

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point[1]	R_{thchs}		K/W
BF1005, BF1005R		≤ 370	
BF1005W		≤ 280	

Electrical Characteristics

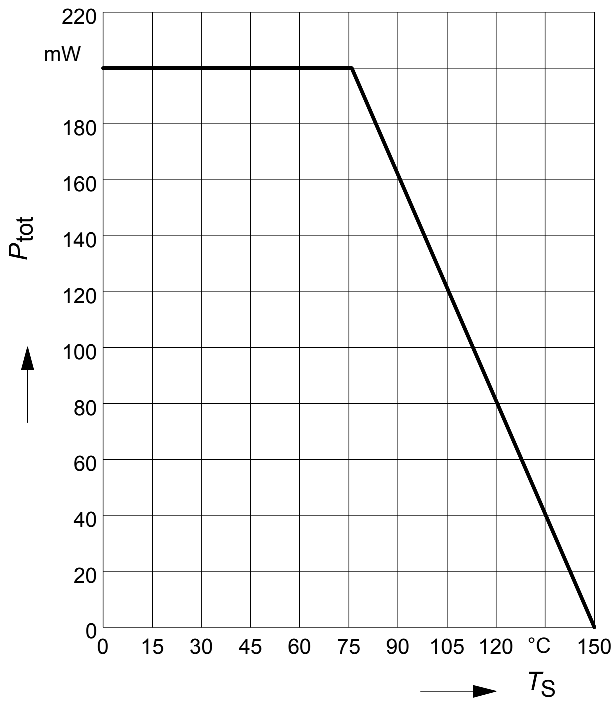
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 650 µA, V_{G1S} = 0 , V_{G2S} = 0	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S}$ = 10 mA, V_{G2S} = 0 , V_{DS} = 0	$+V_{(BR)G1SS}$	8	-	12	
Gate2 source breakdown voltage $\pm I_{G2S}$ = 10 mA, V_{G1S} = 0 , V_{DS} = 0	$\pm V_{(BR)G2SS}$	8	-	13	
Gate1-source leakage current V_{G1S} = 0 , V_{G2S} = 6 V	$+I_{G1SS}$	-	100	-	µA
Gate 2 source leakage current $\pm V_{G2S}$ = 8 V, V_{G1S} = 0 , V_{DS} = 0	$\pm I_{G2SS}$	-	-	50	nA
Drain current V_{DS} = 5 V, V_{G1S} = 0 , V_{G2S} = 4 V	I_{DSS}	-	-	1.5	mA
Operating current (selfbiased) V_{DS} = 5 V, V_{G2S} = 4 V	I_{DSO}	8	10	16	
Gate2-source pinch-off voltage V_{DS} = 5 V, I_D = 100 µA	$V_{G2S(p)}$	-	1	-	V

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

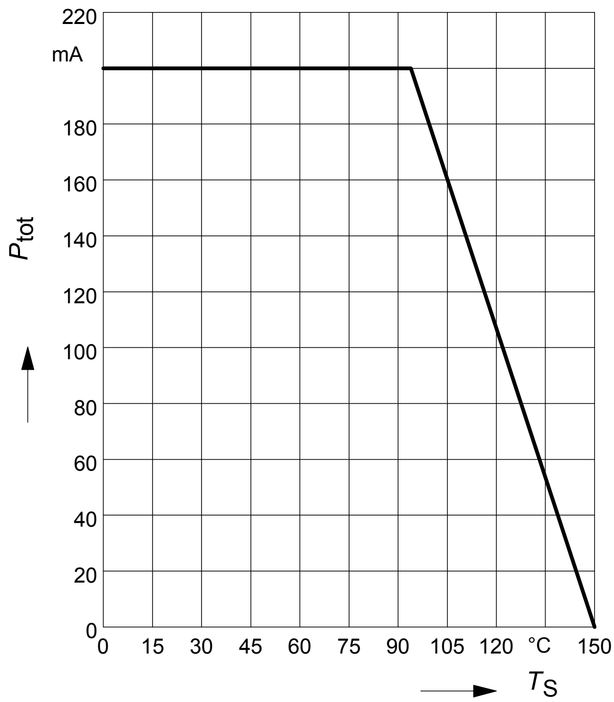
Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Forward transconductance V_{DS} = 5 V, V_{G2S} = 4.5 V	g_{fs}	20	24	-	mS
Gate1 input capacitance V_{DS} = 5 V, V_{G2S} = 4 V, f = 1 MHz	C_{g1ss}	-	2.1	2.5	pF
Output capacitance V_{DS} = 5 V, V_{G2S} = 4 V, f = 100 MHz	C_{dss}	-	1.3	-	
Power gain (self biased) V_{DS} = 5 V, V_{G2S} = 4 V, f = 800 MHz	G_p	17	19	-	dB
Noise figure V_{DS} = 5 V, V_{G2S} = 4 V, f = 800 MHz	F	-	1.6	2.5	dB
Gain control range V_{DS} = 5 V, V_{G2S} = 4V ...0V, f = 800 GHz	ΔG_p	40	50	-	

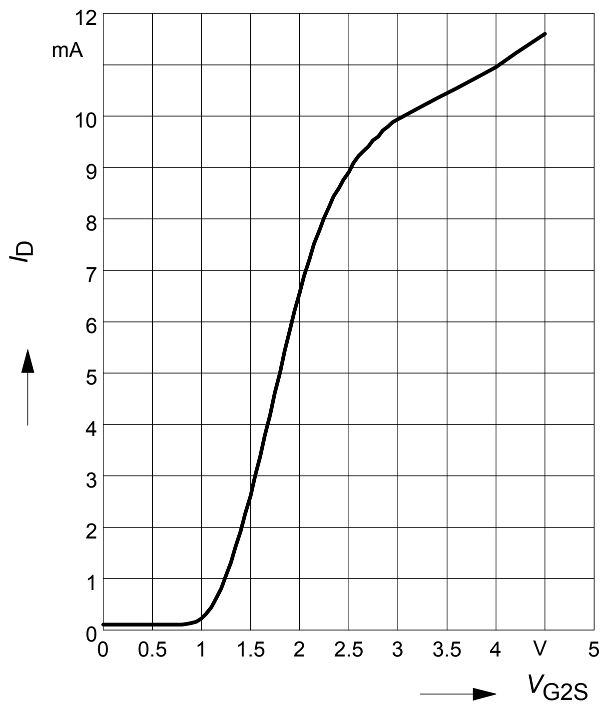
Total power dissipation $P_{tot} = f(T_S)$
BF1005, BF1005R



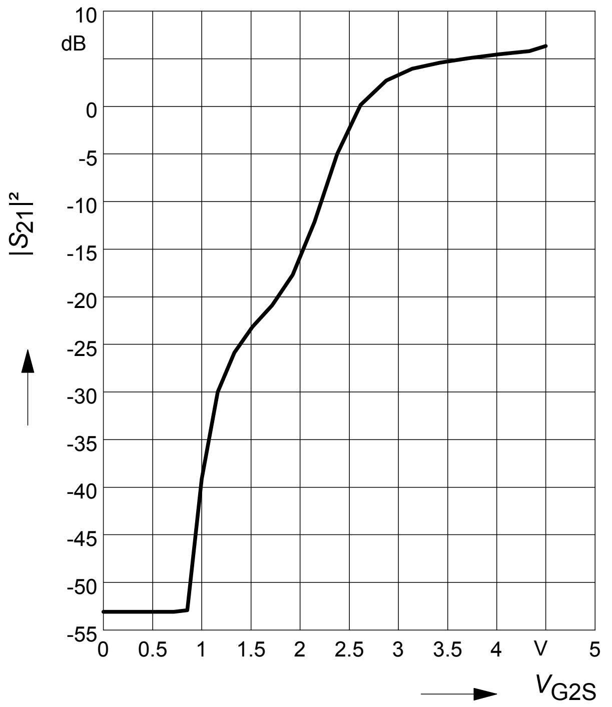
Total power dissipation $P_{tot} = f(T_S)$
BF1005W



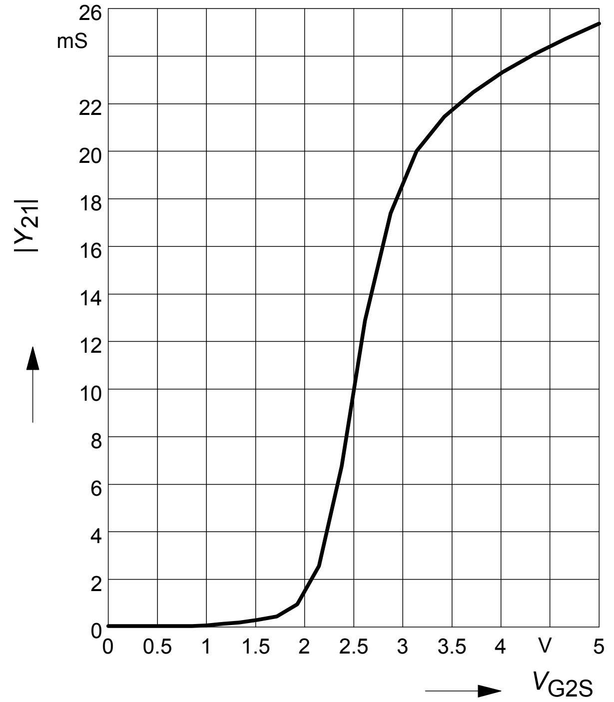
Drain current $I_D = f(V_{G2S})$



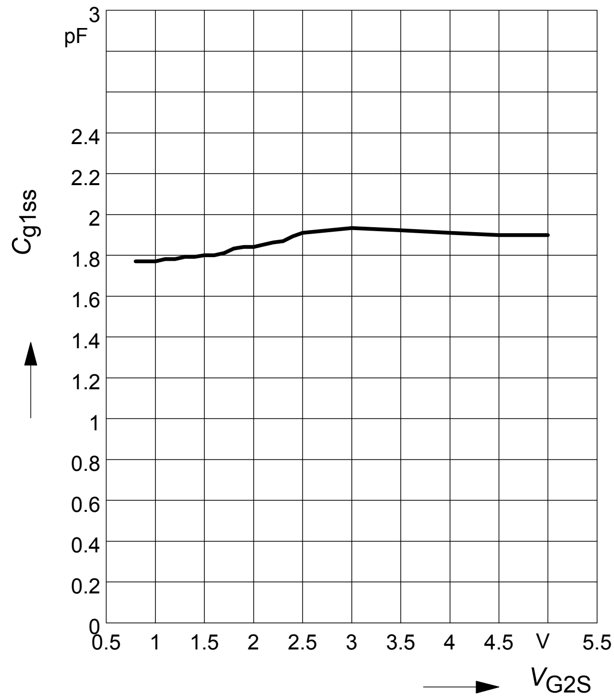
Insertion power gain
$|S_{21}|^2 = f(V_{G2S})$



Forward transfer admittance
$|Y_{21}| = f(V_{G2S})$



Gate 1 input capacitance $C_{g1ss} = f(V_{g2s})$
f = 200MHz



Output capacitance $C_{dss} = f(V_{G2S})$
f = 200MHz