DATA SHEET

BGB110
Bluetooth radio module

Objective specification 2000 Oct 03

Philips Semiconductors

PHILIPS

FEATURES

- Plug-and-play Bluetooth class II radio module, needs only external antenna and reference clock
- Small dimensions (13.75 x 10.2 x 1.9 mm)
- Fully compliant to Bluetooth radio specification v1.0
- High sensitivity (typical −80 dBm)
- Advanced AFC for improved reception quality
- RSSI with high dynamic range
- BlueRF unidirectional JTAG RXMODE 2 compatible
- Simple interfacing to Philips VW2600X baseband controller family
- Internal shielding for better EMI (Electro Magnetic Interference) immunity.
- 13 MHz system clock output for baseband processor
- 2.048 MHz clock output for PCM voice codecs.

APPLICATIONS

Bluetooth transceivers in:

- Cellular phones
- Laptop computers
- Personal digital assitants
- Consumer applications.

DESCRIPTION

The BGB110 TrueBlue Bluetooth radio module is a short-range radio transceiver for wireless links operating in the globally available ISM band, between 2402 and 2480 MHz. It is composed of a fully integrated, state-of-the-art near-zero-IF transceiver chip, an antenna filter for improved out-of-band blocking performance, a TX/RX switch, TX and RX baluns, the VCO resonator and a basic amount of supply decoupling. The device is a “Plug-and Play” module that needs no external components for proper operation. Robust design allows for untrimmed components, giving a cost-optimized solution. Demodulation is done in open-loop mode to reduce the effects of reference frequency breakthrough on reception quality. An advanced AFC circuit compensates for VCO drift and RF frequency errors during open-loop demodulation.

The circuit is integrated on a ceramic substrate. It is connected to the main PCB through a LGA (Land Grid Array). A metal cap suppresses the effects of EMI (Electro Magnetic Interference). The RF port has a normalized 50 Ω impedance and can be connected directly to an external antenna, with a 50 Ω transmission line.

The control interface is compatible whith BlueRF unidirectional JTAG RXMODE 2. The connection to Philips Semiconductors VW2600X family of Bluetooth baseband processors is straightforward.

Frequency selection is done internally by a conventional synthesizer. The synthesizer accepts a reference frequency of 13 MHz. This reference frequency should either be stabilised by an external crystal or be supplied by en external source. The 13 MHz clock signal is also made available as a system clock to the baseband processor. It can be switched off for power saving. In that case, a 3.2 kHz clock is provided for wake-up timing.

A 1 MHz reference, derived from the 13 MHz system clock, is available externally to clock out the transmit data from the baseband processor. The BGB110 also provides a 2.048 MHz clock for PCM voice codecs

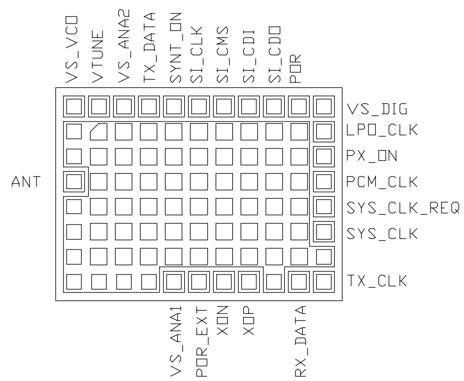
The circuit is designed to operate from 3.0 V nominal supplies. Separate ground and supply connections are provided for reduced parasitic coupling between different stages of the circuit. There is a basic amount of RF supply decoupling incorporated into the circuit.

The envelope is a leadless SOTtbdA package with a metal cap.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING

PIN	DESCRIPTION
1	VCO supply voltage
2	VCO tuning voltage (for test only)
3	analog part 2 supply voltage
4	transmit data stream input
5	synthesiser turn-on input signal
6	serial interface (JTAG) clock input
7	serial interface (JTAG) control mode select input
8	serial interface (JTAG) control data input
9	serial interface (JTAG) control data output
10	power-on reset output
11	digital part supply voltage
12	low-power clock output
13	packet switching on input signal
14	2.048 MHz clock output for PCM codecs
15	system clock request input
16	system clock output
17, 20, 25, 26, 27, 28, 29, 30, 31, 33, 34	ground
18	transmit data clock output
19	receive data stream output
21	crystal oscillator output
22	crystal oscillator or external clock input
23	power-on reset input
24	analog part 1 supply voltage
32	antenna input/output



bottom view

Fig.1 Simplified outline

QUICK REFERENCE DATA

V_S = 3.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage		2.8	3	3.6	V
I_S (RX guard)	supply current	during RX guard space	–	30	–	mA
I_S (RX demod)	supply current	during demodulation	–	65	–	mA
I_S (TX guard)	supply current	during TX guard space	–	43	–	mA
I_S (TX)	supply current	during transmission	–	37	–	mA
I_S (pd)	supply current	in power-down mode	–	1	–	mA
Sens	receiver sensitivity	BER = 0.1 % under standard conditions	–	–80	–73	dBm
P_{out}	output power		–	0	–	dBm
f_0	RF frequency		2402	–	2480	MHz
f_{ref}	reference input frequency		–	13	–	MHz
T_{amb}	operating ambient temperature		–10	–	50	°C

BLOCK DIAGRAM

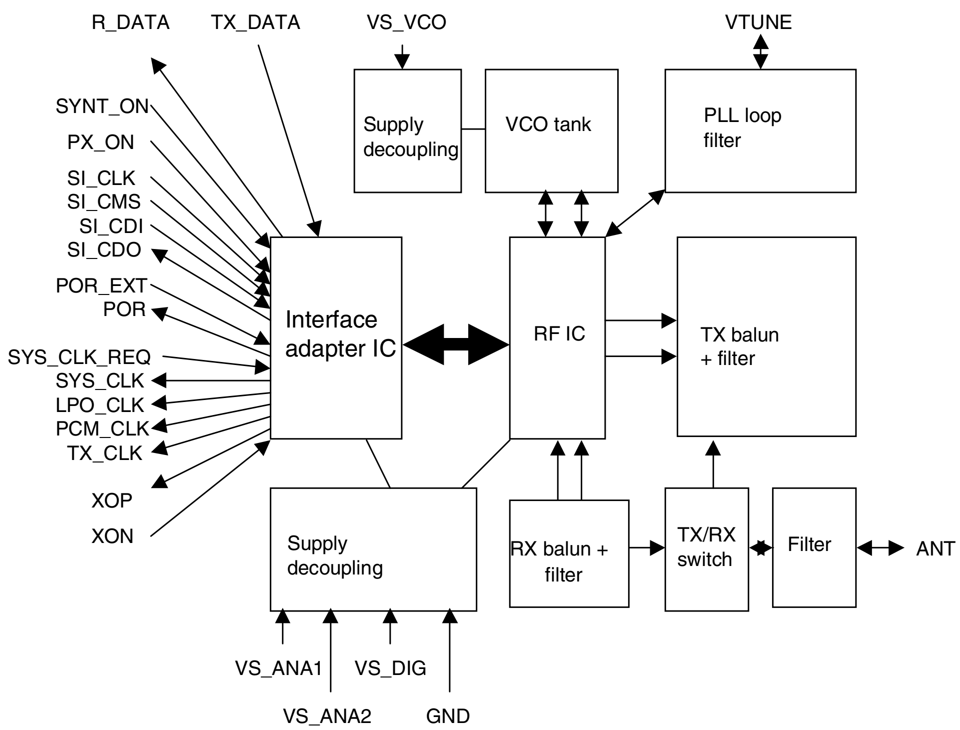


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

Control

The BGB110 TrueBlue Bluetooth Radio Module is compatible with BlueRF unidirectional JTAG RXMODE 2. It can be controlled directly by a Philips VW2600X family baseband processor, via an 8-wire control interface.
These 8 wires can be grouped into:

- A four-wire serial JTAG interface for initialisation and general control of the radio module. The control signals are SI_CDI (control data input), SI_CMS (control mode select), SI_CLK (control clock) and SI_CDO (control data output).
- Three asynchronous control input signals SYS_CLK_REQ, PX_ON and SYNT_ON.
- One asynchronous reset input signal POR_EXT.

These latter four wires control specific blocks inside the radio module.

Furthermore, the BGB110 supplies the baseband processor with four clock signals:

- A 13 MHz system clock SYS_CLK, which can be switched off in order to save power.
- A 1 MHz transmit clock TX_CLK, for clocking out the data to be transmitted.
- A 3.2 kHz low-power clock for wake-up timing in the baseband processor.
- A 2.048 MHz clock for PCM voice codecs.

JTAG interface

The JTAG serial interface is used to control the BGB110. The BGB110 has to be the only slave on the JTAG bus, it does not allow for multi-slave operation. The JTAG interface protocol used is fully compliant with the standard set out in IEEE Std 1149.1-1990. The following features are supported:

- 5-bit register address.
- 8-bit data.
- Set instruction register.
- Read/write data register (note that some addresses denote separate read and write data registers).

The JTAG interface allows for 2 ways of accessing a register. One is the communicate address and data, and the second one is for successive accesses to the same register where only the data is communicated. This can e.g. be used for updating the channel information before every packet.

STATE DIAGRAM

The state diagram is shown in Fig.3. Transitions from one state to another depend on the SI_CMS input at the rising edge of SI_CLK. The SI_CMS and SI_CDI should change value at the falling edge of SI_CLK. Output SI_CDO will also change at the falling edge of SI_CLK.

An instruction register scan (IR-Scan) period starts with a status information download (Capture-IR). The status inputs to the instruction register are user-defined observability inputs. Afterwards, the data can be shifted out (Shift-IR), at the same time as serial data/instruction are shifted in, or directly updated to the parallel output (Exit1-IR, Update-IR).

There is also a possibility for the IR-Scan period to be paused (Pause-IR) before a new data-shift. A data register scan period is identical but there are no restrictions on the data during Capture-DR.

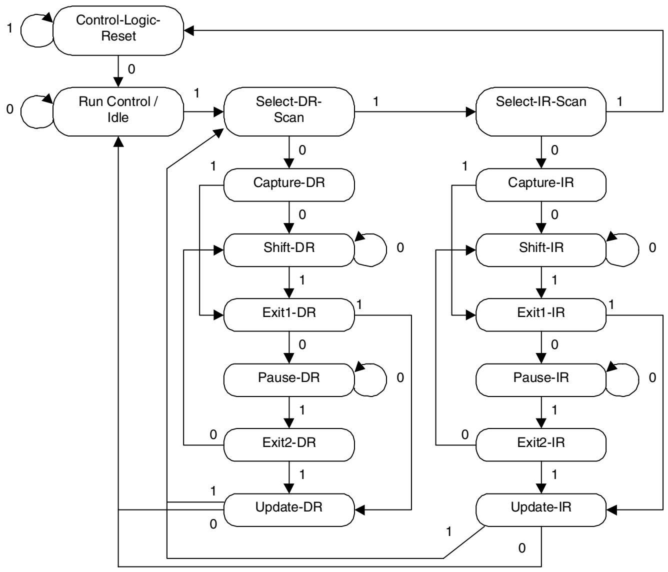


Fig.3 State diagram for register programming using the JTAG serial interface

REGISTER SCAN

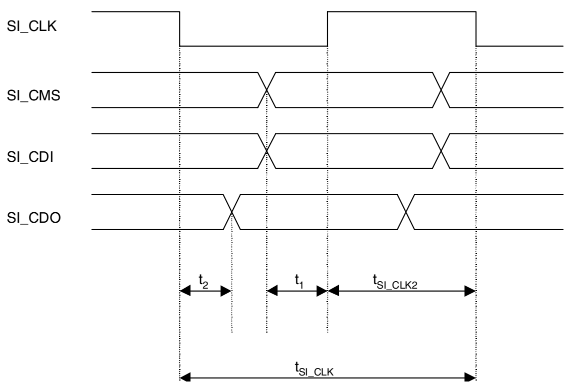
There are two types of register scans used for controlling the functionality:

- IR (instruction register) scan is the normal read/write instruction. This instruction selects a specific register to write to or read from.
- DR (data register) scan where 8 bits of data are shifted into the register.

By choosing the register with an IR scan and performing a DR scan the data can be captured into the instruction registers.

TIMING

The serial interface is operational when there is a 13 MHz SYS_CLK and POR_EXT is ‘high’. All input signals (SI_CDI, SI_CMS) into the serial interface should change on the negative edge of the serial clock (SI_CLK). The serial interface samples the SI_CDI and SI_CMS signals on the positive edge of SI_CLK to eliminate setup and hold violations. The output signal (SI_CDO) should also change on the negative edge of SI_CLK. The input data always be in whole bytes.



	MIN.	TYP.	MAX.	UNIT
t_{SI_CLK}	200	250	–	ns
t_{SI_CLK2}	76	76	–	ns
t_1	20	–	–	ns
t_2	–	–	20	ns

Fig.4 Timing diagram for the JTAG serial interface

Registers

The following registers are important for setting up a Bluetooth link with the BGB110. They are controlled over the serial interface.

REGISTER		ADDRESS	RESET	DESCRIPTION
S_EN_WIDTH	R/W	9	0xC8	S_EN width
CHANNEL	W	18	0x00	frequency channel number and TX/RX information
RSSI	R	18	0x00	RSSI
XO_Trim	W	19	0x80	trim value for system clock
ID	R	19	0xA1	device identification
CONTROL	R/W	22	0x00	system clock control
ENABLE	R/W	25	0x00	module control
GFSK_TABLE	R/W	28	0x00	GFSK filter lookup table values

S_EN_WIDTH

The S_EN_WIDTH register is used to control the amount of time that the RF frequency synthesizer has to switch from one frequency to the next, and to settle down. It defaults to 200 µs.

S_EN_WIDTH	b7	b6	b5	b4	b3	b2	b1	b0
9	S_EN_WIDTH							

Bits b7 -b0	S_EN_WIDTH	S_EN_WIDTH (in µs)

CHANNEL PROGRAMMING

The serial interface channel programming word is converted to a synthesizer division ratio.

CHANNEL	b7	b6	b5	b4	b3	b2	b1	b0
18	trx	channel number						

Bit b7	trx	0 = TX, 1 = RX
Bits b6 - b0	channel number	channel 0 is at 2402 MHz, channel 78 is at 2480 MHz. There is no need to program different values for RX and TX on the same channel

RSSI

The RSSI is read via the serial interface. The RSSI value can only be read from the serial interface register after the measurement has been completed, which is at the end of the packet. RSSI measurements are only done in receive packets.

RSSI	b7	b6	b5	b4	b3	b2	b1	b0
18	RSSI							

XO_TRIM

The XO_Trim register is used to control the frequency of the 13 MHz oscillator, by controlling the capacitive load on the XIN and XOUT pins.

XO_TRIM	b7	b6	b5	b4	b3	b2	b1	b0
19	not used	XO-trim						

Bit b7	not to be used
Bit b6	add 6 pF to XIN and XOUT
Bit b5	add 3 pF to XIN and XOUT
Bit b4	add 1.5 pF to XIN and XOUT
Bit b3	add 0.75 pF to XIN and XOUT
Bit b2	add 0.375 pF to XIN and XOUT
Bit b1	add 0.1875 pF to XIN and XOUT
Bit b0	add 0.09375 pF to XIN and XOUT

ID

The ID register is used to identify the BGB110 set from the baseband. This is read only.

ID	b7	b6	b5	b4	b3	b2	b1	b0
19	ID							

Bits b7 -b0	ID	radio chip set identification (value = 0xA1)

CONTROL

The CONTROL register is used to control SYS_CLK in the BGB110.

CONTROL	b7	b6	b5	b4	b3	b2	b1	b0
22	not used				Rdy	not used		

Bits b7 - b3	not used	not to be used
Bit b2	Rdy	baseband ready, used to control the function of SYS_CLK_REQ
Bits b1 - b30	not used	not to be used

ENABLE

The ENABLE register is used to control functions inside the BGB110

ENABLE	b7	b6	b5	b4	b3	b2	b1	b0
25	not used	grst	not used	clk_en	not used			

Bit b7	not used	not to be used
Bit b6	grst	GFSK table address reset. Writing ‘1’ will reset the GFSK table addressing. This bit needs to be reset to ‘0’ before writing to the GFSK table
Bit b5	not used	not to be used
Bit b4	clk_en	enables the 2.048 MHz clock on PCM_CLK, ‘0’ = clock diable, ‘1’ = clock enable
Bits b3 - b0	not used	not to be used

GFSK_TABLE

The GFSK_TABLE register defines the Gaussian filtering of the datastream to be transmitted. It consists of 13 registers, the contents of which define the shape of the Gaussian-filtered modulating signal. There is an auto-increment facility, so that subsequent writes to this register result in subsequent shape values being written. Setting the ‘grst’ bit in the ENABLE register to ‘1’ resets the auto-increment counter. It should be reset to ‘0’ before loading the shape values. The values into this table depend on the supply voltage. Below is given an example table that can be used for a 3.0 V supply voltage. If there is a different supply voltage, these values should be scaled accordingly.

GFSK_TABLE	b7	b6	b5	b4	b3	b2	b1	b0
28	GFSK_TABLE							

Bits b7 -b0	GFSK_TABLE	Gaussian filter shape value

Shape value #	Value
0	0x3B
1	0x3C
2	0x3E
3	0x42
4	0x4A
5	0x57
6	0x66
7	0x75
8	0x82
9	0x8A
10	0x8E
11	0x90
12	0x91

Reset

The BGB110 has an internal power-on reset function, which is operational every time the supply voltage is switched on. This will reset all internal registers and will bring the device into a known state. Next to the built-in power-on reset, there is the POR_EXT reset signal. This will also reset the device and put it into the same state as the power-on reset. The POR_EXT signal is intended to be used as a reset from a host processor.
Following the power-on reset or a POR_EXT reset, the system oscillator is started and the SYS_CLK output is activated (enabled). The SYS_CLK can be controlled by the SYS_CLK_REQ signal. It will only control the SYS_CLK once the Rdy bit in the CONTROL register has been set. The function of the SYS_CLK _REQ has two phases:

1. After reset, the SYS_CLK_REQ is not taken into account for generation of SYS_CLK. The 13 MHz system clock is enabled on SYS_CLK.
2. Once register CONTROL Rdy is set to ‘1’, the 13 MHz system clock on the SYS_CLK is controlled by SYS_CLK_REQ.

SYS_CLK_REQ does not control the oscillator itself. The oscillator will not be disabled by the SYS_CLK_REQ signal. LPO_CLK output is only controlled by the POR_EXT which also controls the POR output. POR is activated 4 SYS_CLK cycles after POR_EXT.

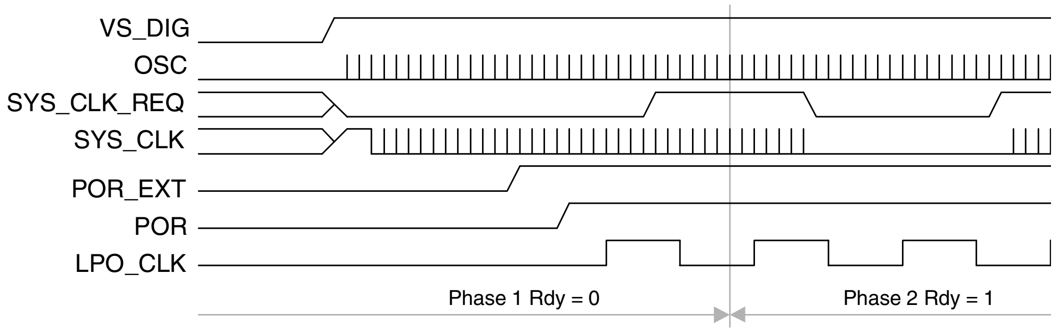


Fig.5 Reset timing

Transmit mode

The BGB110 TrueBlue Bluetooth radio module contains a fully integrated transmitter function. The RF channel frequency is selected in a conventional synthesizer, which is controlled via the serial JTAG interface. After the RF frequency has settled, the power amplifier is switched on and the modulation input is preset to its mean value. The RF frequency is allowed to resettle, to overcome possible frequency pulling effects, and the synthesizer loop is opened.
The data stream present on the TX_DATA line is Gaussian filtered and converted to an analog signal which then directly modulates the VCO. The robust design of the VCO makes it unnecessary to trim its freerunning frequency. This leads to a lower component cost. A carefully designed PLL loop filter keeps frequency drift during open-loop modulation down to a very low value.
The output stage of the transmit chain active part is balanced, for reduced spurious emissions (EMC). It is connected through a balun (balanced-to-unbalanced) circuit to the TX/RX switch. This switch is controlled by internal logic circuits in the active die. The balun circuit has built-in selectivity, to further reduce out-of-band spurious emissions.

Receive mode

Also the receiver functionality is fully integrated. It is a near-zero-IF (1 MHz) architecture with active image rejection. The sensitive RX input of the active die is a balanced configuration, in order to reduce unwanted (spurious) responses. The balun structure to convert from unbalanced to balanced signals has built-in selectivity. This suppresses GSM-900 frequencies by more than 40 dB. For better immunity to DCS, DECT, GSM-1800 and W-CDMA signals, an extra band-pass filter has been included.

The synthesizer PLL is switched off during demodulation. This reduces the effects that reference frequency breakthrough may have on receiver sensitivity, and also reduces the power consumption. The demodulator contains an advanced AFC circuit. This reduces the effects of frequency mismatch between (remote) transmitter and receiver. These may be caused by differences in reference frequency, but also by frequency drift during open-loop modulation and demodulation.

The demodulated RF signal is sampled and compared against a reference (slicer) value and then output on the RX_DATA line. An RSSI output with a high dynamic range of nearly 50 dB provides information on the quality of the signal received. The RSSI value is read out via the JTAG interface, as described above.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_S	supply voltage		–0.3	3.6	V
V_{ctrl}	control pin voltage		–0.3	V_S	V
ΔGND	difference in ground supply voltage between ground pins	note 1	–	0.01	V
P_{tot}	total power dissipation		–	tbd	W
P_D	drive power at receiver input		–	0	dBm
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–10	+50	°C
T_j	junction temperature		–	150	°C

Notes

1. Pins short-circuited internally must be short-circuited externally.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	tbd	K/W

CHARACTERISTICS

V_{CC} = 3.0 V; T_{amb} = 25 °C; f_{dev} = 160 kHz; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_S	supply voltage		2.8	3.0	3.6	V
$I_{S(GUARD-RX)}$	total supply current	during RX guard space	–	30	tbd	mA
$I_{S(RX)}$	total supply current	during RX (PLL off)	–	65	tbd	mA
$I_{S(GUARD-TX)}$	total supply current	during TX guard space	–	43	tbd	mA
$I_{S(TX)}$	total supply current	during TX (PLL off)	–	37	tbd	mA
$I_{S(pd)}$	total supply current	power-down mode	–	1	tbd	mA
Frequency selection						
f_{ref}	reference input frequency			13		MHz
Δf_{ref}	reference frequency inaccuracy		tbd	–	tbd	ppm
$V_{ref(min)}$	sinusoidal input signal level	RMS value	tbd	–	tbd	mV
R_{in}	input resistance (real part of the input impedance)	at 13 MHz; XON, XOP pins	–	tbd	–	kΩ
C_{in}	input capacitance	at 13 MHz; XON, XOP pins	–	tbd	–	pF
f_{VCO}	oscillator frequency	over full temperature and supply range; note 1	1201	–	1240	MHz
CNR_{500kHz}	carrier to noise ratio	offset from carrier 500 kHz	89	105	–	dBcHz
$CNR_{2500kHz}$		offset from carrier 2500 kHz	120	tbd	–	dBcHz
$\Delta f_{1\ slot}$	carrier drift	over 1 TX slot	–25	0	25	kHz
$\Delta f_{3,\ 5\ slots}$		over 3, 5 TX slots (DM3, DH3, DM5, DH5 packets)	–40	0	40	kHz
t_{PLL}	PLL settling time	across entire band	–	150	200	µs
TX performance						
f_{RF}	RF frequency	over full temperature and supply range	2402	–	2480	MHz
Δf	VCO frequency deviation	“0” bit	–175	–160	–140	kHz
		“1” bit	140	160	175	kHz
P_o	output power	wanted channel	–6	0	4	dBm
$P_{o\ 1\ MHz}$	adjacent channel output power	at 1 MHz offset; measured in 100 kHz bandwidth; referred to wanted channel	–	–	–20	dBc
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	tbd	tbd	
$H_{1,\ VCO}$	VCO frequency feedtrough	referred to wanted output level; f_{RF} = 2450 MHz; f_{VCO} = 1225 MHz	–	tbd	tbd	dBc
$H_{3,\ VCO}$	VCO 3rd harmonic		–	tbd	tbd	dBc
$H_{4,\ VCO}$	VCO 4th harmonic		–	tbd	tbd	dBc
$H_{6,\ VCO}$	VCO 6th harmonic		–	tbd	tbd	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	out of band spurious emissions	30 MHz to 1 GHz	–	tbd	–36	dBm
		1 GHz to 12.75 GHz	–	tbd	–30	dBm
		1.8 GHz to 1.9 GHz	–	tbd	–47	dBm
		5.15 GHz to 5.3 GHz	–	tbd	–47	dBm
Receiver performance						
SENS	sensitivity	BER = 0.1 %	–	–80	–73	dBm
$P_{i\ max}$	maximum input power in one channel	BER < 0.1 %	–20	tbd	–	dBm
VSWR	voltage standing wave ratio	normalized to Z_o = 50 Ω	–	tbd	tbd	
f_{RF}	RF input frequency	over full temperature and supply range	2402	–	2480	MHz
RSSI	RSSI range		–86	–	–36	dBm
res_{RSSI}	RSSI resolution		–	8	–	bits
	RSSI linearity error		–0.5	–	0.5	lsb
IM_3	intermodulation rejection	wanted signal –64 dBm; Interferers 5 and 10 channels away; BER < 0.1 %	28	tbd	–	dBc
R_{CO}	co-channel rejection	wanted signal –60dBm; BER < 0.1 %	-11	-10	–	dBc
$R_{C/I\ 1MHz}$	adjacent channel rejection (± 1 MHz)	wanted signal –60dBm; BER < 0.1 %	0	3	–	dBc
$R_{C/I\ 2MHz}$	bi-adjacent channel rejection (N-2)	wanted signal –60dBm; BER < 0.1 %	30	tbd	–	dBc
$R_{C/I\ Image}$	rejection at image frequency (N+2)	wanted signal –67dBm; BER < 0.1 %	9	11	–	dBc
$R_{C/I\ Image\ 1MHz}$	rejection at image-adjacent frequency (N+3)	wanted signal –67dBm; BER < 0.1 %	20	27	–	dBc
$R_{C/I\ \geq 3MHz}$	image adjacent channel rejection	wanted signal –67dBm; BER < 0.1 %; N+3 is a special case, see above	40	tbd	–	dBc
	out of band blocking	wanted signal –67dBm; CW interferer level				
		range 30 MHz to 2 GHz	–10	–	–	dBm
		range 2 GHz to 2400 MHz	–27	–	–	dBm
		range 2500 MHz to 3 GHz	–27	–	–	dBm
		range 3 GHz to 12.75 GHz	–10	–	–	dBm
		wanted signal –67dBm; GSM modulated signal between 880 and 915 MHz (GSM–900 uplink)	tbd	tbd	–	dBm
		wanted signal –67dBm; GSM modulated signal between 1800 and 1785 MHz (GSM–1800 uplink)	tbd	tbd	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	spourious emissions	30 MHz to 1 GHz	–	tbd	tbd	dBc
		1 GHz to 12.75 GHz	–	tbd	tbd	dBc
FTLOrf	LO to RF feedthrough	measured at 2450MHz	–	tbd	-47	dBc
Interface (logic) inputs and outputs						
V_{IH}	HIGH-level input voltage		2.1	–	V_S	V
V_{IL}	LOW-level input voltage		–0.5	–	0.9	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
V_{OL}	LOW-level output voltage		–	–	0.5	V
I_{bias}	input bias current	HIGH or LOW level	–10	–	10	µA
f_{JTAG}	JTAG interface frequency		1	–	5	MHz
f_{SYS}	system clock frequency		–	13	–	MHz
f_{LPO}	low-power clock frequency		–	3.2	–	kHz

Notes

1. The VCO frequency is one-half the RF frequency.

SOLDERING

The indicated temperatures are those at the solder interfaces.

Advised solder types are types with a liquidus less than or equal to 210 °C.

Solder dots or solder prints must be large enough to wet the contact areas.

Soldering can be carried out using a conveyor oven, a hot air oven, an infrared oven or a combination of these ovens. A double reflow process is permitted.

Hand soldering is not recommended because the soldering iron tip can exceed the maximum permitted temperature of 250 °C and damage the module.
In case handsoldering is needed, recommendations can be found in RNR-45-98-A-0485.

The maximum allowed temperature is 250 °C for a maximum of 5 seconds.

The maximum ramp-up is 10 °C per second.

The maximum cool-down is 5 °C per second.

Cleaning

The following fluids may be used for cleaning:

- Alcohol
- Bio-Act (Terpene Hydrocarbon)
- Acetone.

Ultrasonic cleaning should not be used since this can cause serious damage to the product.

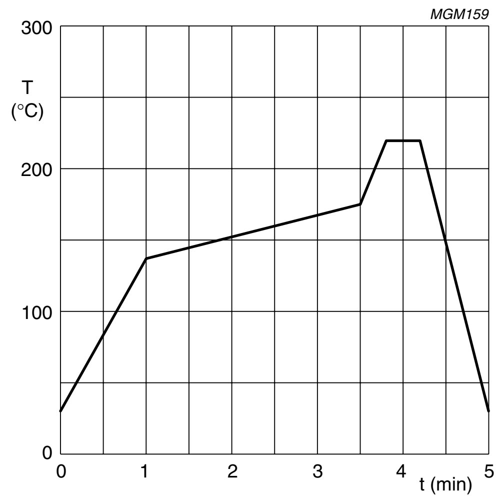


Fig.7 Recommended reflow temperature profile.

Packing

An extended packing / SMD specification can be found in document RNR-T49D-2183.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

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