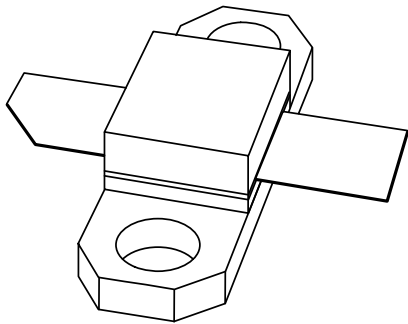


DATA SHEET



BLA1011-10 Avionics LDMOS transistor

Product specification
Supersedes data of 2002 Oct 02

2003 Nov 19

Avionics LDMOS transistor

BLA1011-10

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

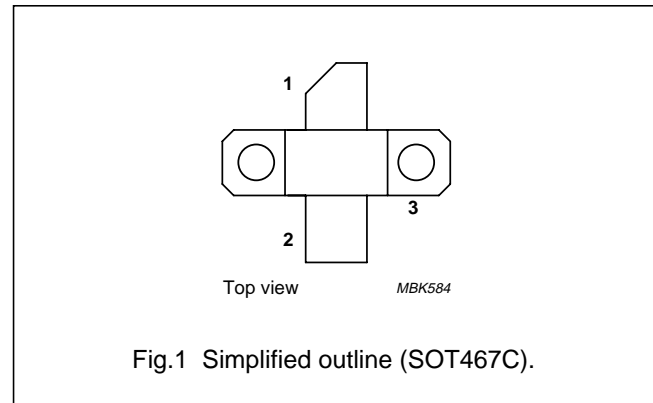
- Avionics transmitter applications in the 1030 to 1090 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ °C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
Pulsed class-AB; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$	1030 to 1090	36	10	>15	>40

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BLA1011-10	–	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	± 15	V
I_D	drain current (DC)		–	2.2	A
P_{tot}	total power dissipation	$T_h \leq 25\text{ °C}$	–	25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th(j-mb)}$	thermal impedance from junction to mounting base	$T_{mb} = 25\text{ °C}$; note 1	1.2	K/W
$R_{th(mb-h)}$	thermal resistance from mounting base to heatsink	note 2	0.55	K/W

Notes

1. Thermal impedance is determined under RF operating conditions with pulsed bias.
2. Typical value for SOT467C mounted with thermal compound and 0.6 Nm fastening torque.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.7\text{ mA}$	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 20\text{ mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$	–	–	0.1	mA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	2.8	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	40	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 0.75\text{ A}$	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 0.75\text{ A}$	–	1.2	–	Ω

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ °C}$; $R_{th\ mb-h} = 0.55\text{ K/W}$ unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)	PULSE DROOP (dB)
Pulsed class-AB; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$	1030 to 1090	36	50	10	>15	>40	<20	<20	<0.5

Ruggedness in class-AB operation

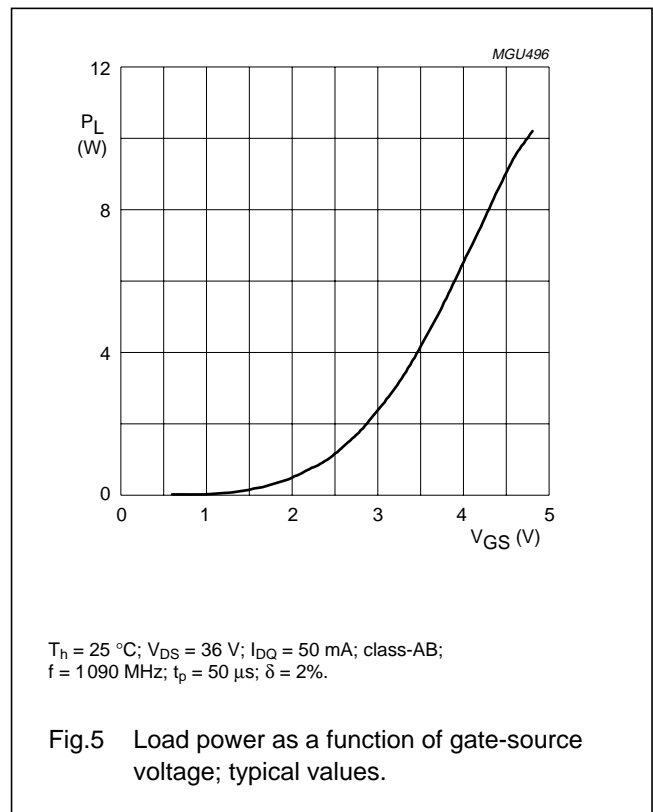
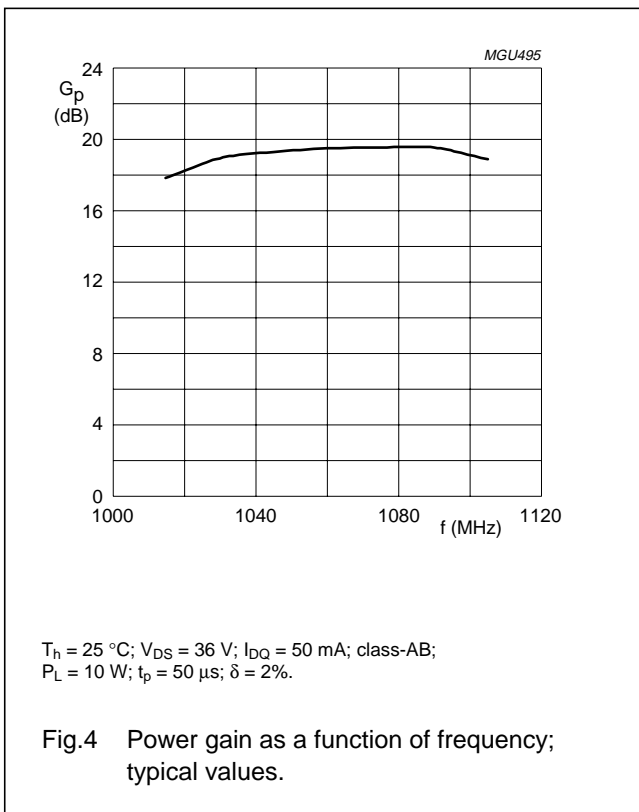
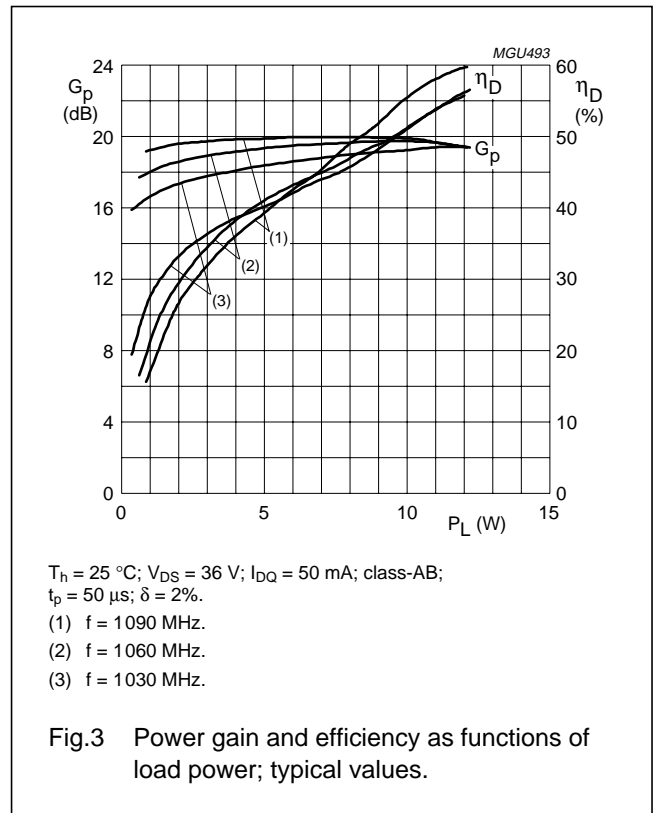
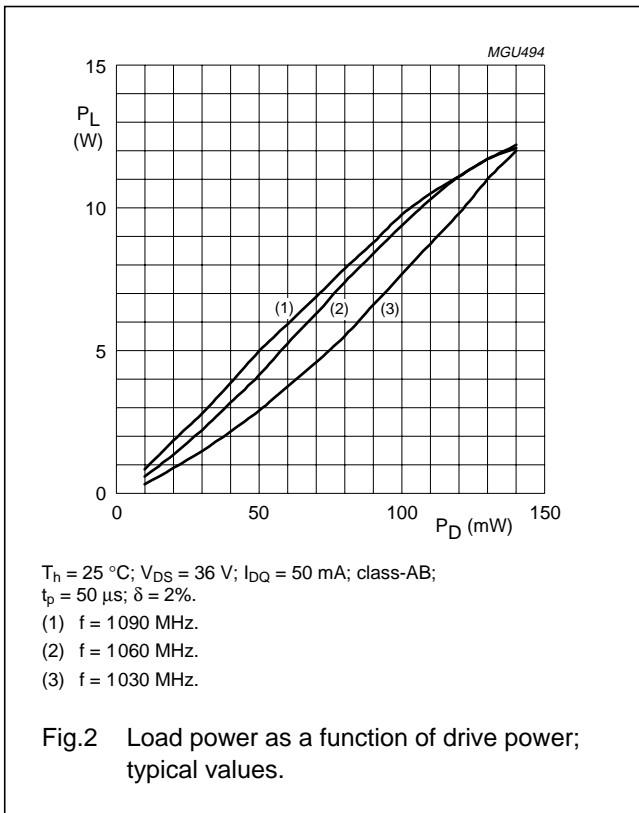
The BLA1011-10 is capable of withstanding a load mismatch corresponding to $VSWR = 5 : 1$ through all phases under the operating conditions.

Typical impedance values

FREQUENCY (MHz)	Z_S (Ω)	Z_L (Ω)
1030	$1 + j\ 10.6$	$4.3 + j\ 7$
1060	$1.3 + j\ 6.99$	$5.99 + j\ 13.98$
1090	$1.42 + j\ 7$	$7 + j\ 11.58$

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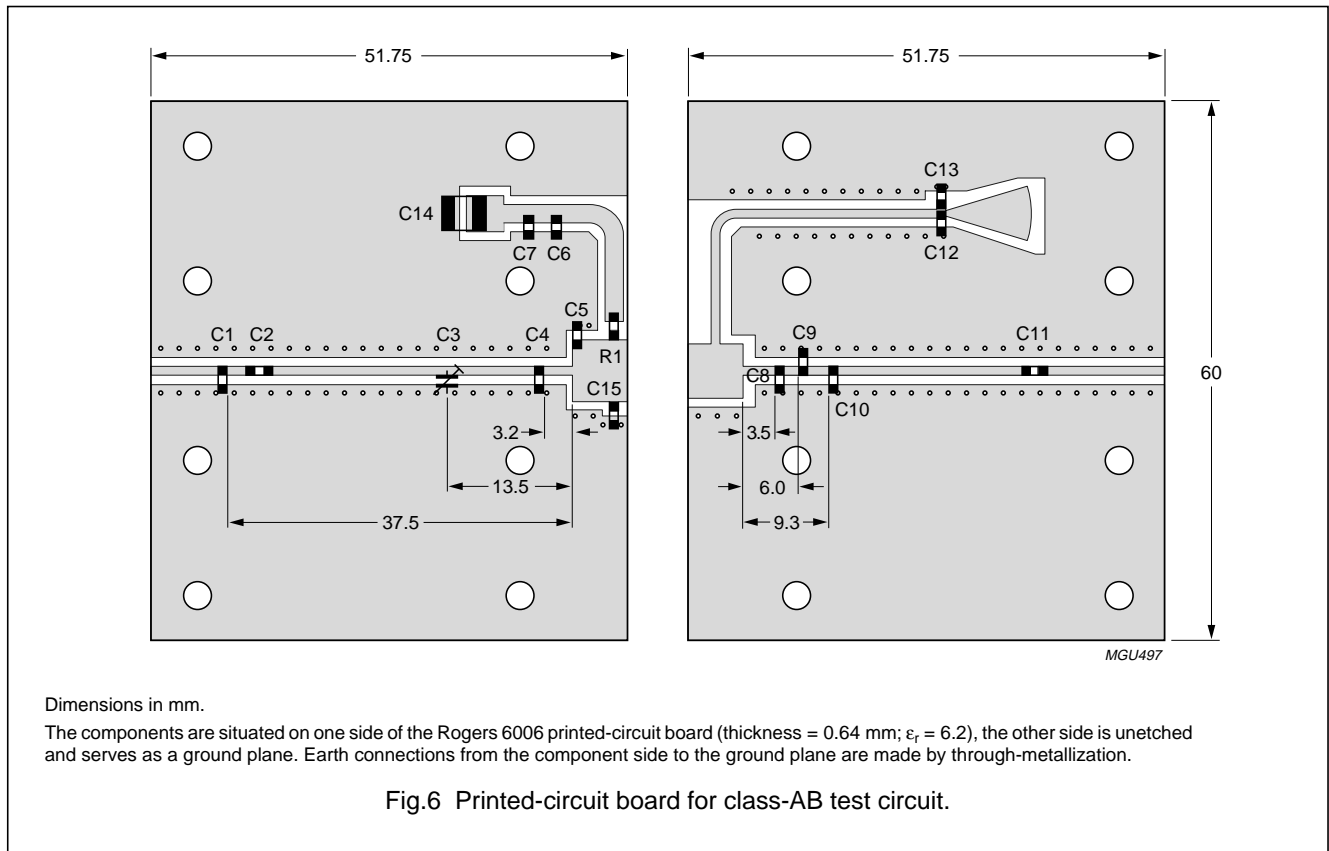


Fig.6 Printed-circuit board for class-AB test circuit.

List of components for class-AB test circuit (see Fig.6)

COMPONENT	DESCRIPTION	VALUE
C1	multilayer ceramic chip capacitor; note 1	2.7 pF
C2, C11	multilayer ceramic chip capacitor; note 1	56 pF
C3	tekelec trimmer; type 37293	0.8 to 8 pF
C4	multilayer ceramic chip capacitor; note 1	3.6 pF
C5	multilayer ceramic chip capacitor; note 1	6.2 pF
C6	multilayer ceramic chip capacitor; note 1	2 pF
C7, C13	multilayer ceramic chip capacitor; note 1	62 pF
C8	multilayer ceramic chip capacitor; note 1	11 pF
C9	multilayer ceramic chip capacitor; note 1	1.5 pF
C10	multilayer ceramic chip capacitor; note 1	6.2 pF
C12	multilayer ceramic chip capacitor; note 2	20 nF
C14	electrolytic capacitor	4.7 μ F; 50 V
C15	multilayer ceramic chip capacitor; note 1	36 pF
R1	SMD resistor (0805)	22 Ω

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- American Technical Ceramics type 200B or capacitor of same quality.

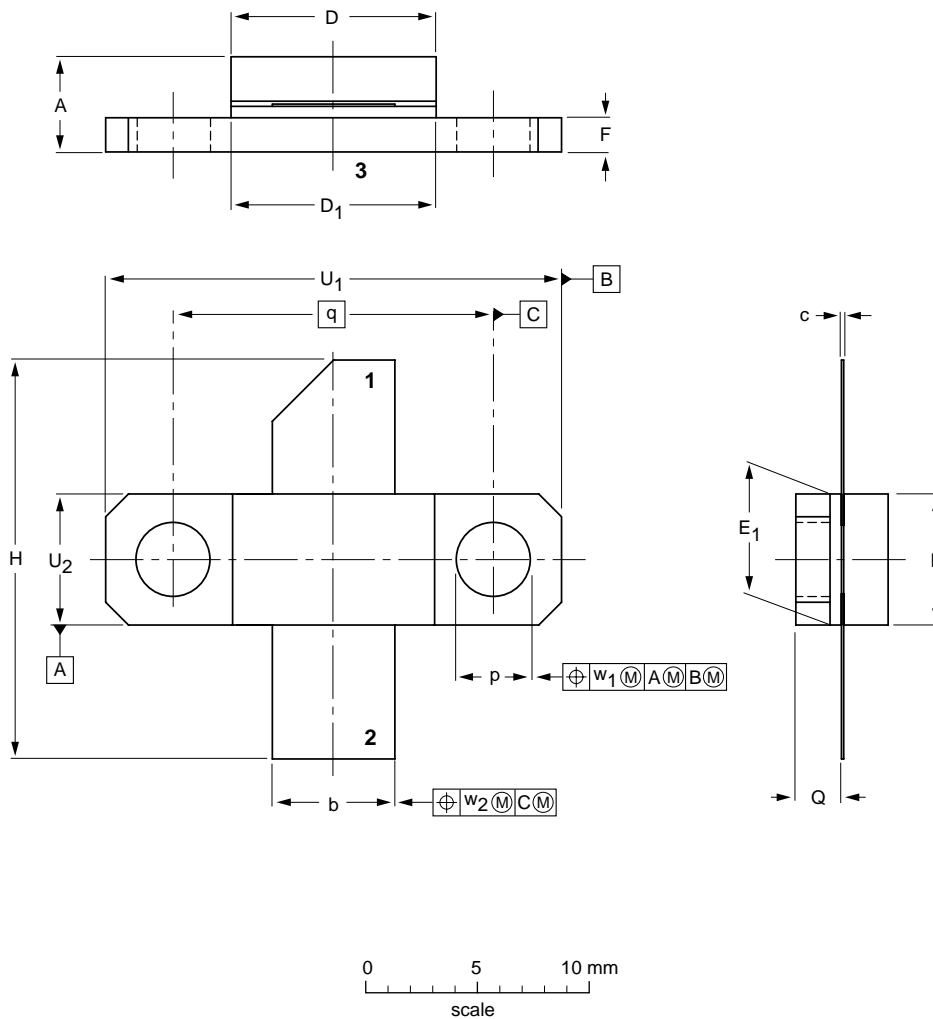
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

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DATA SHEET STATUS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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