

# DATA SHEET

## **BSP145**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC07

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**Philips Semiconductors**



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# N-channel enhancement mode vertical D-MOS transistor

**BSP145**

**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

**APPLICATIONS**

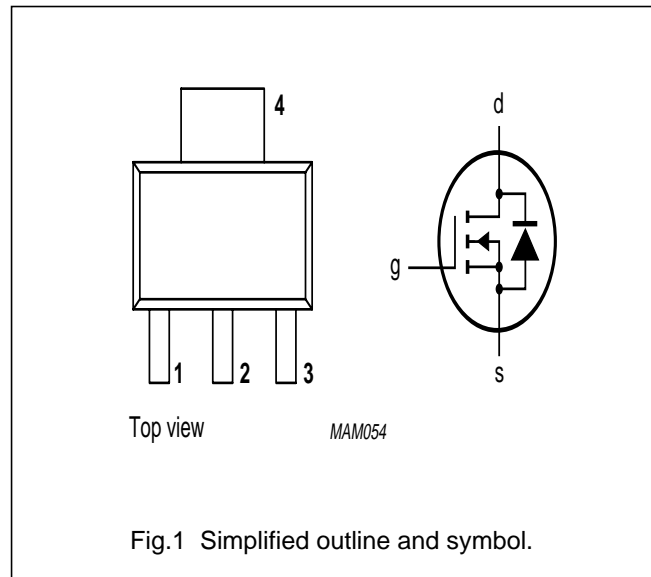
- Intended for applications in relay, high speed and line transformer drivers.

**DESCRIPTION**

N-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

**PINNING - SOT223**

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



**CAUTION**

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	450	V
$V_{GSO}$	gate-source voltage	open drain	–	$\pm 20$	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$	3	4	V
$I_D$	drain current		–	250	mA
$R_{DSon}$	drain-source on-state resistance	$I_D = 100 \text{ mA}; V_{GS} = 10 \text{ V}$	10	14	$\Omega$
$P_{tot}$	total power dissipation	up to $T_{amb} = 25 \text{ }^\circ\text{C}$	–	1.5	W

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	450	V
$V_{GSO}$	gate-source voltage	open drain	–	±20	V
$I_D$	drain current		–	250	mA
$I_{DM}$	peak drain current		–	1	A
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ °C}$ ; note 1	–	1.5	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	operating junction temperature		–	150	°C

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

**Note to the “Limiting values” and “Thermal characteristics”**

1. Device mounted on an epoxy printed-circuit board,  $40 \times 40 \times 1.5\text{ mm}$ ; mounting pad for drain lead minimum  $6\text{ cm}^2$ .

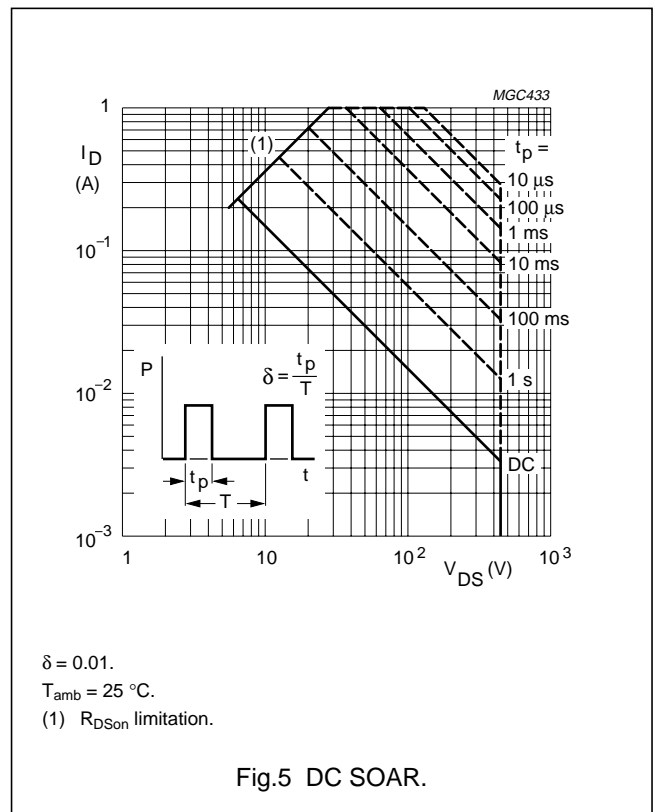
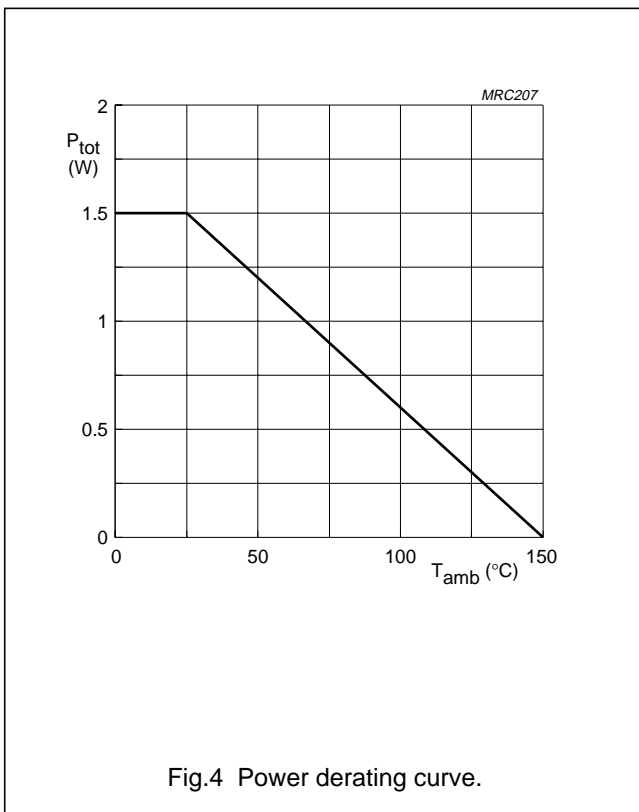
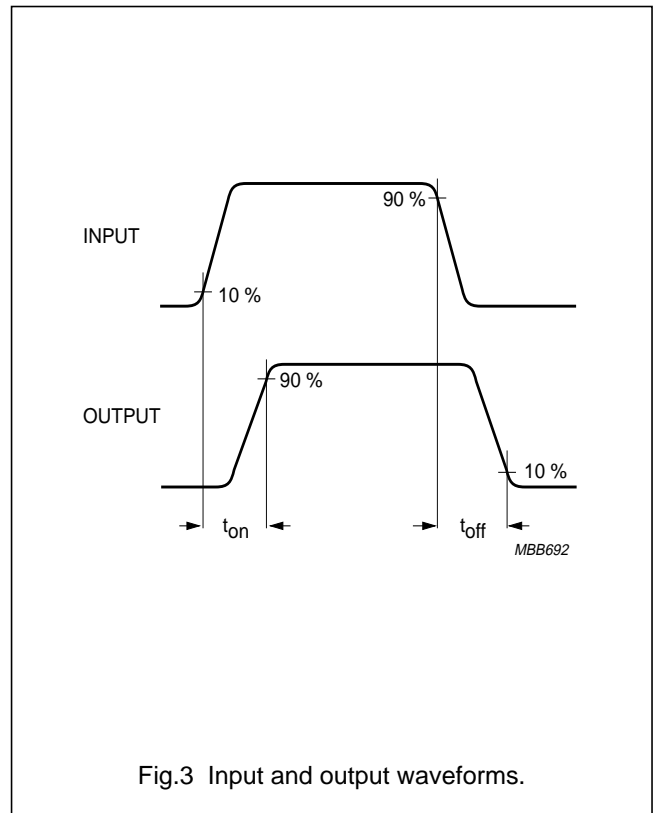
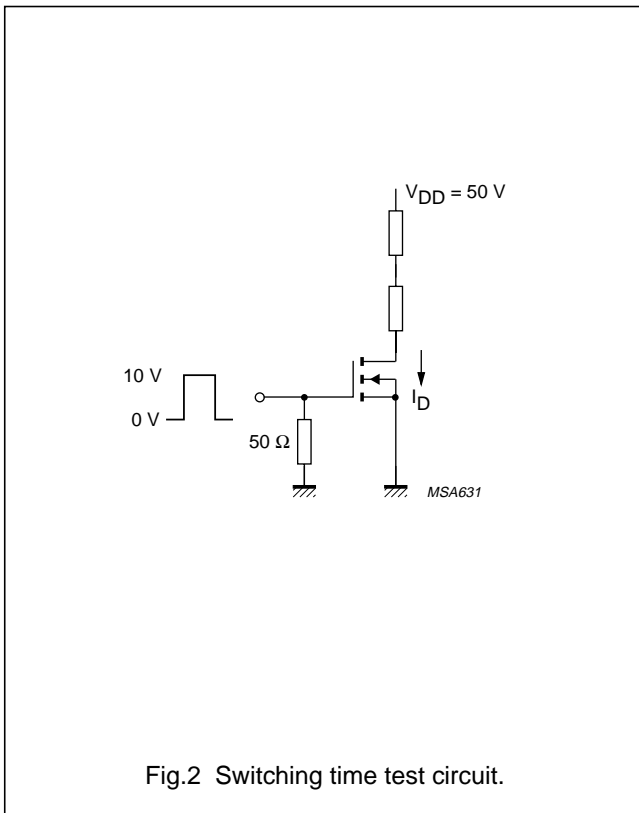
### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = 10\ \mu\text{A}$	450	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$	2	3	4	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = 350\text{ V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0$ ; $V_{GS} = \pm 20\text{ V}$	–	–	±100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 100\text{ mA}$	–	10	14	$\Omega$
$ y_{fs} $	forward transfer admittance	$V_{DS} = 25\text{ V}$ ; $I_D = 250\text{ mA}$	200	–	–	mS
$C_{iss}$	input capacitance	$V_{GS} = 0$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$	–	90	120	pF
$C_{oss}$	output capacitance	$V_{GS} = 0$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$	–	25	35	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$	–	2	5	pF
<b>Switching times</b> (see Figs 2 and 3)						
$t_{on}$	turn-on time	$V_{GS} = 0\text{ to }10\text{ V}$ ; $V_{DD} = 200\text{ V}$ ; $I_D = 100\text{ mA}$	–	–	10	ns
$t_{off}$	turn-off time	$V_{GS} = 10\text{ to }0\text{ V}$ ; $V_{DD} = 200\text{ V}$ ; $I_D = 100\text{ mA}$	–	–	100	ns

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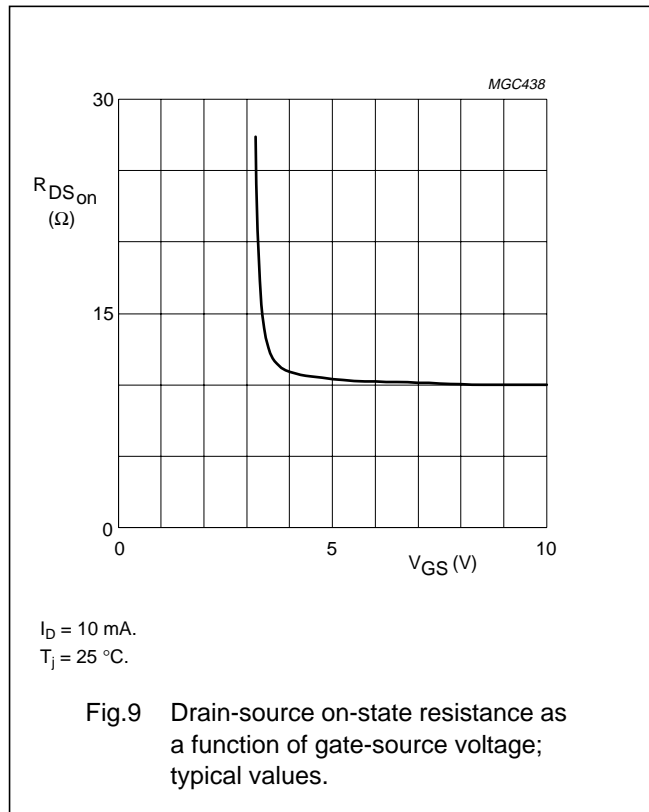
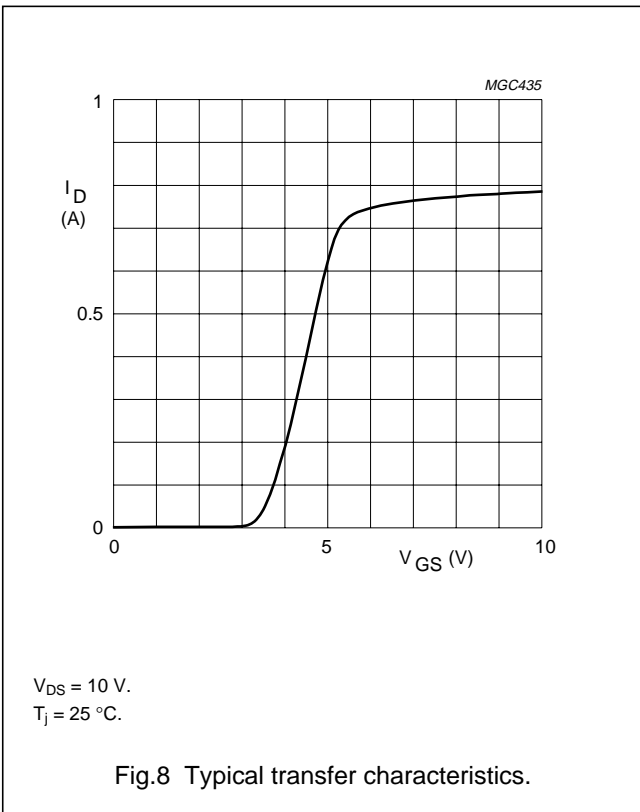
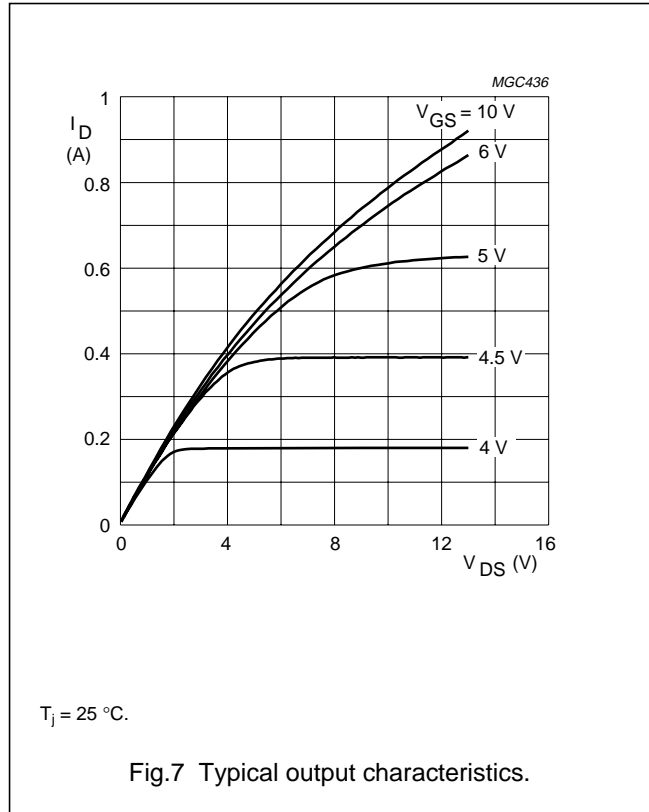
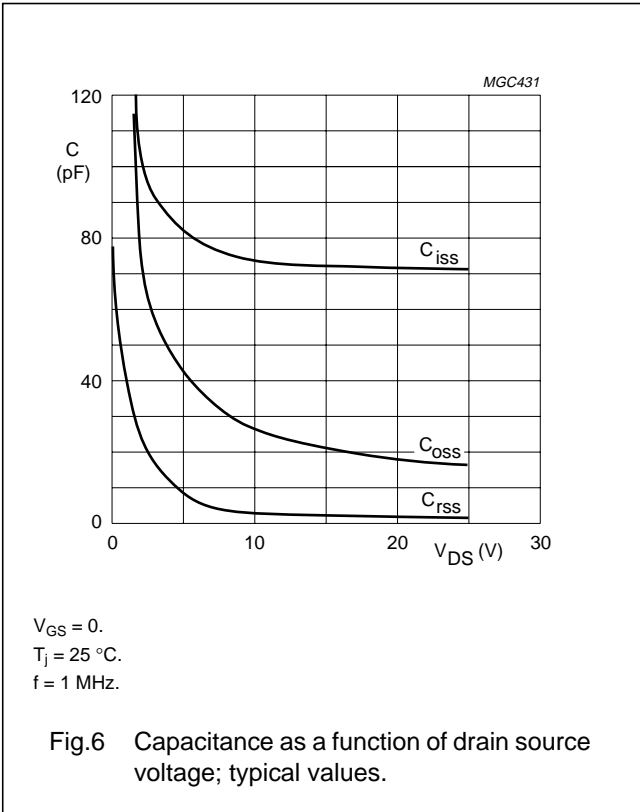
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$\delta = 0.01$ .  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
 (1)  $R_{DSon}$  limitation.

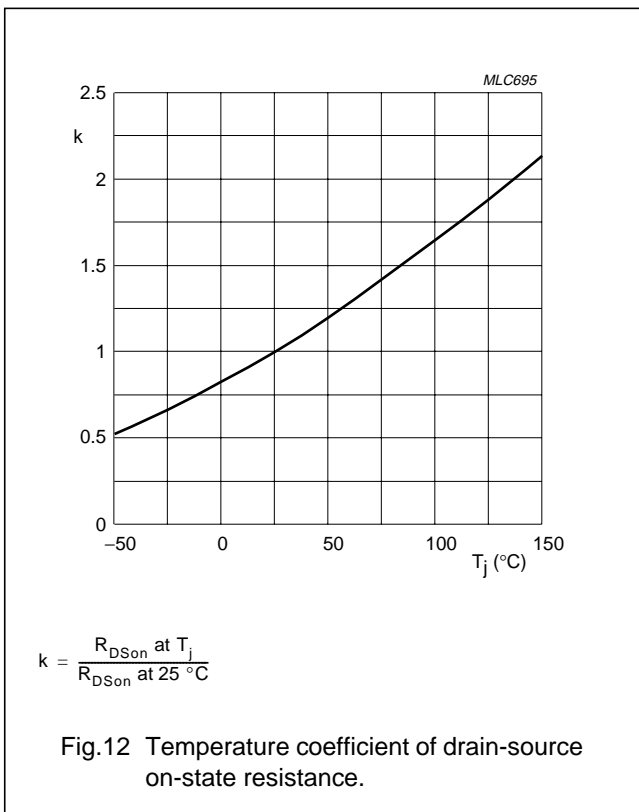
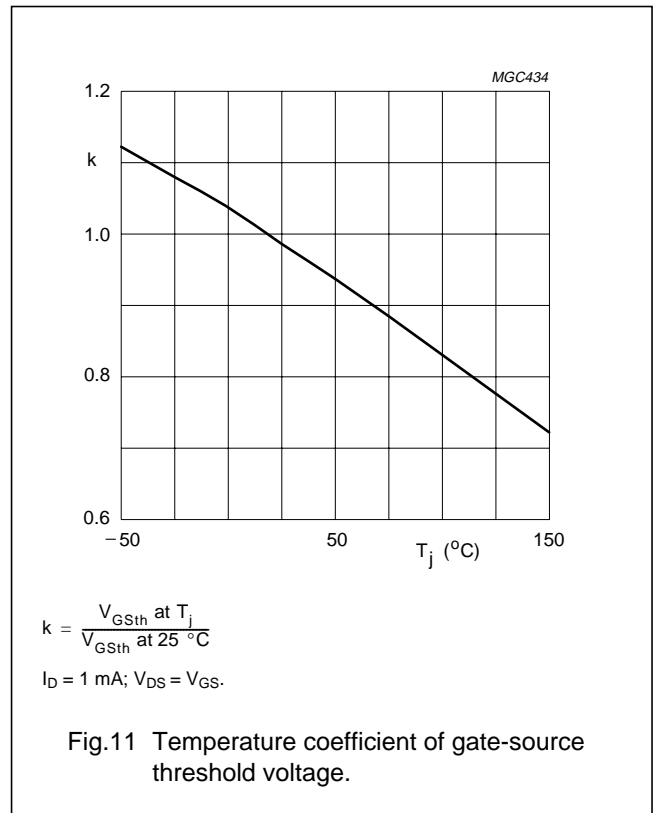
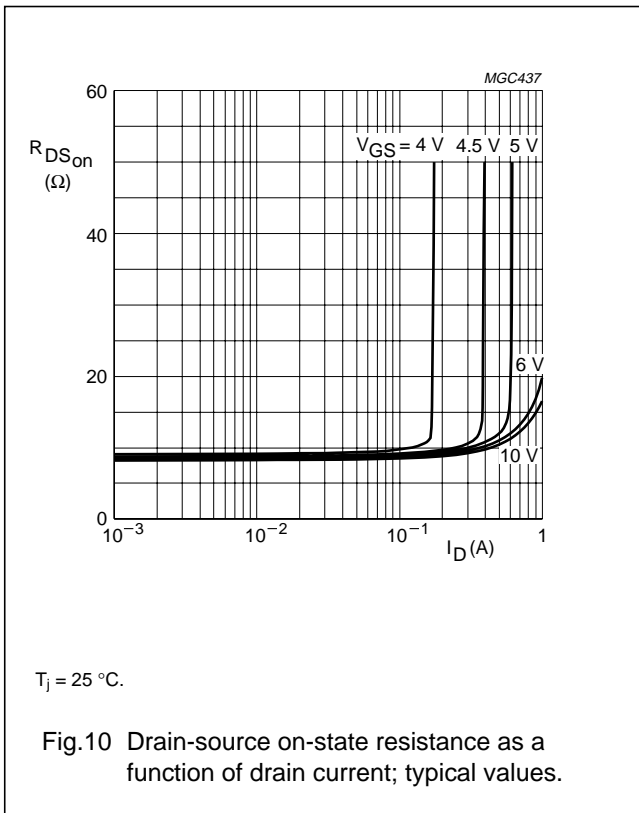
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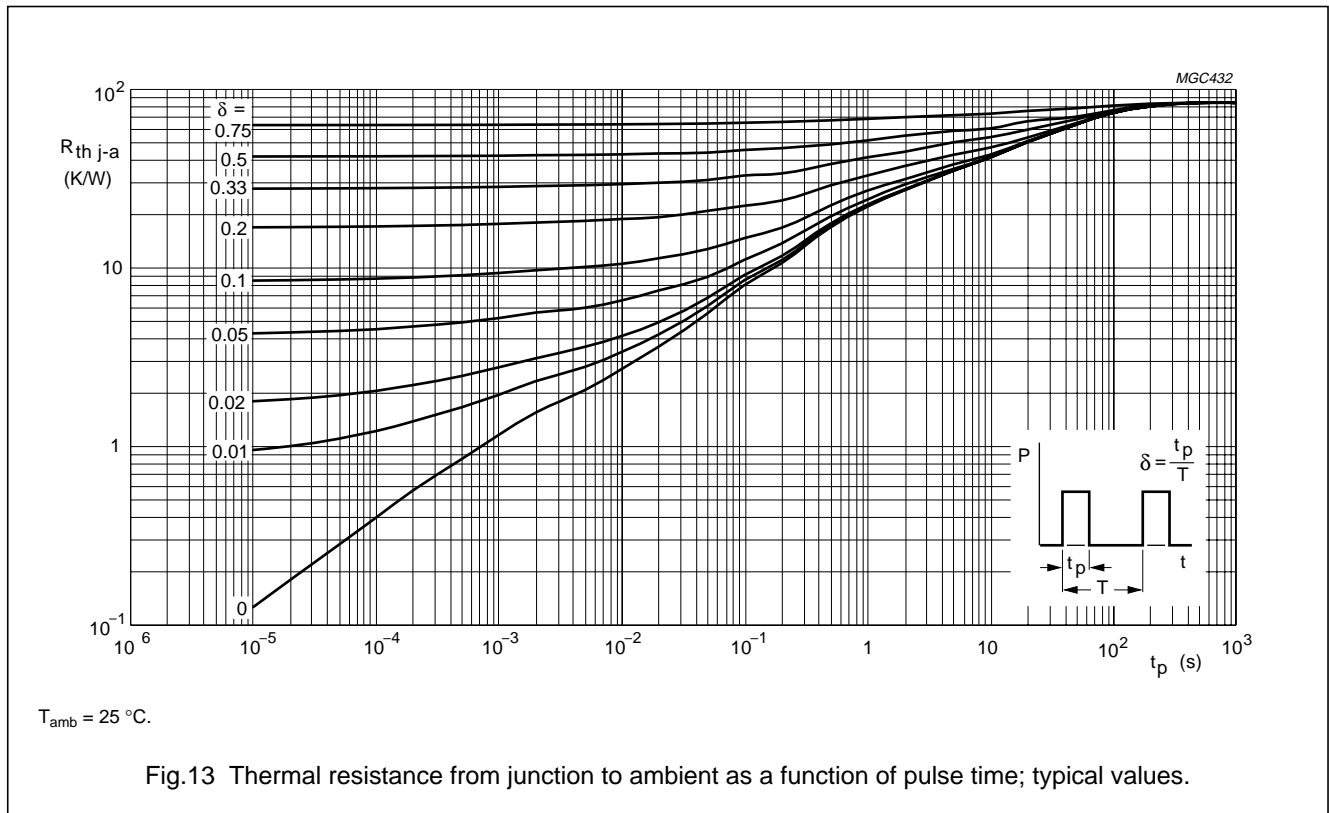
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# N-channel enhancement mode vertical D-MOS transistor

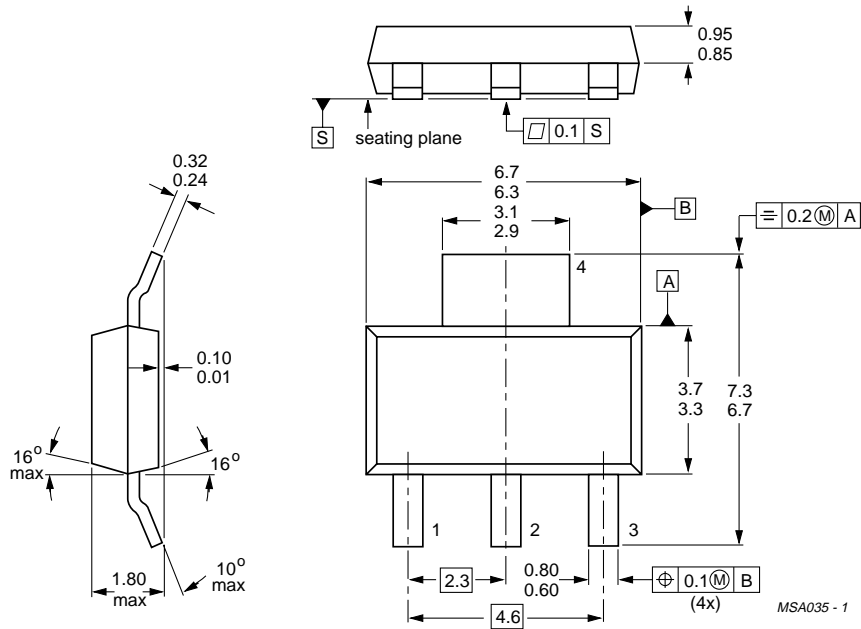
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PACKAGE OUTLINE



Dimensions in mm.

Fig.14 SOT223.



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## DEFINITIONS

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.