

DATA SHEET

BSP204; BSP204A P-channel enhancement mode vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

P-channel enhancement mode vertical D-MOS transistor

BSP204; BSP204A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

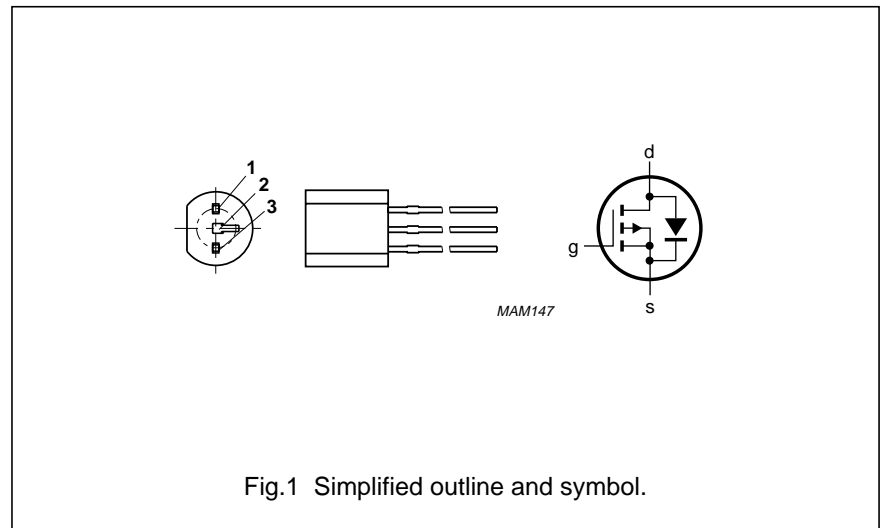
PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200 \text{ mA}$ $-V_{GS} = 10 \text{ V}$	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1 \text{ mA}$ $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ °C}$ (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

- Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	125	K/W

Note

- Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

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CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 160\ \text{V}$ $V_{GS} = 0$	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\ \text{V}$ $V_{DS} = 0$	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200\ \text{mA}$ $-V_{GS} = 10\ \text{V}$	–	10	15	Ω
$ Y_{fs} $	transfer admittance	$-I_D = 200\ \text{mA}$ $-V_{DS} = 25\ \text{V}$	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS} = 25\ \text{V}$ $-V_{GS} = 0$ $f = 1\ \text{MHz}$	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D = 250\ \text{mA}$ $-V_{DD} = 50\ \text{V}$ $-V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	5	10	ns
t_{off}	turn-off time	$-I_D = 250\ \text{mA}$ $-V_{DD} = 50\ \text{V}$ $-V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	20	30	ns

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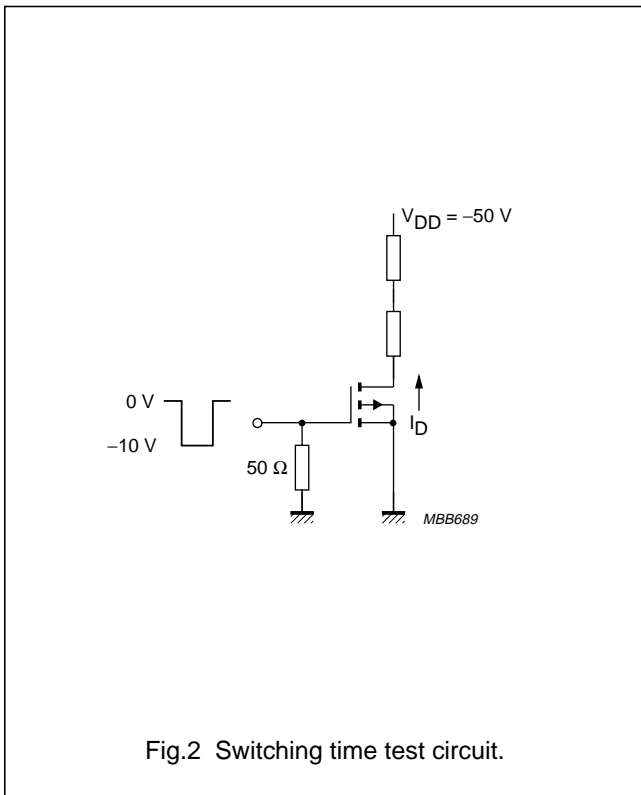


Fig.2 Switching time test circuit.

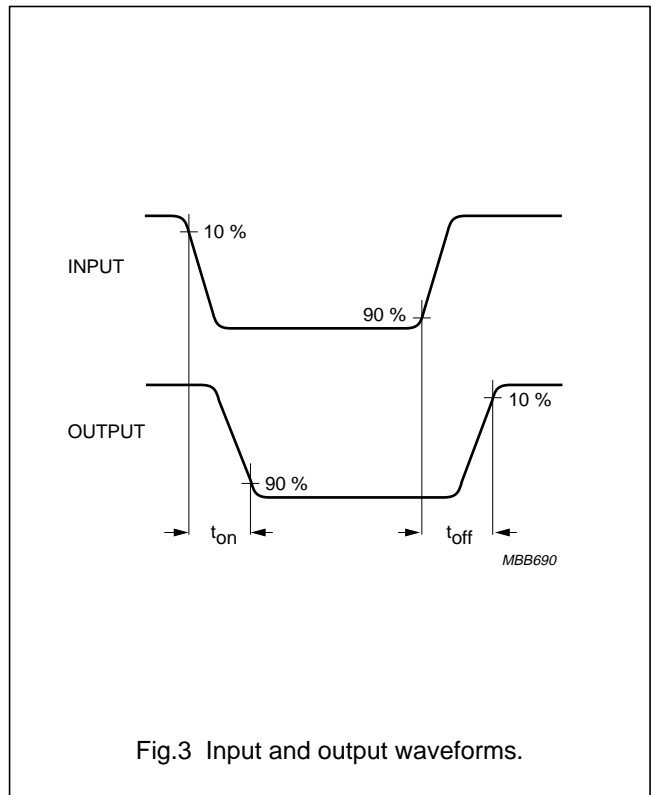


Fig.3 Input and output waveforms.

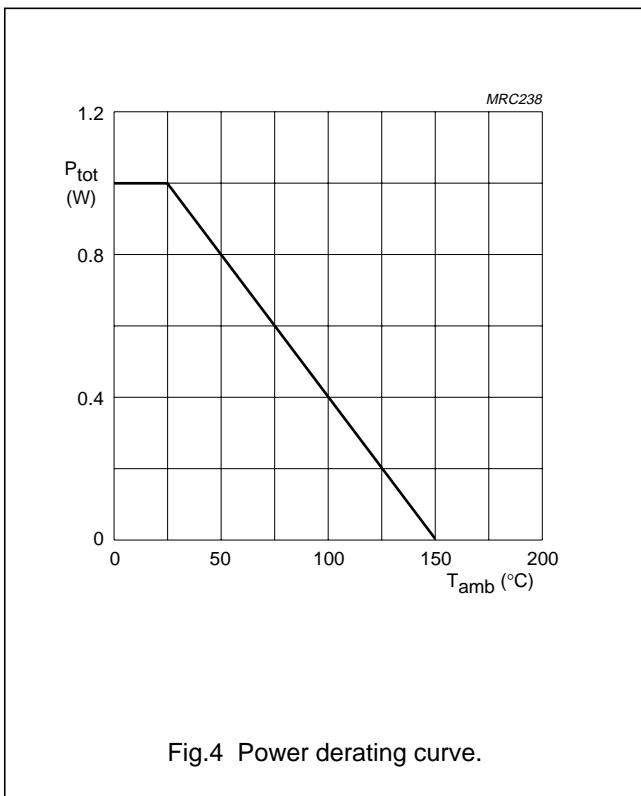


Fig.4 Power derating curve.

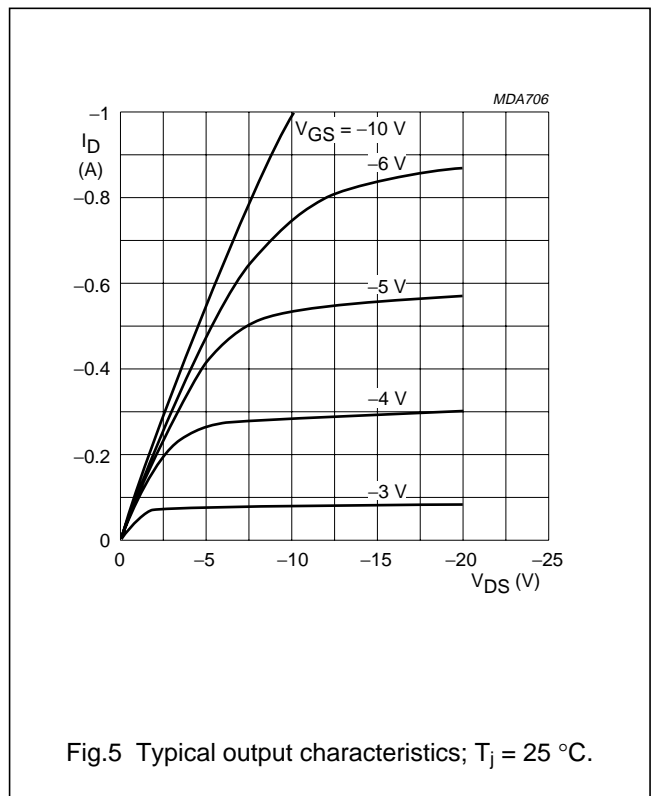
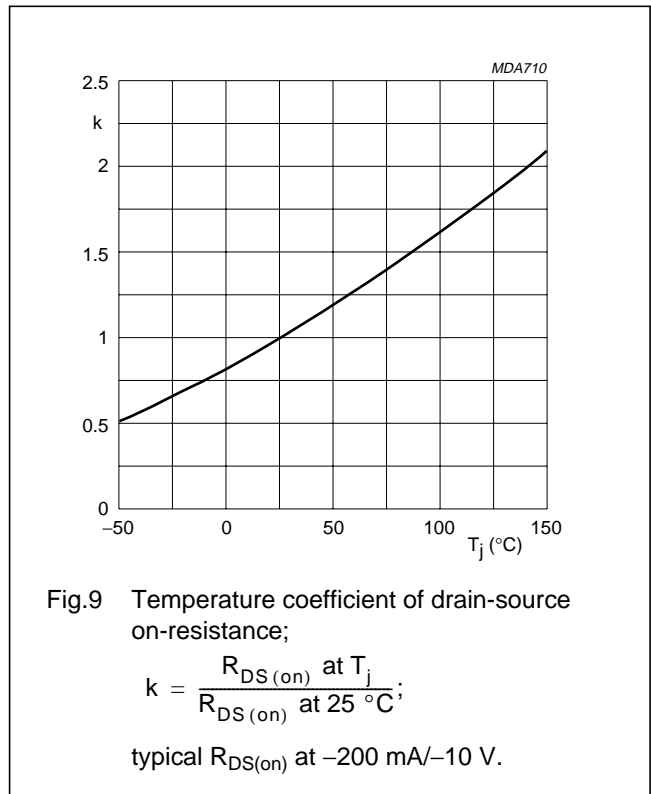
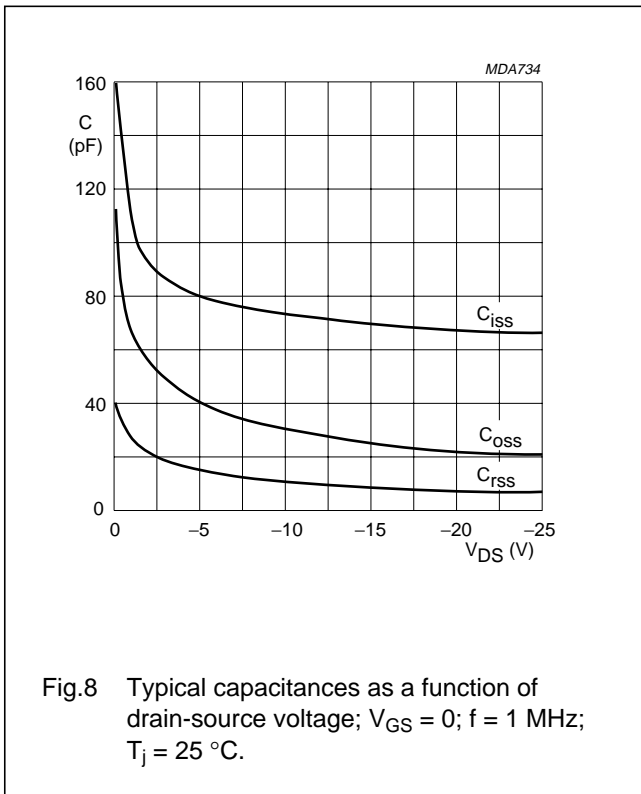
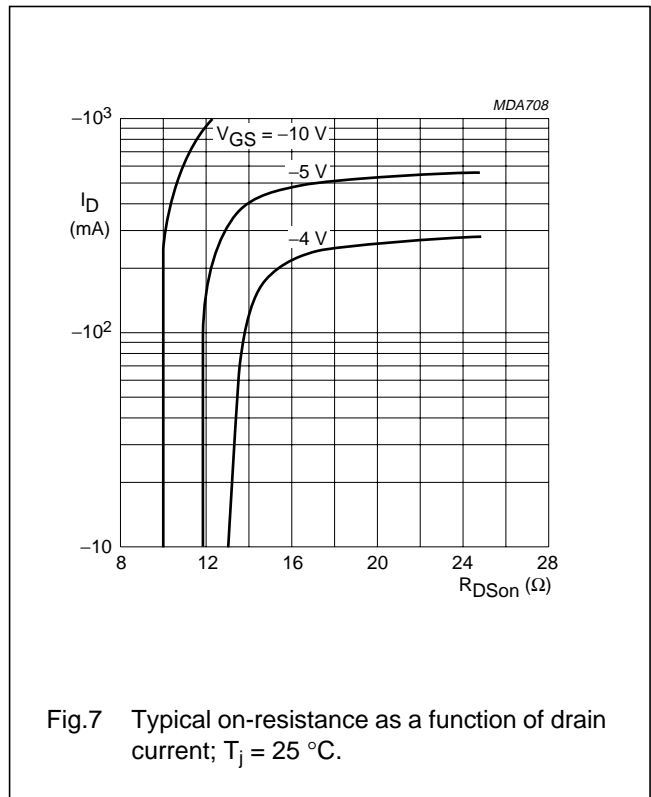
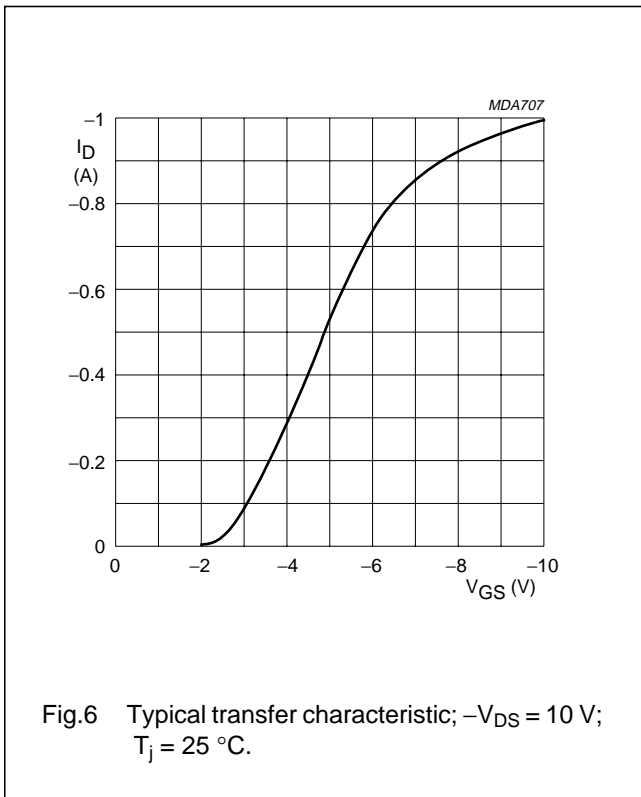


Fig.5 Typical output characteristics; Tj = 25 °C.

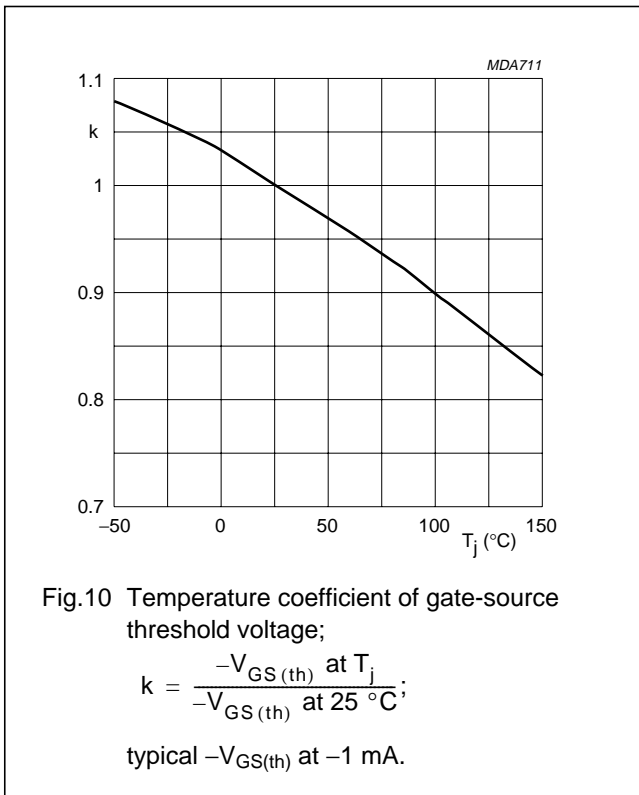
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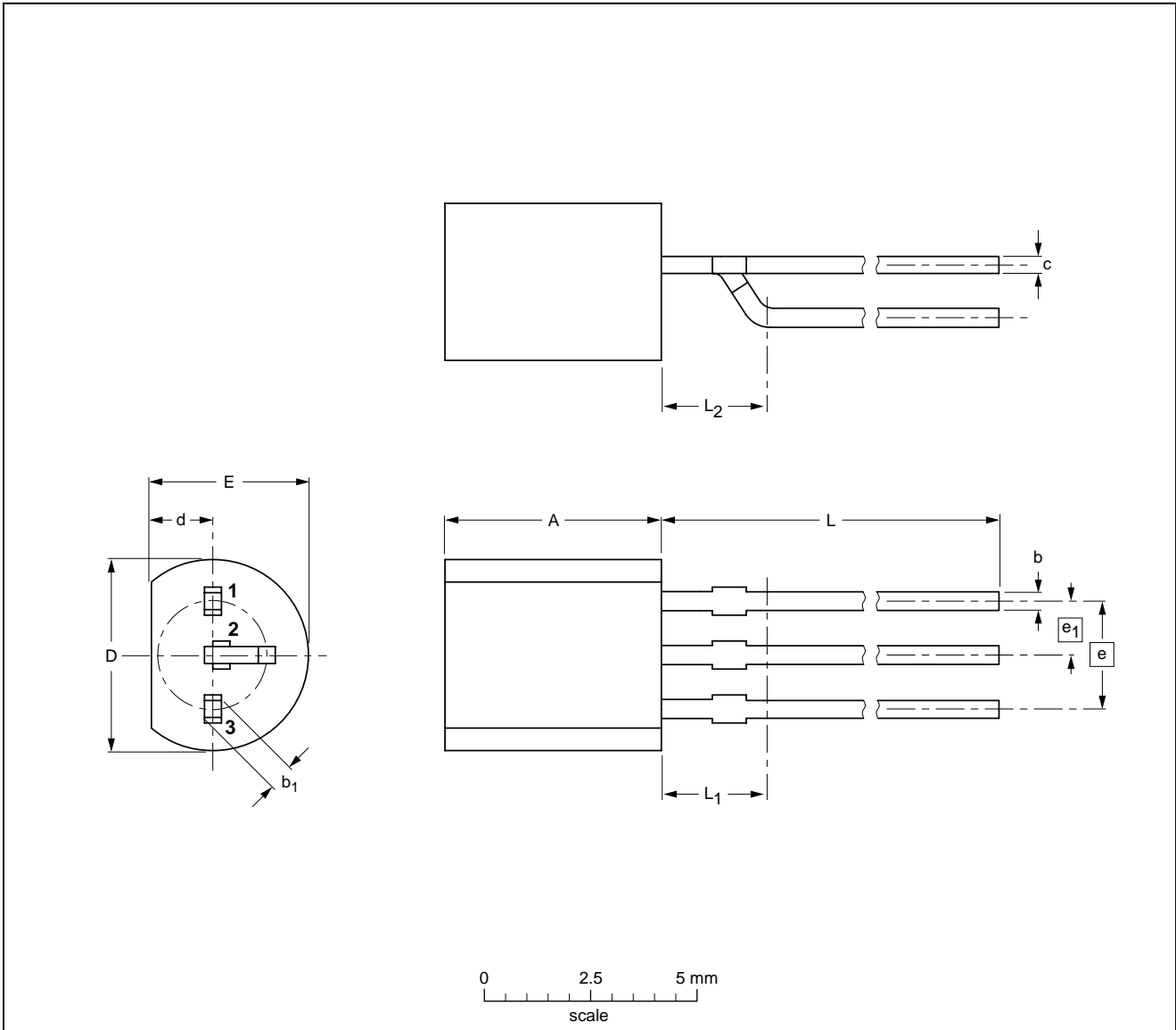
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max	L ₂ max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14

**P-channel enhancement mode vertical
D-MOS transistor**

BSP204; BSP204A**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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