Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt829A/827A

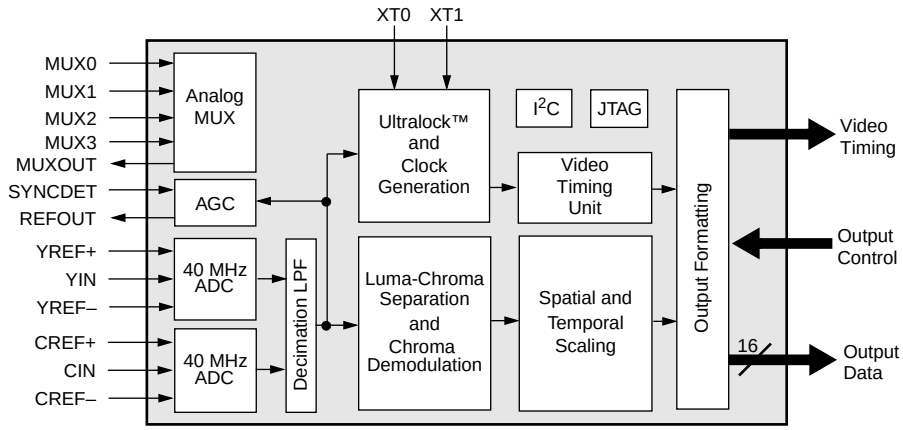
VideoStream II Decoders

Bt829A– *Video Capture Processor & Scaler for TV/VCR Analog Input*

Bt827A– *Composite Video and S-Video Decoder*

The Bt829A and Bt827A VideoStream™ Decoders are a family of single-chip, pin- and register-compatible, composite NTSC/PAL/SECAM video and S-Video decoders. They are also pin and register backward compatible with the Bt829/827 family of products. Low operating power consumption and power-down capability make them ideal low-cost solutions for PC video capture applications on both desktop and portable system platforms. They support square pixel and CCIR601 resolutions for NTSC, PAL and SECAM video. They have a flexible pixel port which supports a variety of system interface configurations, and they are offered in 100-pin PQFP and 100-pin TQFP packages.

Functional Block Diagram



Distinguishing Features

- Single-chip composite/S-Video NTSC/PAL/SECAM to YCrCb digitizer
- On-chip Ultralock™
- Square pixel and CCIR601 resolution for:
  - NTSC (M)
  - NTSC (M) without 7.5IRE pedestal
  - PAL (B, D, G, H, I, M, N, N combination)
  - SECAM
- Chroma comb filter
- Arbitrary horizontal and 5-tap vertical filtered scaling
- Hardware closed-caption decoder
- Vertical Blanking Interval (VBI) data pass-through
- Arbitrary temporal decimation for a reduced frame-rate video sequence
- Programmable hue, brightness, saturation, and contrast
- User-programmable cropping of the video window
- 2x oversampling to simplify external analog filtering
- Two-wire Inter-Integrated Circuit (I^2C) bus interface
- 8- or 16-bit pixel interface
- YCrCb (4:2:2) output format
- Software selectable four-input analog MUX
- 4 fully programmable GPIO bits
- Auto NTSC/PAL format detect
- Automatic Gain Control (AGC)
- Typical power consumption 0.85 W
- IEEE 1149.1 Joint Test Action Group (JTAG) interface
- 100-Pin PQFP and TQFP packages

Related Products

- Bt819A, Bt829, Bt856/857, Bt864/865, Bt866/867, Bt852

Applications

- Multimedia
- Image processing
- Desktop video
- Video phone
- Teleconferencing
- Interactive video

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt829AKRF	100-pin PQFP	0˚C to +70˚C
Bt827AKRF	100-pin PQFP	0˚C to +70˚C
Bt829AKTF	100-pin TQFP	0˚C to +70˚C

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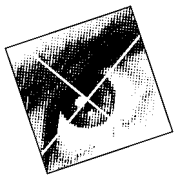
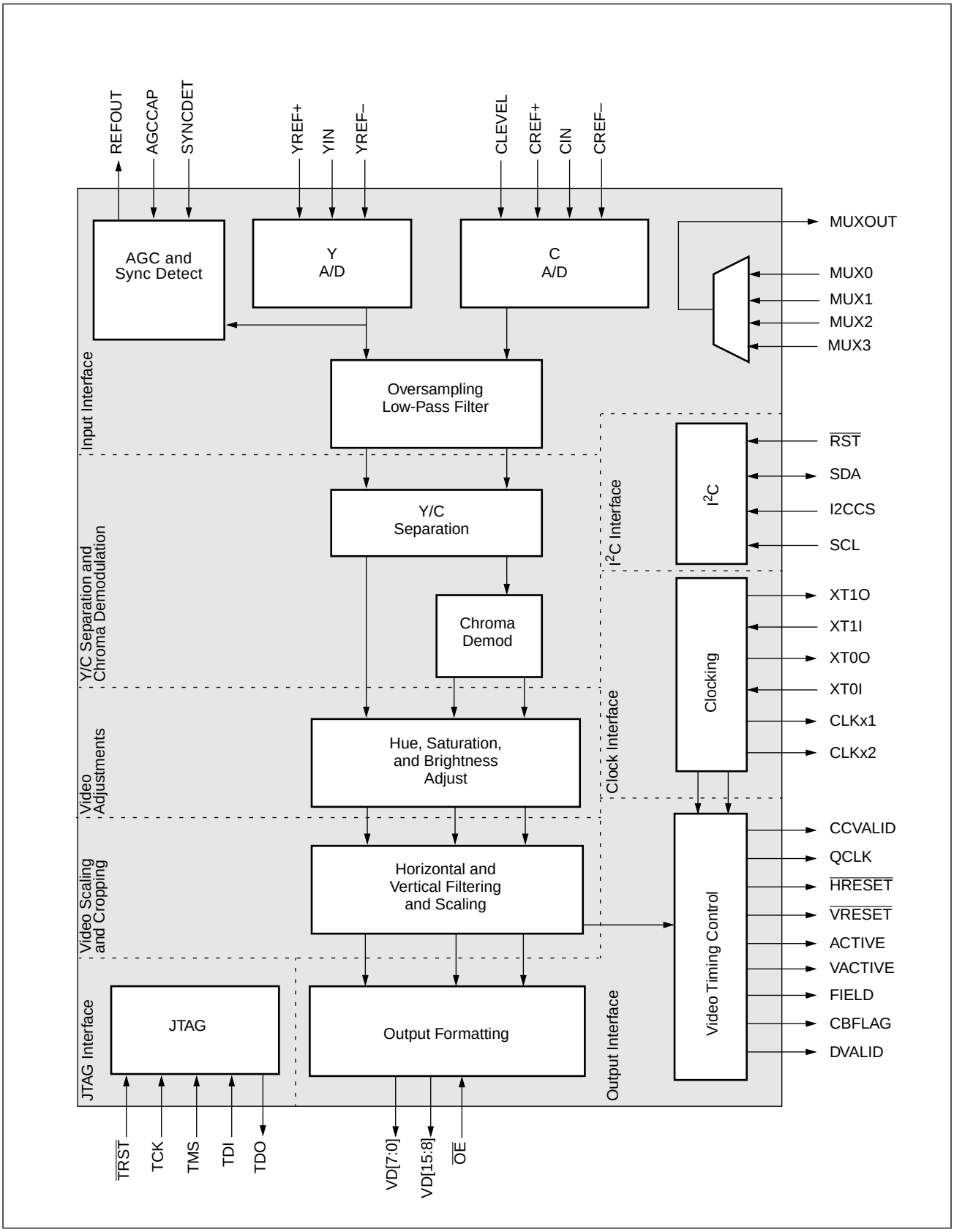


FUNCTIONAL DESCRIPTION

Functional Overview

Rockwell's VideoStream™ II products are a family of single-chip, pin-and register-compatible solutions for processing analog NTSC/PAL/SECAM video into digital 4:2:2 YCrCb video. They provide a comprehensive choice of capabilities to enable the feature set and cost to be tailored to different system hardware configurations. All solutions are housed in a 100-pin QFP package. A detailed block diagram is shown in Figure 1.

Figure 1. Bt829A/827A Detailed Block Diagram



Bt829A Video Capture Processor for TV/VCR Analog Input

The Bt829A Video Capture Processor is a fully integrated single-chip decoding and scaling solution for analog NTSC/PAL/SECAM input signals from TV tuners, VCRs, cameras, and other sources of composite or Y/C video. It is the second generation front-end input solution for low-cost PC video/graphics systems that deliver complete integration and high-performance video synchronization, Y/C separation, and filtered scaling. The Bt829A has all the mixed signal and DSP circuitry required to convert an analog composite waveform into a scaled digital video stream, supporting a variety of video formats, resolutions, and frame rates.

Bt827A Composite/S-Video Decoder

The Bt827A provides full composite and S-Video capability along with filtered horizontal scaling. Vertical scaling can only be implemented by line-dropping.

The Synchronous Pixel Interface (SPI) is common to both pin-compatible devices, which enables implementation of a single system hardware design. Similarly, a common I^2C register set allows a single piece of driver code to be written for software control of both options. Table 1 compares Bt829A and Bt827A features.

Table 1. VideoStream™ II Features Options

Feature Options	Bt829A	Bt827A
Composite Video Decoding	X	X
S-Video Decoding	X	X
SECAM Video	X	X
Hardware Closed Caption Decode	X	X
Filtered Vertical Scaling	X	

Bt829A Architecture and Partitioning

The Bt829A has been developed to provide the most cost-effective, high-quality video input solution for low-cost multimedia subsystems that integrate both graphics display and video capabilities. The feature set of the Bt829A supports a video/graphics system partitioning which optimizes the total cost of a system configured both with and without video capture capabilities. This enables system vendors to easily offer products with various levels of video support using a single base-system design.

As graphics chip vendors move from graphics-only to video/graphics coprocessors and eventually to single-chip video/graphics processor implementations, the ability to efficiently use silicon and package pins to support both graphics acceleration, video playback acceleration, and video capture becomes critical. This problem becomes more acute as the race towards higher performance graphics requires more and more package pins to be consumed for wide 64-bit memory interfaces and glueless local bus interfaces.

The Bt829A minimizes the cost of video capture function integration in two ways. First, recognizing that YCrCb to RGB color space conversion is a required feature of multimedia controllers for acceleration of digital video playback, the Bt829A avoids redundant functionality and allows the downstream controller to perform this task. Second, the Bt829A can minimize the number of interface pins required by a downstream multimedia controller in order to keep package costs to a minimum.

Controller systems designed to take advantage of these features allow video capture capability to be added to the base system in a modular fashion using only a single Integrated Circuit (IC).

The Bt827A is targeted at system configurations using video processors which typically integrate the scaling function.

UltraLock™

The Bt829A and Bt827A employ a proprietary technique known as UltraLock™ to lock to the incoming analog video signal. It will always generate the required number of pixels per line from an analog source in which the line length can vary by as much as a few microseconds. UltraLock™'s digital locking circuitry enables the VideoStream™ decoders to quickly and accurately lock on to video signals, regardless of their source. Since the technique is completely digital, UltraLock™ can recognize unstable signals caused by VCR headswitches or any other deviation and adapt the locking mechanism to accommodate the source. UltraLock™ uses nonlinear techniques which are difficult, if not impossible, to implement in genlock systems. And unlike linear techniques, it adapts the locking mechanism automatically.

Scaling and Cropping

The Bt829A can reduce the video image size in both horizontal and vertical directions independently using arbitrarily selected scaling ratios. The X and Y dimensions can be scaled down to one-sixteenth of the full resolution. Horizontal scaling is implemented with a 6-tap interpolation filter, while up to 5-tap interpolation is used for vertical scaling with a line store. The Bt827A supports vertical scaling by line-dropping.

The video image can be arbitrarily cropped by programming the ACTIVE flag to reduce the number of active scan lines and active horizontal pixels per line.

The Bt829A and Bt827A also support a temporal decimation feature that reduces video bandwidth by allowing frames or fields to be dropped from a video sequence at regular but arbitrarily selected intervals.

Input Interface

Analog video signals are input to the Bt829A/827A via a four-input multiplexer that can select between four composite source inputs or between three composite and a single S-Video input source. When an S-Video source is input to the Bt829A, the luma component is fed through the input analog multiplexer, and the chroma component is fed directly into the C input pin. An AGC circuit enables the Bt829A/827A to compensate for reduced amplitude in the analog signal input.

The clock signal interface consists of two pairs of pins for crystal connection and two clock output pins. One pair of crystal pins is for connection to a 28.64 MHz (8*NTSC Fsc) crystal which is selected for NTSC operation. The other is for PAL operation with a 35.47 MHz (8*PAL Fsc) crystal. Either of the two crystal frequencies can be selected to generate CLKx1 and CLKx2 output signals. CLKx2 operates at the full crystal frequency (8*Fsc) whereas CLKx1 operates at half the crystal frequency (4*Fsc). Either fundamental or third harmonic crystals may be used. Alternatively, CMOS oscillators may be used.

Output Interface

The Bt829A and Bt827A support a Synchronous Pixel Interface (SPI) mode.

The SPI supports a YCrCb 4:2:2 data stream over an 8- or 16-bit-wide path. When the pixel output port is configured to operate 8 bits wide, 8 bits of chrominance data are output on the first clock cycle followed by 8 bits of luminance data on the next clock cycle for each pixel. Two clocks are required to output one pixel in this mode, thus a 2x clock is used to output the data.

The Bt829A/827A outputs all horizontal and vertical blanking pixels in addition to the active pixels synchronous with CLKX1 (16-bit mode) or CLKX2 (8-bit mode). It is also possible to insert control codes into the pixel stream using chrominance and luminance values that are outside the allowable chroma and luma ranges. These control codes can be used to flag video events such as ACTIVE, HRESET, and VRESET. Decoding these video events downstream enables the video controller to eliminate pins required for the corresponding video control signals.

VBI Data Pass-through

The Bt829A/827A provides VBI data passthrough capability. The VBI region ancillary data is captured by the video decoder and made available to the system for subsequent software processing. The Bt829A/827A may operate in a VBI Line Output mode, in which the VBI data is only made available during select lines. This mode of operation is intended to enable capture of VBI lines containing ancillary data as well as processing normal YCrCb video image data. In addition, the Bt829A/827A supports a VBI Frame Output mode, in which every line in the video signal is treated as if it was a vertical interval line and no image data is output. This mode of operation is designed for use in still-frame capture/processing applications.

Closed Caption Decoding

The Bt829A and Bt827A provide a Closed Captioning (CC) and Extended Data Services (EDS) decoder. Data presented to the video decoder on the CC and EDS lines is decoded and made available to the system through the CC_DATA and CCSTATUS registers.

I^2C Interface

The Bt829A/827A registers are accessed via a two-wire I^2C interface. The Bt829A/827A operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate of 100 Kbits/s. Chip select and reset signals are also available to select one of two possible Bt829A/827A devices in the same system and to set the registers to their default values.

Pin Descriptions

Figure 2 details the Bt829A and Bt827A pinout. Table 2 provides pin numbers, names, input and output functions, and descriptions.

Figure 2. Bt829A/7A Pinout

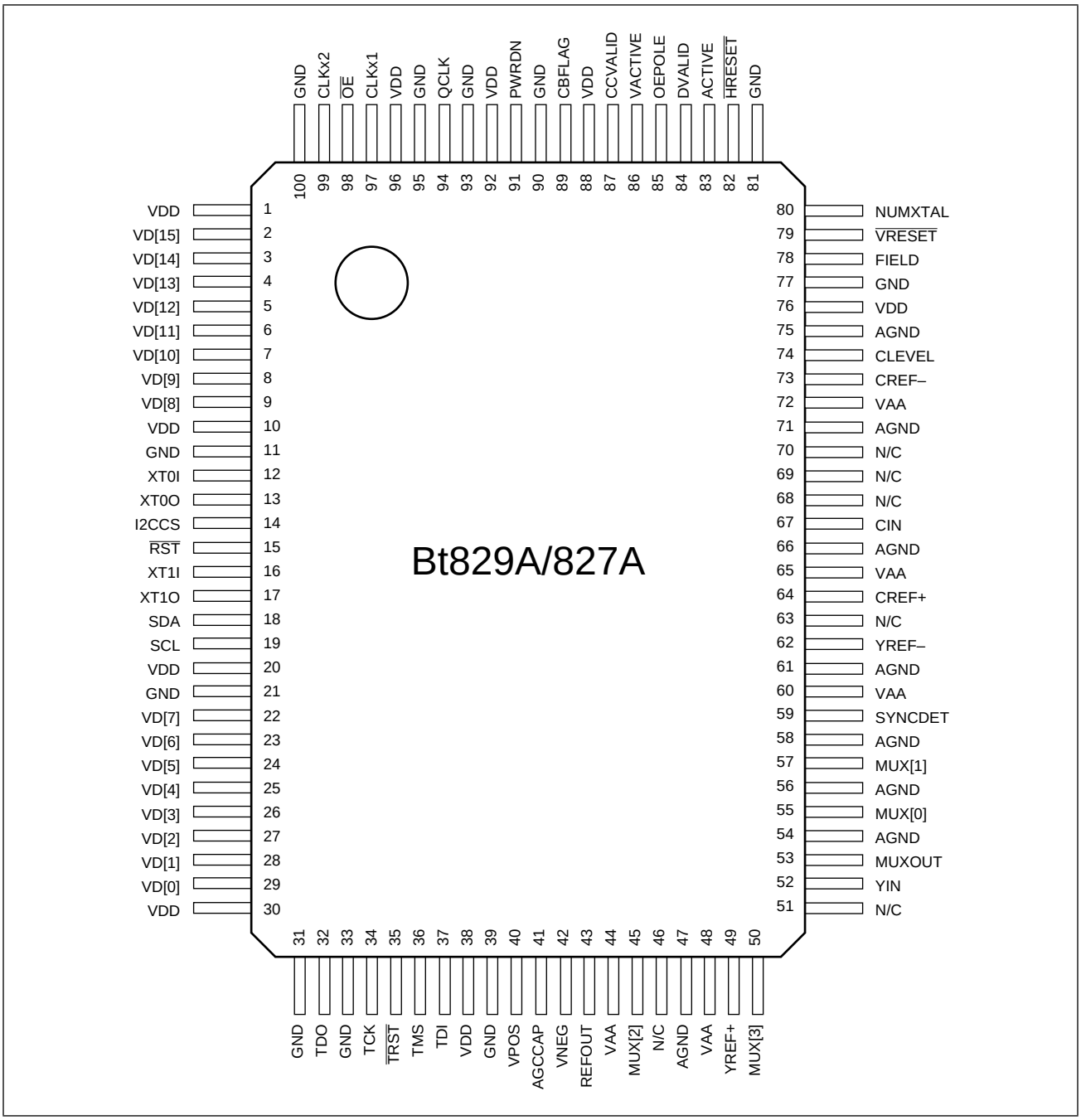


Table 2. Pin Descriptions Grouped By Pin Function *(1 of 4)*

Pin #	I/O	Pin Name	Description
Input Stage Pins			
45, 50, 55, 57	I	MUX[3:0]	Analog composite video inputs to the on-chip input multiplexer. They are used to select between four composite sources or three composite and one S-Video source. Unused pins should be connected to GND.
53	O	MUXOUT	The analog video output of the 4-to-1 multiplexer. Connected to the YIN pin.
52	I	YIN	The analog composite or luma input to the Y-ADC.
67	I	CIN	The analog chroma input to the C-ADC.
59	I	SYNCDET	The sync stripper input generates timing information for the AGC circuit. Can be optionally connected through a 0.1 µF capacitor to the same source as the Y-ADC, to maintain compatibility with Bt829 board layouts. A 1 MΩ bleeder resistor can be connected to ground, to maintain compatibility with Bt829 board layouts. For new Bt829A designs, this pin may be connected to VAA.
41	A	AGCCAP	The AGC time constant control capacitor node. Must be connected to a 0.1 µF capacitor to ground.
43	O	REFOUT	Output of the AGC which drives the YREF+ and CREF+ pins.
49	A	YREF+	The top of the reference ladder of the Y-ADC. This should be connected to REFOUT.
62	A	YREF–	The bottom of the reference ladder of the Y-ADC. This should be connected to analog ground (AGND).
64	A	CREF+	The top of the reference ladder of the C-ADC. This should be connected to REFOUT.
73	A	CREF–	The bottom of the reference ladder of the C-ADC. This should be connected to analog ground (AGND).
74	A	CLEVEL	An input to provide the DC level reference for the C-ADC. For compatibility with Bt829 board layouts, the 30 kΩ divider resistors may be maintained. Note: This pin should be left to float for new Bt829A designs.
51	A	N/C	No connect.
46	A	N/C	No connect.
63, 68	A	N/C	No connect.
70	A	N/C	No connect.
69	A	N/C	No connect.
I^2C Interface Pins			
19	I	SCL	The I^2C Serial Clock Line.
18	I/O	SDA	The I^2C Serial Data Line.
14	I	I2CCS	The I^2C Chip Select Input (TTL compatible). This pin selects one of two Bt829A devices in the same system. This pin is internally pulled to ground with an effective 18 KΩ resistance.
15	I	$\overline{RST}$	Reset Control Input (TTL compatible). A logical zero for a minimum of four consecutive clock cycles resets the device to its default state. A logical zero for less than eight XTAL cycles will leave the device in an undetermined state.

Table 2. Pin Descriptions Grouped By Pin Function *(2 of 4)*

Pin #	I/O	Pin Name	Description
Video Timing Unit Pins			
82	O	$\overline{\text{HRESET}}$	Horizontal Reset Output (TTL compatible). This signal indicates the beginning of a new line of video. This signal is 64 CLKx1 clock cycles wide. The falling edge of this output indicates the beginning of a new scan line of video. This pin may be defined in pixels as opposed to CLKx1 cycles. Refer to the HSFMT bit in the VTC register. Note: The polarity of this pin is programmable through the VPOLE register.
79	O	$\overline{\text{VRESET}}$	Vertical Reset Output (TTL compatible). This signal indicates the beginning of a new field of video. This signal is output coincident with the rising edge of CLKx1, and is normally six lines wide. The falling edge of $\overline{\text{VRESET}}$ indicates the beginning of a new field of video. Note: The polarity of this pin is programmable through the VPOLE register.
83	O	ACTIVE	Active Video Output (TTL compatible). This pin can be programmed to output the composite active or horizontal active signal via the VTC register. It is a logical high during the active/viewable periods of the video stream. The active region of the video stream is programmable. Note: The polarity of this pin is programmable through the VPOLE register.
94	O	QCLK	Qualified Clock Output. This pin provides a rising edge only during valid, active pixel data. This output is generated from CLKx1 (or CLKx2 in 8-bit mode), DVALID and, if programmed, ACTIVE. The phase of QCLK is inverted from the CLKx1 (or CLKx2) to ensure adequate setup and hold time with respect to the data outputs. QCLK is not output during control codes when using SPI mode 2.
98	I	OE	Output Enable Control (TTL compatible). All video timing unit output pins and all clock interface output pins contain valid data following the rising edge of CLKx2, after $\overline{\text{OE}}$ has been asserted low. This function is asynchronous. The three-stated pins include: VD[15:0], $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$, ACTIVE, DVALID, CBFLAG, FIELD, QCLK, CLKx1, and CLKx2. See the OES bits in the OFORM register to disable subgroups of output pins.
78	O	FIELD	Odd/Even Field Output (TTL compatible). A high state on the FIELD pin indicates that an odd field is being digitized. Note: The polarity of this pin is programmable through the VPOLE register.
89	O	CBFLAG	Cb Data Identifier (TTL compatible). A high state on this pin indicates that the current chroma byte contains Cb chroma information. Note: The polarity of this pin is programmable through the VPOLE register.
2–9	O	VD[15:8]	Digitized Video Data Outputs (TTL compatible). VD[0] is the least significant bit of the bus in 16-bit mode. VD[8] is the least significant bit of the bus in 8-bit mode. The information is output with respect to CLKx1 in 16-bit mode, and CLKx2 in 8-bit mode. In mode 2, this port is configured to output control codes as well as data. When data is output in 8-bit mode using VD[15:8], VD[7:0] can be used as general purpose I/O pins. See the P_IO register.
22–29	I/O	VD[7:0]	
84	O	DVALID	Data Valid Output (TTL compatible). This pin indicates when a valid pixel is being output onto the data bus. The Bt829A digitizes video at eight times the subcarrier rate, and outputs scaled video. Therefore, there are more clocks than valid data. DVALID indicates when valid pixel data is being output. Note: The polarity of this pin is programmable through the VPOLE register.

Table 2. Pin Descriptions Grouped By Pin Function *(3 of 4)*

Pin #	I/O	Pin Name	Description
87	O	CCVALID	A logical low on this pin indicates that the CC FIFO is half full (8 characters). This pin may be disabled. This open drain output *requires* a pullup resistor for proper operation. However, if closed captioning is not implemented, this pin may be left unconnected.
91	I	PWRDN	A logical high on this pin puts the device into power-down mode. This is equivalent to programming CLK_SLEEP high in the ADC register.
86	O	VACTIVE	Vertical Blanking Output (TTL compatible). The falling edge of VACTIVE indicates the beginning of the active video lines in a field. This occurs VDELAY/2 lines after the rising edge of $\overline{\text{VRESET}}$. The rising edge of VACTIVE indicates the end of active video lines and occurs ACTIVE_LINES/2 lines after the falling edge of VACTIVE. VACTIVE is output following the rising edge of CLKx1. Note: The polarity of the pin is programmable through the VPOLE register.
85	I	OEPOLE	A logical low on this pin allows the Bt829A/827A to power up in the same manner as the Bt829/827. A logical high on this pin, followed by a device reset will TRISTATE the video outputs, sync outputs and clock outputs.
Clock Interface Pins			
12	A	XT0I	Clock Zero pins. A 28.64 MHz (8*Fsc) fundamental (or third harmonic) crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XT0I. CMOS level inputs must be used. This clock source is selected for NTSC input sources. When the chip is configured to decode PAL but not NTSC (and therefore only one clock source is needed), the 35.47 MHz source is connected to this port (XT0).
13	A	XT0O	
16	A	XT1I	Clock One pins. A 35.47 MHz (8*Fsc) fundamental (or third harmonic) crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XT1I. CMOS level inputs must be used. This clock source is selected for PAL input sources. If only NTSC or PAL is being decoded, and therefore only XT0I and XT0O are connected to a crystal, XT1I should be tied either high or low, and XT1O *must* be left floating.
17	A	XT1O	
97	O	CLKx1	1x clock output (TTL compatible). The frequency of this clock is 4*Fsc (14.31818 MHz for NTSC or 17.73447 MHz for PAL).
99	O	CLKx2	2x clock output (TTL compatible). The frequency of this clock is 8*Fsc (28.63636 MHz for NTSC, or 35.46895 MHz for PAL).
80	I	NUMXTAL	Crystal Format Pin. This pin is set to indicate whether one or two crystals are present so that the Bt829A can select XT1 or XT0 as the default in auto format mode. A logical zero on this pin indicates one crystal is present. A logical one indicates two crystals are present. This pin is internally pulled down to ground with an effective 18 KΩ resistance.

Table 2. Pin Descriptions Grouped By Pin Function *(4 of 4)*

Pin #	I/O	Pin Name	Description
JTAG Pins			
34	I	TCK	Test Clock (TTL compatible). Used to synchronize all JTAG test structures. When JTAG operations are not being performed, this pin must be driven to a logical low.
36	I	TMS	Test Mode Select (TTL compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin must be left floating or tied high.
37	I	TDI	Test Data Input (TTL compatible). JTAG pin used for loading instruction into the TAP controller or for loading test vector data for boundary-scan operation. When JTAG operations are not being performed, this pin must be left floating or tied high.
32	O	TDO	Test Data Output (TTL compatible). JTAG pin used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG operations and will be three-stated at all other times.
35	I	TRST	Test Reset (TTL compatible). JTAG pin used to initialize the JTAG controller. This pin is tied low for normal device operation. When pulled high, the JTAG controller is ready for device testing.
Power And Ground Pins			
1, 10, 20, 30, 38, 76, 88, 92, 96	P	VDD +5 V	Power supply for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VDD pins and the ground plane as close to the device as possible.
40, 44, 48, 60, 65, 72	P	VAA +5 V, VPOS +5 V	Power supply for analog circuitry. All VAA pins and VPOS must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and the ground plane as close to the device as possible.
11, 21, 31, 33, 39, 77, 81, 90, 93, 95, 100	G	GND	Ground for digital circuitry. All GND pins must be connected together as close to the device as possible.
42, 47, 54, 56, 58, 61, 66, 71, 75	G	AGND, VNEG	Ground for analog circuitry. All AGND pins and VNEG must be connected together as close to the device as possible.

I/O Column Legend:
I = Digital Input
O = Digital Output
I/O = Digital Bidirectional
A = Analog
G = Ground
P = Power

Differences Between Bt829/827 and Bt829A/827A

While both Bt829/827 and Bt829A/827A video decoders are pin and software compatible, please note the following register differences shown in Table 3.

Table 3. Register Differences

Register Bits	Bt829/827	Bt829A/827A	Comments
0x11 Register (Reserved in Bt829, WC_UP in Bt829A)			
[7:6]	Reserved	MAJS	Comparison point for white crush
[5:0]	Reserved	UPCNT	AGC Accumulator
IDCODE Register			
[7:4]	PART_ID	PART_ID	Will reflect Bt829A and Bt827A codes
[3:0]	PART_REV	PART_REV	
VTC Register			
[2]	Reserved	VALID FMT	Video Timing Control
0x1E Register (Reserved in Bt829, WC_DN in Bt829A)			
[7]	Reserved	VERTEN	Improves Vertical Locking
[6]	Reserved	WC FRAME	White Crush Control
[5:0]	Reserved	DNCNT	AGC Accumulator

UltraLock™

The Challenge

The line length (the interval between the midpoints of the falling edges of succeeding horizontal sync pulses) of analog video sources is not constant. For a stable source such as a studio grade video source or test signal generators, this variation is very small: ±2 ns. However, for an unstable source such as a VCR, laser disk player, or TV tuner, line length variation is as much as a few microseconds.

Digital display systems require a fixed number of pixels per line, despite these variations. The Bt829A employs a technique known as UltraLock™ to implement locking to the horizontal sync and the subcarrier of the incoming analog video signal and generating the required number of pixels per line.

Operation Principles of UltraLock™

UltraLock™ is based on sampling, using a fixed-frequency stable clock. Because the video line length will vary, the number of samples generated using a fixed-frequency sample clock will also vary from line to line. If the number of generated samples per line is always greater than the number of samples per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line.

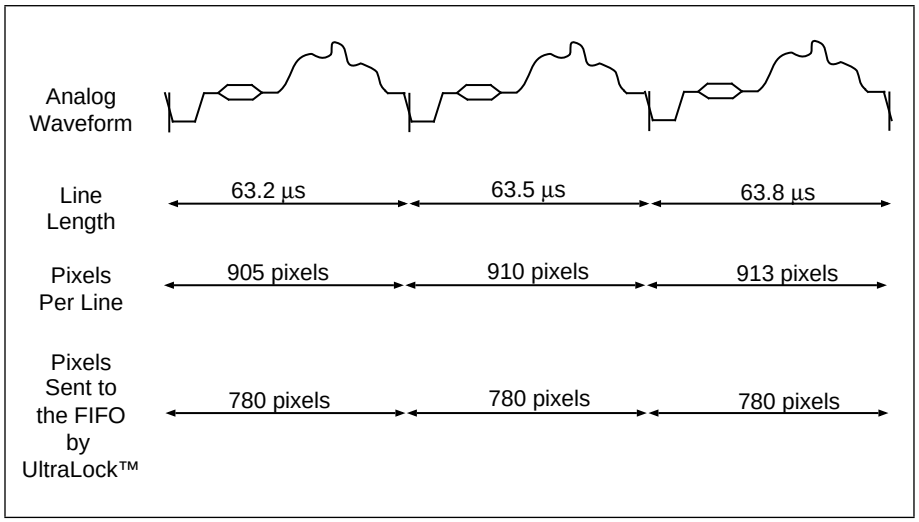
The Bt829A requires an 8*Fsc (28.64 MHz for NTSC and 35.47 MHz for PAL) crystal or oscillator input signal source. The 8*Fsc clock signal, or CLKx2, is divided down to CLKx1 internally (14.32 MHz for NTSC and 17.73 MHz for PAL). Both CLKx2 and CLKx1 are made available to the system. UltraLock™ operates at CLKx1 although the input waveform is sampled at CLKx2 then low-pass filtered and decimated to CLKx1 sample rate.

At a 4*Fsc (CLKx1) sample rate there are 910 pixels for NTSC and 1,135 pixels for PAL/SECAM within a nominal line time interval (63.5 µs for NTSC and 64 µs for PAL/SECAM). For square pixel NTSC and PAL/SECAM formats there should only be 780 and 944 pixels per video line, respectively. This is because the square pixel clock rates are slower than a 4*Fsc clock rate: for example, 12.27 MHz for NTSC and 14.75 MHz for PAL.

UltraLock™ accommodates line length variations from nominal in the incoming video by always acquiring more samples (at an effective 4*Fsc rate) than are required by the particular video format. It then outputs the correct number of pixels per line. UltraLock™ then interpolates the required number of pixels so that it maintains the stability of the original image, despite variation in the line length of the incoming analog waveform.

The example illustrated in Figure 3 shows three successive lines of video being decoded for square pixel NTSC output. The first line is shorter than the nominal NTSC line time interval of 63.5 µs. On this first line, a line time of 63.2 µs sampled at 4*Fsc (14.32 MHz) generates only 905 pixels. The second line matches the nominal line time of 63.5 µs and provides the expected 910 pixels. Finally, the third line is too long at 63.8 µs within which 913 pixels are generated. In all three cases, UltraLock™ outputs only 780 pixels.

Figure 3. UltraLock™ Behavior for NTSC Square Pixel Output



UltraLock™ can be used to extract any programmable number of pixels from the original video stream as long as the sum of the nominal pixel line length (910 for NTSC and 1,135 for PAL/SECAM) and the worst case line length variation from nominal in the active region is greater than or equal to the required number of output pixels per line, i.e.,

$$P_{Nom} + P_{Var} \geq P_{Desired}$$

where: P_{Nom} = Nominal number of pixels per line at 4*Fsc sample rate (910 for NTSC, 1,135 for PAL/SECAM)

P_{Var} = Variation of pixel count from nominal at 4*Fsc (can be a positive or negative number)

$P_{Desired}$ = Desired number of output pixels per line

NOTE: For stable inputs, UltraLock™ guarantees the time between the falling edges of HRESET only to within one pixel. UltraLock™ does, however, guarantee the number of active pixels in a line as long as the above relationship holds.

Composite Video Input Formats

The Bt829A supports several composite video input formats. Table 4 shows the different video formats and some of the countries in which each format is used.

Table 4. Video Input Formats Supported by the Bt829A

Format	Lines	Fields	F_{SC}	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan(1)	525	60	3.58 MHz	Japan
PAL-B	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-G	625	50	4.43 MHz	Many
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	4.43 MHz	Brazil
PAL-N	625	50	4.43 MHz	Paraguay, Uruguay
PAL-N combination	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406 MHz 4.250 MHz	Eastern Europe, France, Middle East
Notes: (1). NTSC-Japan has 0 IRE setup.				

The video decoder must be programmed appropriately for each of the composite video input formats. Table 5 lists the register values that need to be programmed for each input format.

Table 5. Register Values for Video Input Formats

Register	Bit	NTSC-M	NTSC-Japan	PAL-B, D, G, H, I	PAL-M	PAL-N	PAL-N combination	SECAM
IFORM (0x01)	XTSEL 4:3	01	01	10	01	10	01	10
	FORMAT 2:0	001	010	011	100	101	111	110
Cropping: HDELAY, VDELAY, VACTIVE, CROP	7:0 in all 5 registers	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to PAL-B, D, G, H, I square pixel values	Set to PAL-B, D, G, H, I CCIR values	Set to PAL-B, D, G, H, I square pixel values
HSCALE (0x08, 0x09)	15:0	0x02AA	0x02AA	0x033C	0x02AC	0x033C	0x00F8	0x033C
ADELAY (0x18)	7:0	0x68	0x68	0x7F	0x68	0x7F	0x7F	0x7F
BDELAY (0x19)	7:0	0x5D	0x5D	0x72	0x5D	0x72	0x72	0xA0

Y/C Separation and Chroma Demodulation

Y/C separation and chroma decoding are handled as shown in Figure 4. Bandpass and notch filters are implemented to separate the composite video stream. Figure 5 displays the filter responses. The optional chroma comb filter is implemented in the vertical scaling block. See the Video Scaling, Cropping, and Temporal Decimation section in this chapter.

Figure 4. Y/C Separation and Chroma Demodulation for Composite Video

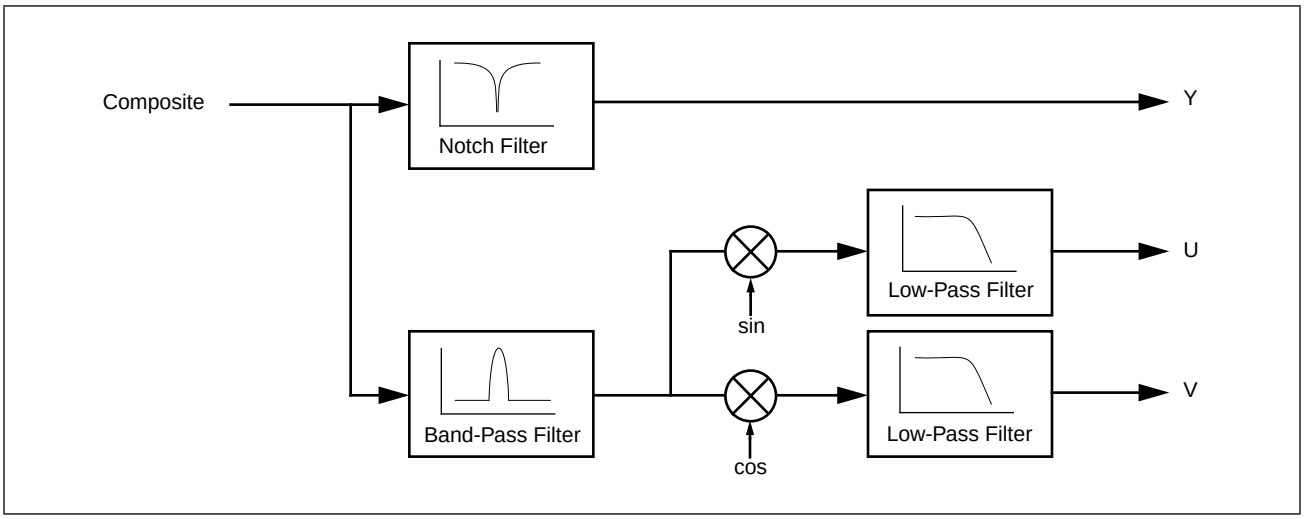


Figure 5. Y/C Separation Filter Responses

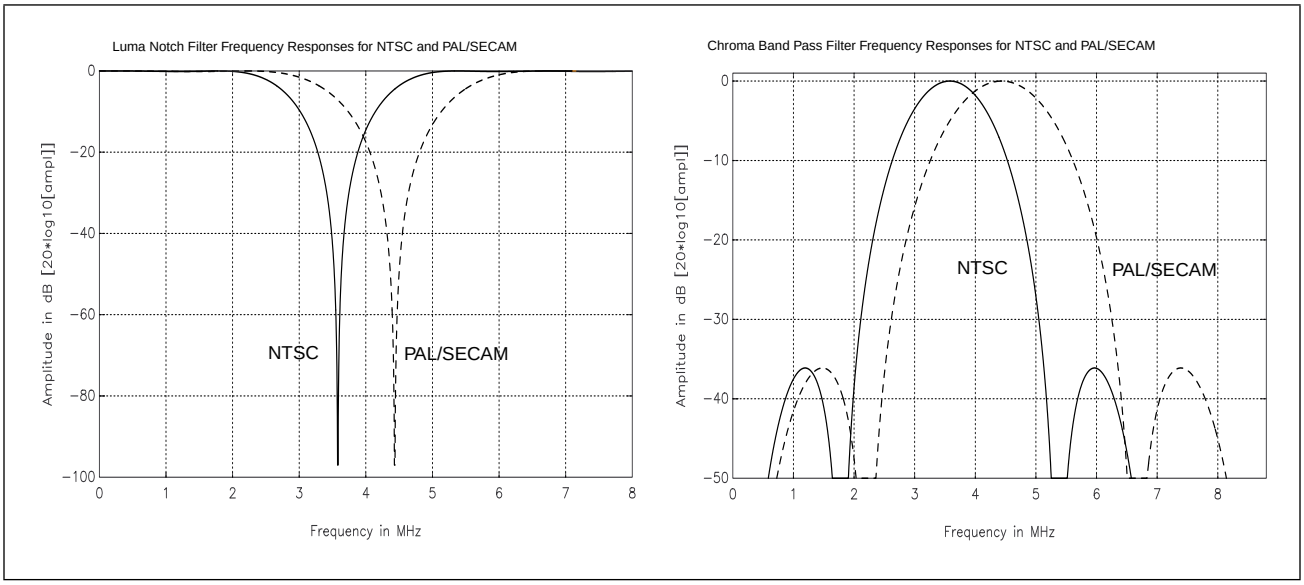


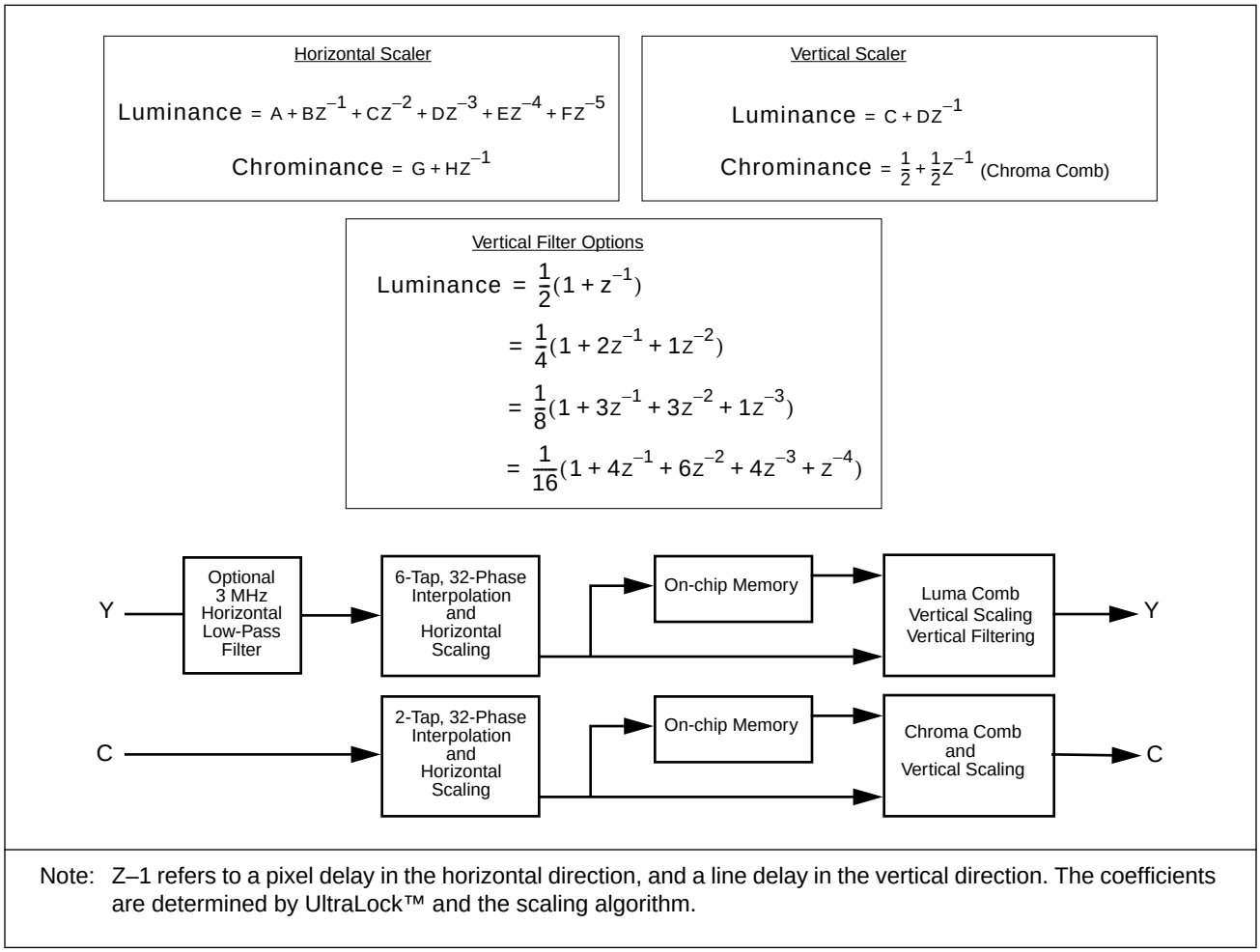
Figure 6 schematically describes the filtering and scaling operations.

In addition to the Y/C separation and chroma demodulation illustrated in Figure 4, the Bt829A also supports chrominance comb filtering as an optional filtering stage after chroma demodulation. The chroma demodulation generates baseband I and Q (NTSC) or U and V (PAL/SECAM) color difference signals.

For S-Video operation, the digitized luma data bypasses the Y/C separation block completely, and the digitized chrominance is passed directly to the chroma demodulator.

For monochrome operation, the Y/C separation block is also bypassed, and the saturation registers (SAT_U and SAT_V) are set to zero.

Figure 6. Filtering and Scaling



Note: Z–1 refers to a pixel delay in the horizontal direction, and a line delay in the vertical direction. The coefficients are determined by UltraLock™ and the scaling algorithm.

Video Scaling, Cropping, and Temporal Decimation

The Bt829A provides three mechanisms to reduce the amount of video pixel data in its output stream: down-scaling, cropping, and temporal decimation. All three can be controlled independently.

Horizontal and Vertical Scaling

The Bt829A provides independent and arbitrary horizontal and vertical down-scaling. The maximum scaling ratio is 16:1 in both X and Y dimensions. The maximum vertical scaling ratio is reduced from 16:1 when using frames to 8:1 when using fields. The different methods utilized for scaling luminance and chrominance are described in the following sections.

Luminance Scaling

The first stage in horizontal luminance scaling is an optional pre-filter which provides the capability to reduce anti-aliasing artifacts. It is generally desirable to limit the bandwidth of the luminance spectrum prior to performing horizontal scaling because the scaling of high-frequency components may create image artifacts in the resized image. The optional low-pass filters shown in Figure 7 reduce the horizontal high-frequency spectrum in the luminance signal. Figure 8 and Figure 9 show the combined results of the optional low-pass filters, and the luma notch and 2x oversampling filter.

Figure 7. Optional Horizontal Luma Low-Pass Filter Responses

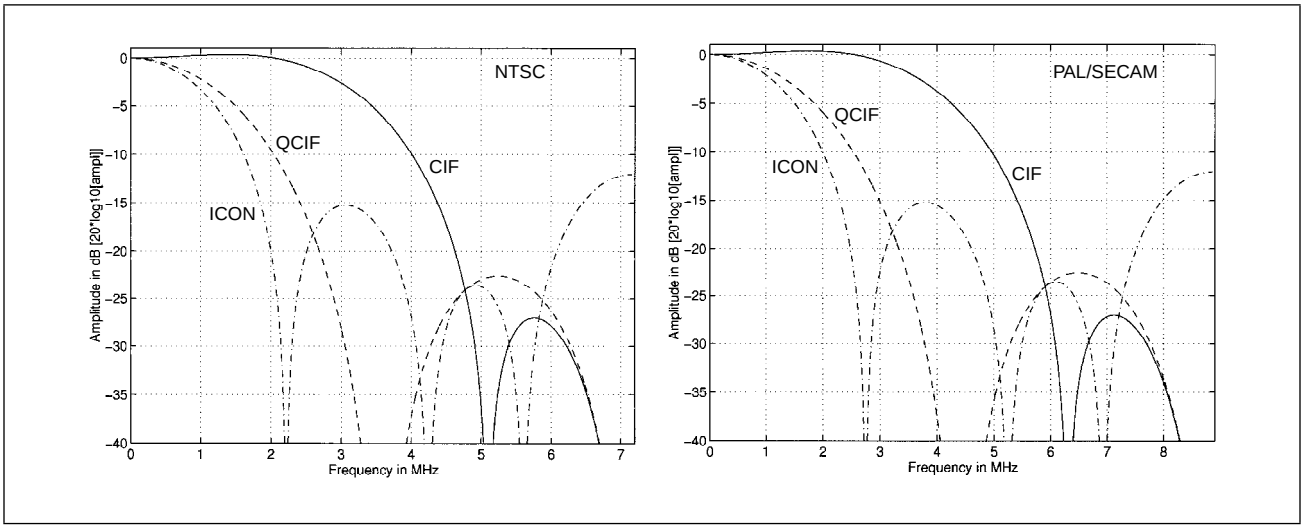


Figure 8. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (NTSC)

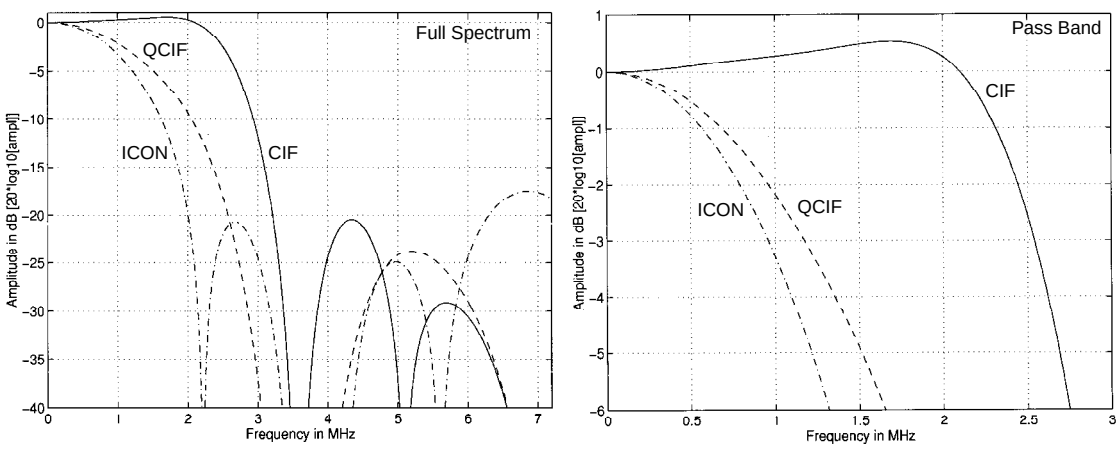
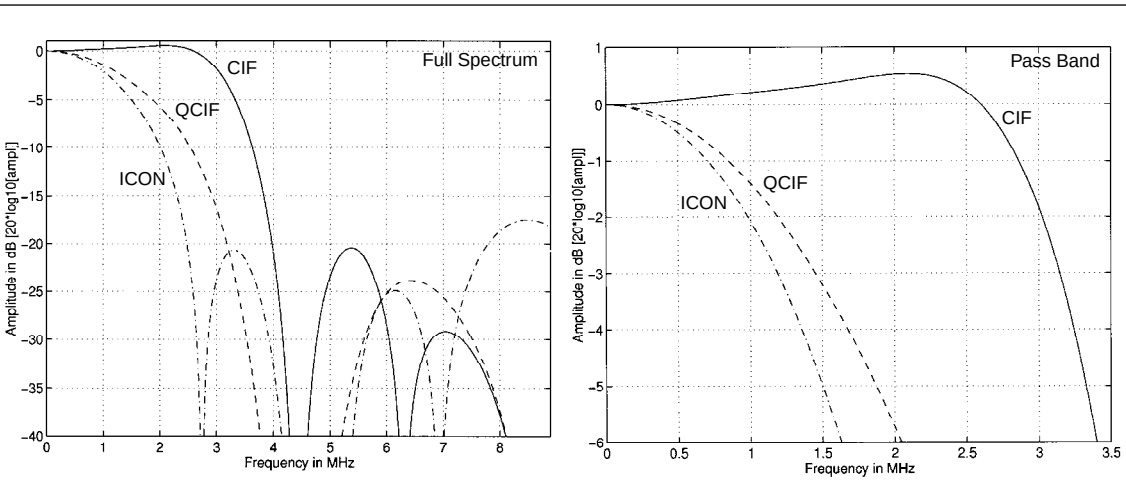


Figure 9. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (PAL/SECAM)



The Bt829A implements horizontal scaling through poly-phase interpolation. The Bt829A uses 32 different phases to accurately interpolate the value of a pixel. This provides an effective pixel jitter of less than 6 ns.

In simple pixel- and line-dropping algorithms, non-integer scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position providing more accurate information. This results in more aesthetically pleasing video as well as higher compression ratios in bandwidth limited applications.

For vertical scaling, the Bt829A uses a line store to implement four different filtering options. The filter characteristics are shown in Figure 10. The Bt829A provides up to 5-tap filtering to ensure removal of aliasing artifacts. Figure 11 shows the combined responses of the luma notch and 2x oversampling filters.

Figure 10. Frequency Responses for the Four Optional Vertical Luma Low-Pass Filters

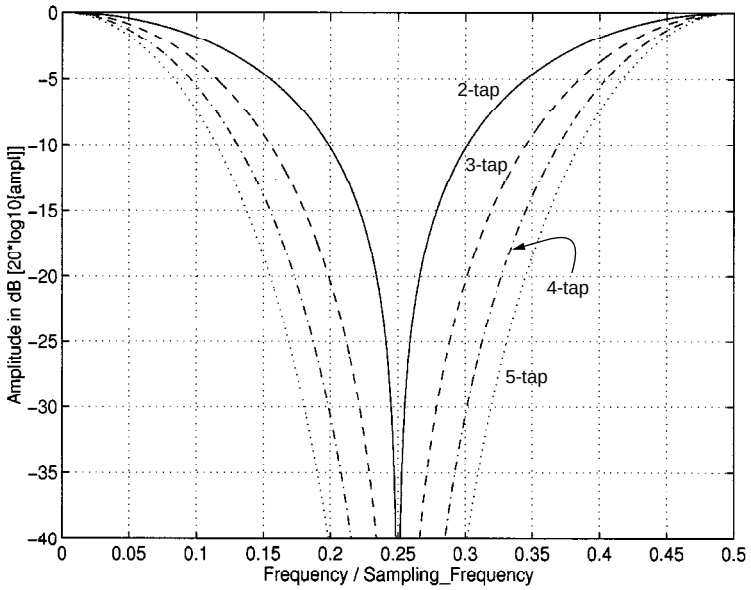
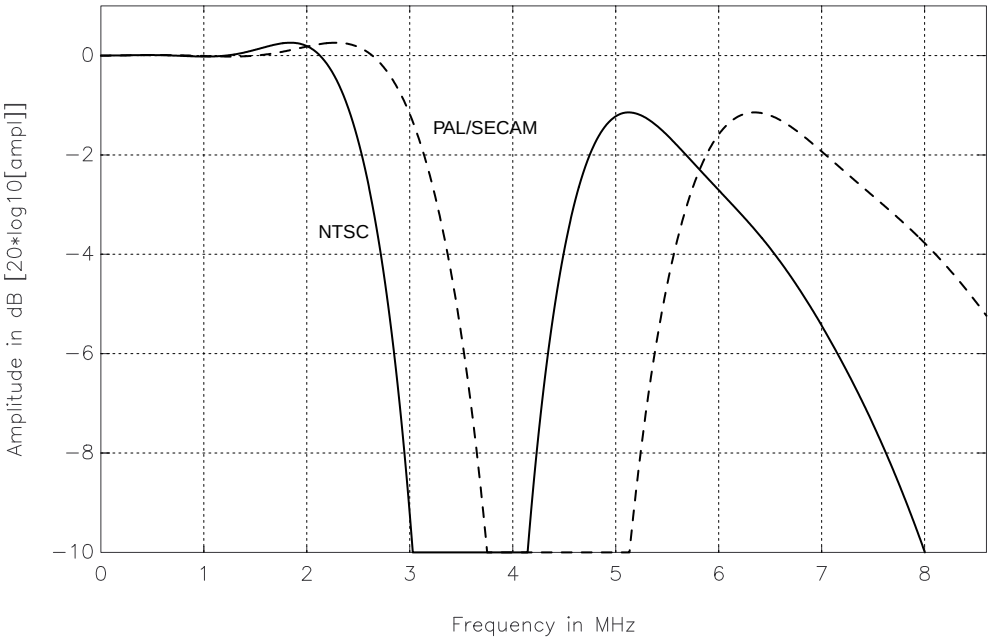


Figure 11. Combined Luma Notch and 2x Oversampling Filter Response



Peaking

The Bt829A enables four different peaking levels by programming the PEAK bit and HFILT bits in the SCLOOP register. The filters are shown in Figures 12 and 13.

Figure 12. Peaking Filters

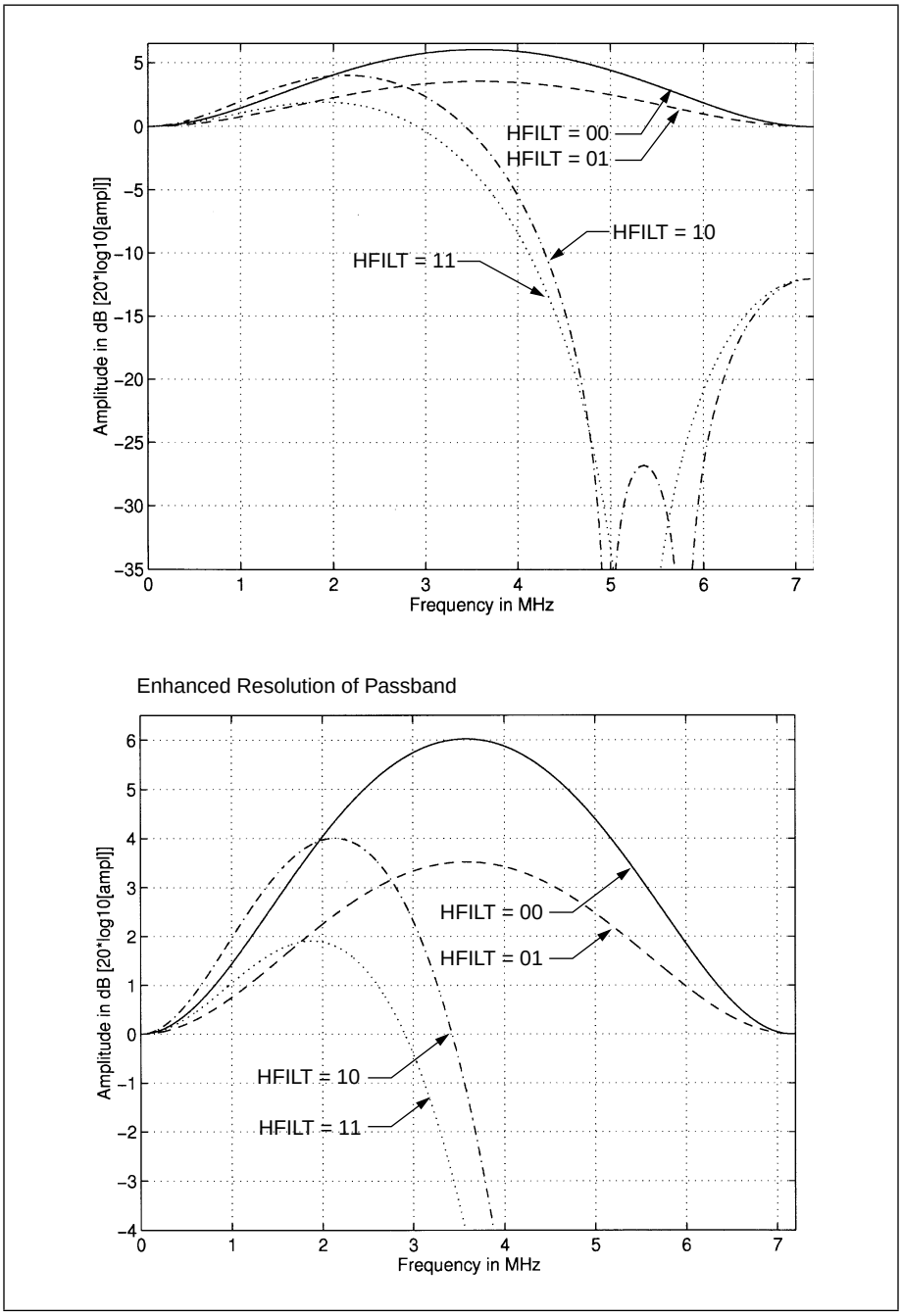
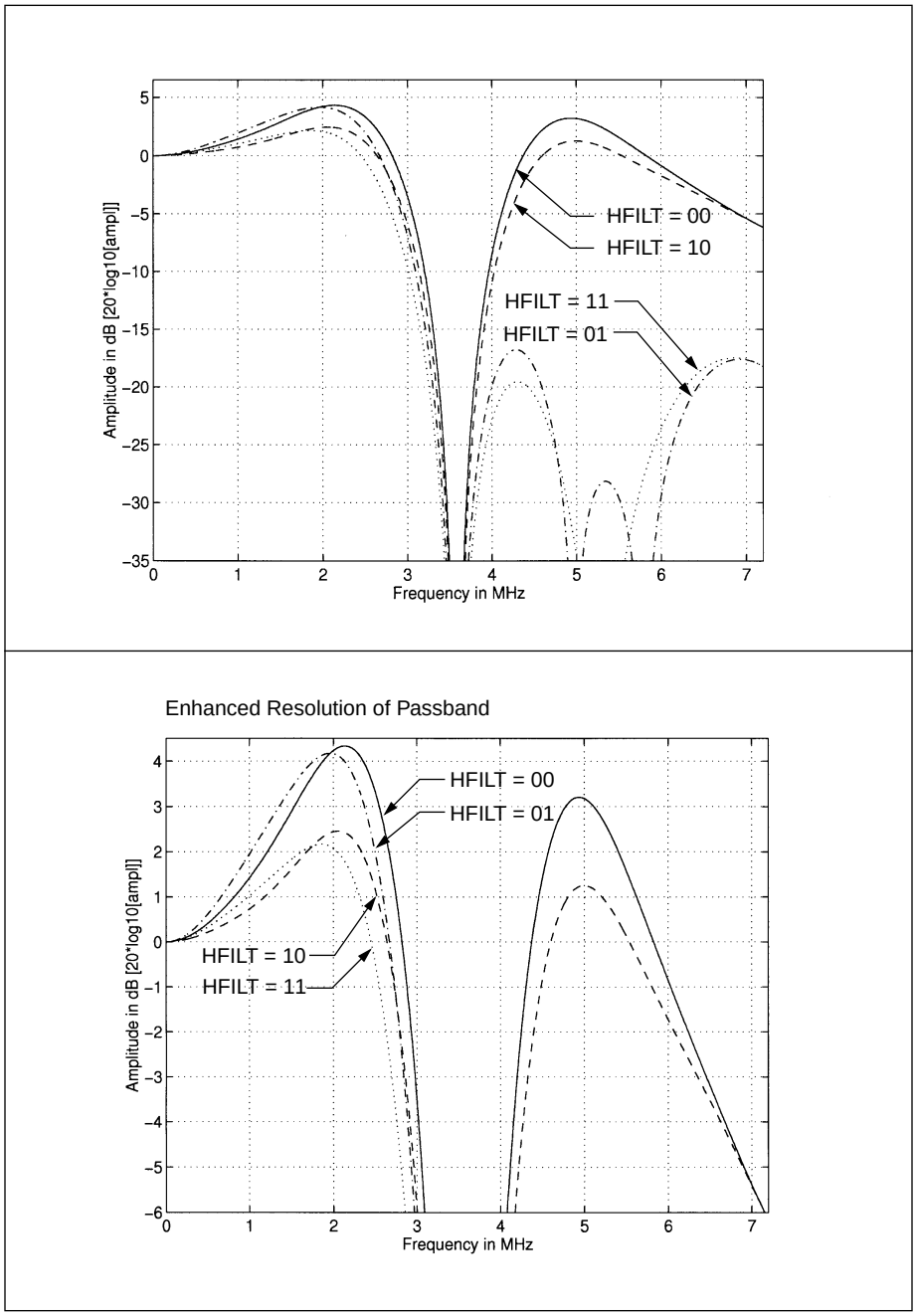


Figure 13. Luma Peaking Filters with 2x Oversampling Filter and Luma Notch



The number of taps in the vertical filter is set by the VTC register. The user may select 2, 3, 4, or 5 taps. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure that the needed data can fit in the internal FIFO (see the VFILT bits in the VTC register for limitations). As the scaling ratio is increased, the number of taps available for vertical scaling is increased. In addition to low-pass filtering, vertical interpolation is also employed to minimize artifacts when scaling to non-integer scaling ratios. The Bt827A employs line dropping for vertical scaling.

Chrominance Scaling

A 2-tap, 32-phase interpolation filter is used for horizontal scaling of chrominance. Vertical scaling of chrominance is implemented through chrominance comb filtering using a line store, followed by simple decimation or line dropping.

Scaling Registers

Horizontal Scaling Ratio Register (HSCALE) HSCALE is programmed with the horizontal scaling ratio. When outputting unscaled video (in NTSC), the Bt829A will produce 910 pixels per line. This corresponds to the pixel rate at f_{CLKx1} (4*Fsc). This register is the control for scaling the video to the desired size. For example, square pixel NTSC requires 780 samples per line, while CCIR601 requires 858 samples per line. HSCALE_HI and HSCALE_LO are two 8-bit registers that, when concatenated, form the 16-bit HSCALE register.

The method below uses pixel ratios to determine the scaling ratio. The following formula should be used to determine the scaling ratio to be entered into the 16-bit register:

$$\text{NTSC:} \quad HSCALE = [\,(910/P_{desired}) - 1] * 4096$$
$$\text{PAL/SECAM:} \quad HSCALE = [\,(1135/P_{desired}) - 1] * 4096$$

where: $P_{desired}$ = Desired number of pixels per line of video, including active, sync and blanking.

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of horizontal pixels is 236:

$$HSCALE = [\,(1135/236) - 1\,] * 4096$$
$$= 15602$$
$$= 0x3CF2$$

An alternative method for determining the HSCALE value uses the ratio of the scaled active region to the unscaled active region as shown below:

$$\text{NTSC:} \quad HSCALE = [\,(754 / HACTIVE) - 1] * 4096$$
$$\text{PAL/SECAM:} \quad HSCALE = [\,(922 / HACTIVE) - 1] * 4096$$

where: *HACTIVE* = Desired number of pixels per line of video, not including sync or blanking.

In this equation, the HACTIVE value cannot be cropped; it represents the total active region of the video line. This equation produces roughly the same result as using the full line length ratio shown in the first example. However, due to truncation, the HSCALE values determined using the active pixel ratio will be slightly different than those obtained using the total line length pixel ratio. The values in Table 6 were calculated using the full line length ratio.

Table 6. Scaling Ratios for Popular Formats Using Frequency Values

Scaling Ratio	Format	Total Resolution (including sync and blanking interval)	Output Resolution (Active Pixels)	HSCALE Register Values	VSCALE Register Values	
					Use Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	780 x 525 858 x 525 864 x 625 944 x 625	640 x 480 720 x 480 720 x 576 768 x 576	0x02AC 0x00F8 0x0504 0x033C	0x0000 0x0000 0x0000 0x0000	N/A N/A N/A N/A
CIF 2:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	390 x 262 429 x 262 432 x 312 472 x 312	320 x 240 360 x 240 360 x 288 384 x 288	0x1555 0x11F0 0x1A09 0x1679	0x1E00 0x1E00 0x1E00 0x1E00	0x0000 0x0000 0x0000 0x0000
QCIF 4:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	195 x 131 214 x 131 216 x 156 236 x 156	160 x 120 180 x 120 180 x 144 192 x 144	0x3AAA 0x3409 0x4412 0x3CF2	0x1A00 0x1A00 0x1A00 0x1A00	0x1E00 0x1E00 0x1E00 0x1E00
ICON 8:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	97 x 65 107 x 65 108 x 78 118 x 78	80 x 60 90 x 60 90 x 72 96 x 72	0x861A 0x7813 0x9825 0x89E5	0x1200 0x1200 0x1200 0x1200	0x1A00 0x1A00 0x1A00 0x1A00

Notes:
1. PAL-M–HSCALE and VSCALE register values should be the same for NTSC.
2. PAL-N combination–HSCALE register values should be the same as for CCIR resolution NTSC. VSCALE register values should be the same as for CCIR resolution PAL.
3. SECAM–HSCALE and VSCALE register values should be the same as for PAL.

Vertical Scaling Ratio Register (VSCALE) VSCALE is programmed with the vertical scaling ratio. It defines the number of vertical lines output by the Bt829A. The following formula should be used to determine the value to be entered into this 13-bit register. The loaded value is a two's-complement, negative value.

$$VSCALE = (0x10000 - \{ [(scaling\_ratio) - 1] * 512 \}) \& 0x1FFF$$

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of vertical lines for PAL square pixel is 156 (see Table 6).

$$VSCALE = (0x10000 - \{ [(4/1) - 1] * 512 \}) \& 0x1FFF$$
$$= 0x1A00$$

Note that only the 13 least significant bits of the VSCALE value are used. The five LSBs of VSCALE_HI and the 8-bit VSCALE_LO register form the 13-bit VSCALE register. The three MSBs of VSCALE_HI are used to control other functions. The user must take care not to alter the values of the three most significant bits when writing a vertical scaling value. The following C-code fragment illustrates changing the vertical scaling value:

```
#define BYTE unsigned char
#define WORD unsigned int
#define VSCALE_HI 0x13
#define VSCALE_LO 0x14

BYTE ReadFromBt829A( BYTE regAddress );
void WriteToBt829A( BYTE regAddress, BYTE regValue );

void SetBt829AVScaling( WORD VSCALE )
{
  BYTE oldVscaleMSByte, newVscaleMSByte;

  /* get existing VscaleMSByte value from */
  /* Bt829A VSCALE_HI register */
  oldVscaleMSByte = ReadFromBt829A( VSCALE_HI );

  /* create a new VscaleMSByte, preserving top 3 bits */
  newVscaleMSByte = (oldVscaleMSByte & 0xE0) | (VSCALE >> 8);

  /* send the new VscaleMSByte to the VSCALE_HI reg */
  WriteToBt829A( VSCALE_HI, newVscaleMSByte );

  /* send the new VscaleLSByte to the VSCALE_LO reg */
  WriteToBt829A( VSCALE_LO, (BYTE) VSCALE );
}
```

where: `&` = bitwise AND
`|` = bitwise OR
`>>` = bit shift, MSB to LSB

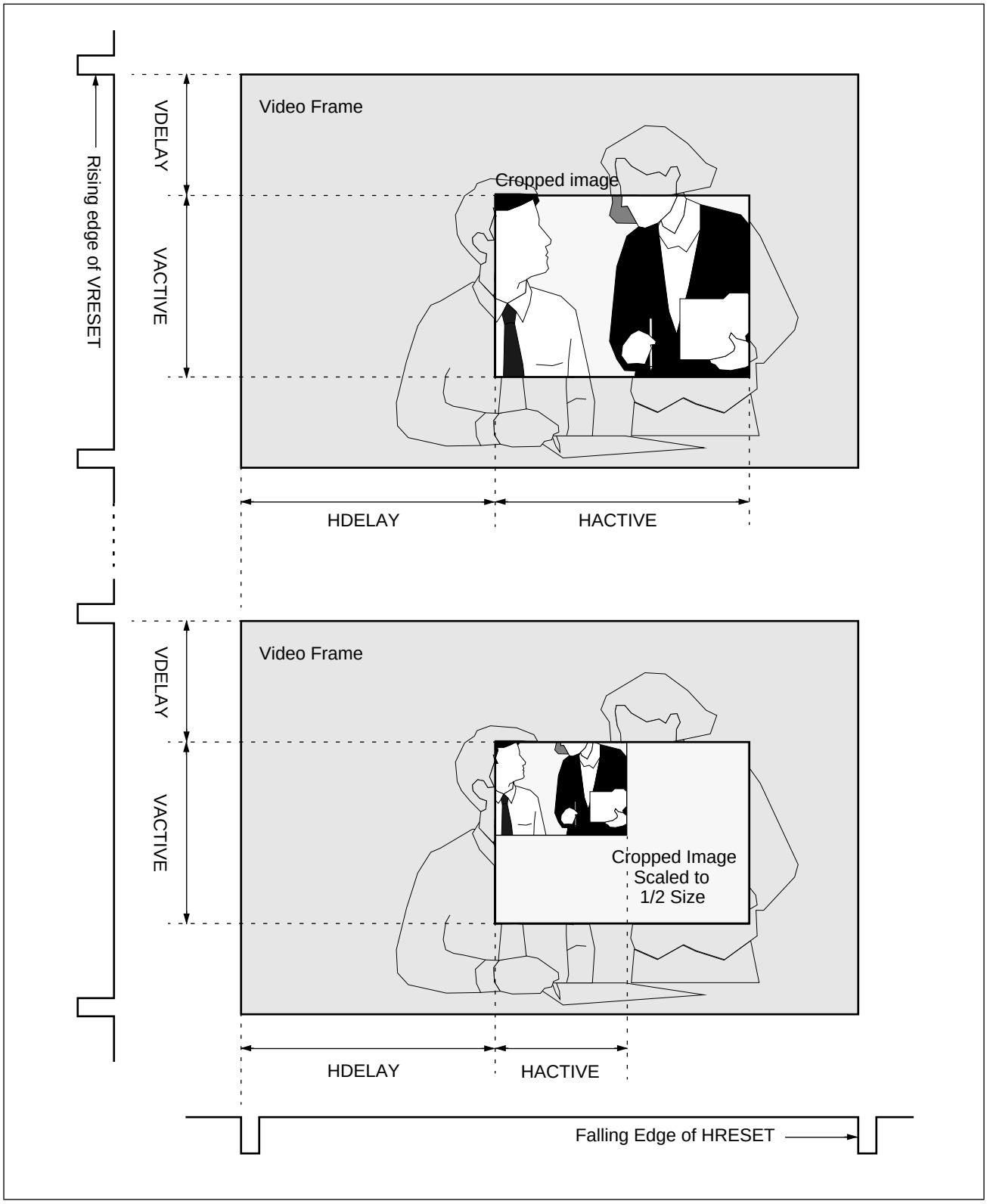
If your target machine has sufficient memory to statically store the scaling values locally, the READ operation can be eliminated.

On vertical scaling (when scaling below CIF resolution) it may be useful to use a single field as opposed to using both fields. Using a single field will ensure there are no inter-field motion artifacts on the scaled output. When performing single field scaling, the vertical scaling ratio will be twice as large as when scaling with both fields. For example, CIF scaling from one field does not require any vertical scaling, but when scaling from both fields, the scaling ratio is 50%. Also, the non-interlaced bit should be reset when scaling from a single field (INT = 0 in the VSCALE_HI register). Table 6 lists scaling ratios for various video formats, and the register values required.

Image Cropping

Cropping enables the user to output any subsection of the video image. The ACTIVE flag can be programmed to start and stop at any position on the video frame as shown in Figure 14. The start of the active area in the vertical direction is referenced to $\overline{\text{VRESET}}$ (beginning of a new field). In the horizontal direction it is referenced to $\overline{\text{HRESET}}$ (beginning of a new line). The dimensions of the active video region are defined by HDELAY, HACTIVE, VDELAY, and VACTIVE. All four registers are 10-bit values. The two MSBs of each register are contained in the CROP register, while the lower eight bits are in the respective HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO registers. The vertical and horizontal delay values determine the position of the cropped image within a frame while the horizontal and vertical active values set the pixel dimensions of the cropped image as illustrated in Figure 14.

Figure 14. Effect of the Cropping and Active Registers



Cropping Registers

Horizontal Delay Register (HDELAY) HDELAY is programmed with the delay between the falling edge of $\overline{\text{HRESET}}$ and the rising edge of ACTIVE. The count is programmed with respect to the scaled frequency clock. Note that HDELAY should always be an even number.

Horizontal Active Register (HACTIVE) HACTIVE is programmed with the actual number of active pixels per line of video. This is equivalent to the number of scaled pixels that the Bt829A should output on a line. For example, if this register contained 90, and HSCALE was programmed to down-scale by 4:1, then 90 active pixels would be output. The 90 pixels would be a 4:1 scaled image of the 360 pixels (at CLKx1) starting at count HDELAY. HACTIVE is restricted in the following manner:

HACTIVE + HDELAY ≤ Total Number of Scaled Pixels.

For example, in the NTSC square pixel format, there is a total of 780 pixels, including blanking, sync and active regions. Therefore:

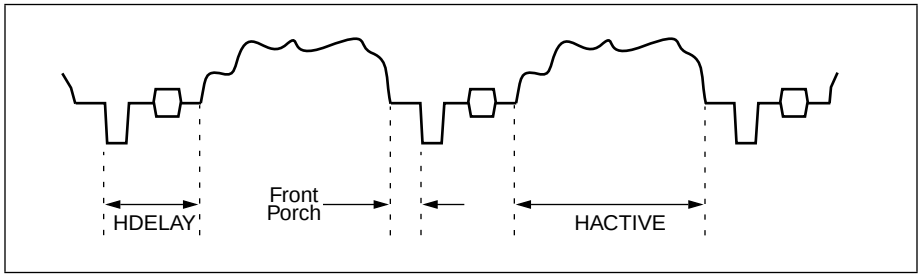
HACTIVE + HDELAY ≤ 780.

When scaled by 2:1 for CIF, the total number of active pixels is 390. Therefore:

HACTIVE +HDELAY ≤ 390.

The HDELAY register is programmed with the number of scaled pixels between HRESET and the first active pixel. Because the front porch is defined as the distance between the last active pixel and the next horizontal sync, the video line can be considered in three components: HDELAY, HACTIVE and the front porch. Figure 15 illustrates the video signal regions.

Figure 15. Regions of the Video Signal



When cropping is not implemented, the number of clocks at the 4x sample rate (the CLKx1 rate) in each of these regions is as follows:

	CLKx1 Front Porch	CLKx1 HDELAY	CLKx1 HACTIVE	CLKx1 Total
NTSC	21	135	754	910
PAL/SECAM	27	186	922	1135

The value for HDELAY is calculated using the following formula:

HDELAY = [(CLKx1_HDELAY / CLKx1_HACTIVE) * HACTIVE] & 0x3FE

CLKx1_HDELAY and CLKx1_HACTIVE are constant values, so the equation becomes:

NTSC: HDELAY = [(135 / 754) * HACTIVE] & 0x3FE
PAL/SECAM: HDELAY = [(186 / 922) * HACTIVE] & 0x3FE

In this equation, the HACTIVE value cannot be cropped.

Vertical Delay Register (VDELAY) VDELAY is programmed with the delay between the rising edge of $\overline{\text{VRESET}}$ and the start of active video lines. It determines how many lines to skip before initiating the ACTIVE signal. It is programmed with the number of lines to skip at the beginning of a frame.

Vertical Active Register (VACTIVE) VACTIVE is programmed with the number of lines used in the vertical scaling process. The actual number of vertical lines output from the Bt829A is equal to this register times the vertical scaling ratio. If VSCALE is set to 0x1A00 (4:1), then the actual number of lines output is VACTIVE/4. If VSCALE is set to 0x0000 (1:1), then VACTIVE contains the actual number of vertical lines output.

NOTE: It is important to note the difference between the implementation of the horizontal registers (HSCALE, HDELAY, and HACTIVE) and the vertical registers (VSCALE, VDELAY, and VACTIVE). Horizontally, HDELAY and HACTIVE are programmed with respect to the scaled pixels defined by HSCALE. Vertically, VDELAY and VACTIVE are programmed with respect to the number of lines before scaling (before VSCALE is applied).

Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when full frame rate cannot be supported due to bandwidth and system restrictions.

For example, when capturing live video for storage, system limitations such as hard disk transfer rates or system bus bandwidth may limit the frame capture rate. If these restrictions limit the frame rate to 15 frames per second, the Bt829A's time scaling operation will enable the system to capture every other frame instead of allowing the hard disk timing restrictions to dictate which frame to capture. This maintains an even distribution of captured frames and alleviates the "jerky" effects caused by systems that simply burst in data when the bandwidth becomes available.

The Bt829A provides temporal decimation on either a field or frame basis. The temporal decimation register (TDEC) is loaded with a value from 1 to 60 (NTSC) or 1 to 50 (PAL/SECAM). This value is the number of fields or frames skipped by the chip during a sequence of 60 for NTSC or 50 for PAL/SECAM. Skipped fields and frames are considered inactive, which is indicated by the ACTIVE pin remaining low. Consequently if QCLK is programmed to depend on ACTIVE, QCLK would become inactive as well.

Examples:

TDEC = 0x02	Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding. Frames 1–29 are output normally, then ACTIVE remains low for one frame. Frames 30–59 are then output followed by another frame of inactive video.
TDEC = 0x9E	Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding. This value outputs every other field (every odd field) of video starting with field one in frame one.
TDEC = 0x01	Decimation is performed by frames. One frame is skipped per 50 frames of video, assuming PAL/SECAM decoding.
TDEC = 0x00	Decimation is not performed. Full frame rate video is output by the Bt829A.

When changing the programming in the temporal decimation register, 0x00 should be loaded first, and then the decimation value. This will ensure that the decimation counter is reset to zero. If zero is not first loaded, the decimation may start on any field or frame in the sequence of 60 (or 50 for PAL/SECAM). On power-up, this preload is not necessary because the counter is internally reset.

When decimating fields, the FLDALIGN bit in the TDEC register can be programmed to choose whether the decimation starts with an odd field or an even field. If the FLDALIGN bit is set to logical zero, the first field that is dropped during the decimation process will be an odd field. Conversely, setting the FLDALIGN bit to logical one causes the even field to be dropped first in the decimation process.

Video Adjustments

The Bt829A provides programmable hue, contrast, saturation, and brightness.

The Hue Adjust Register (HUE)

The Hue Adjust Register is used to offset the hue of the decoded signal. In NTSC, the hue of the video signal is defined as the phase of the subcarrier with reference to the burst. The value programmed in this register is added or subtracted from the phase of the subcarrier, which effectively changes the hue of the video. The hue can be shifted by plus or minus 90 degrees. Because of the nature of PAL/SECAM encoding, hue adjustments cannot be made when decoding PAL/SECAM.

The Contrast Adjust Register (CONTRAST)

The Contrast Adjust Register (also called the luma gain) provides the ability to change the contrast from approximately 0 percent to 200 percent of the original value. The decoded luma value is multiplied by the 9-bit coefficient loaded into this register.

The Saturation Adjust Registers (SAT_U, SAT_V)

The Saturation Adjust Registers are additional color adjustment registers. It is a multiplicative gain of the U and V signals. The value programmed in these registers are the coefficients for the multiplication. The saturation range is from approximately 0 percent to 200 percent of the original value.

The Brightness Register (BRIGHT)

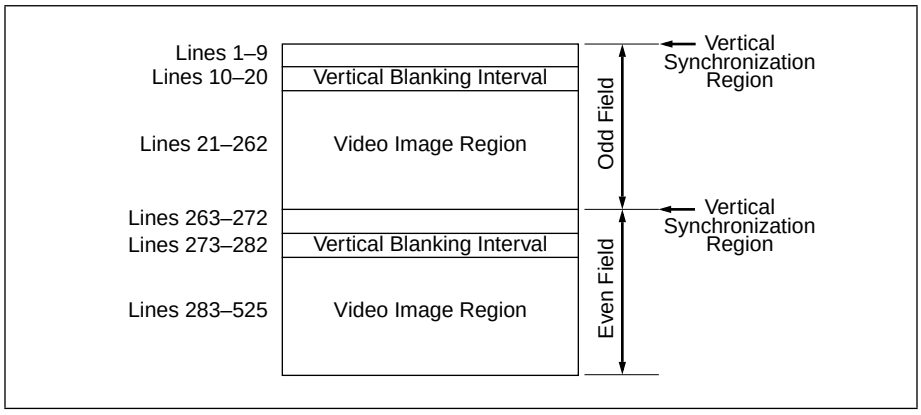
The Brightness Register is simply an offset for the decoded luma value. The programmed value is added or subtracted from the original luma value which changes the brightness of the video output. The luma output is in the range of 0 to 255. Brightness adjustment can be made over a range of –128 to +127.

Bt829A VBI Data Output Interface

Introduction

A frame of video is composed of 525 lines for NSTC and 625 for PAL/SECAM. Figure 16 illustrates an NTSC video frame in which there are a number of distinct regions. The video image or picture data is contained in the ODD and EVEN fields within lines 21 to 262 and lines 283 to 525, respectively. Each field of video also contains a region for vertical synchronization (lines 1 through 9 and 263 through 272) as well as a region which can contain non-video ancillary data (lines 10 through 20 and 273 through 282). We will refer to these regions which are between the vertical synchronization region and the video picture region as the Vertical Blanking Interval or VBI portion of the video signal.

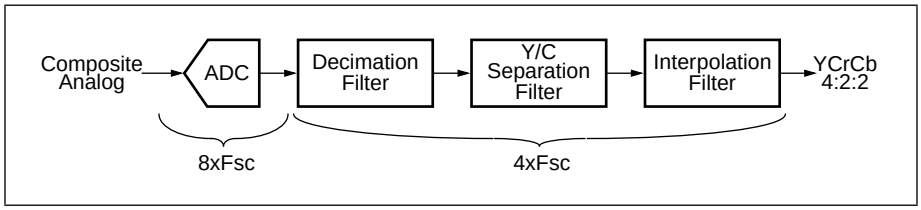
Figure 16. Regions of the Video Frame



Overview

In the default configuration of the Bt829A, the VBI region of the video signal is treated the same way as the video image region of the signal. The Bt829A will decode this signal as if it was video, i.e., it will digitize at 8xFsc, decimate/filter to a 4xFsc sample stream, color separate to derive luma and chroma component information, and interpolate for video synchronization and horizontal scaling. This process is shown in Figure 17.

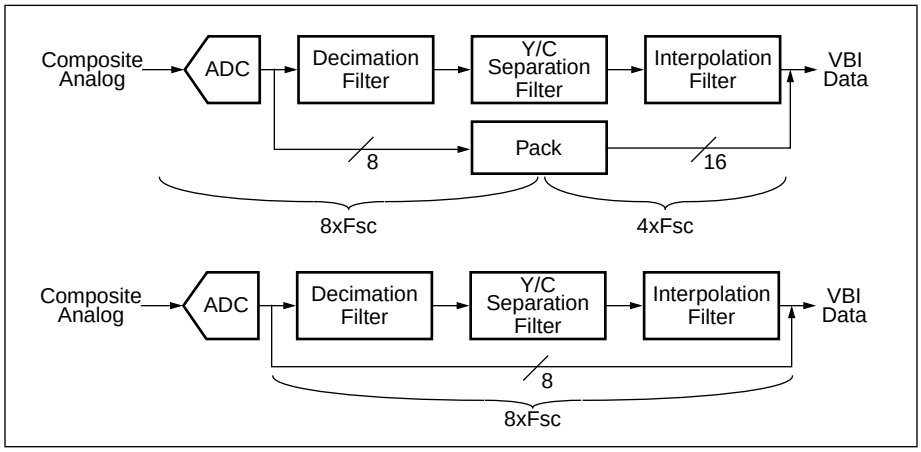
Figure 17. Bt829A YCrCb 4:2:2 Data Path



The Bt829A can be configured in a mode known as VBI data pass-through to enable capture of the VBI region ancillary data for later processing by software. In this mode the VBI region of the video signal is processed as follows:

- The analog composite video signal is digitized at 8*Fsc (28.63636 MHz for NTSC and 35.46895 MHz for PAL/SECAM). This 8-bit value represents a number range from the bottom of sync tip to peak of the composite video signal.
- The 8-bit data stream bypasses the decimation filter, Y/C separation filters, and the interpolation filter (see Figure 18).
- The Bt829A provides the option to pack the 8*Fsc data stream into a 2-byte-wide stream at 4*Fsc before outputting it to the VD[15:0] data pins, or it can simply be output as an 8-bit 8*Fsc data stream on pins VD[15:8]. In the packed format, the first byte of each pair on a 4*Fsc clock cycle is mapped to VD[15:8] and the second byte to VD[7:0] with VD[7] and VD[15] being the MSBs. The Bt829A uses the same 16-pin data port for VBI data and YCrCb 4:2:2 image data. The byte pair ordering is programmable.

Figure 18. Bt829A VBI Data Path



- The VBI datastream is not pipeline delayed to match the YCrCb 4:2:2 image output data with respect to horizontal timing (i.e. valid VBI data will be output earlier than YCrCb 4:2:2 relative to the Bt829A HRESET signal).
- A larger number of pixels per line are generated in VBI output mode than in YCrCb 4:2:2 output mode. The downstream video processor must be capable of dealing with a varying number of pixels per line in order to capture VBI data as well as YCrCb 4:2:2 data from the same frame.
- The following pins may be used to implement this solution: VD[15:0], VACTIVE, HACTIVE, DVALID, $\overline{\text{VRESET}}$, $\overline{\text{HRESET}}$, CLKx1, CLKx2, QCLK. This should allow the downstream video processor to load the VBI data and the YCrCb 4:2:2 data correctly.
- Because the 8*Fsc data stream does not pass through the interpolation filter, the sample stream is not locked/synchronized to the horizontal sync timing. The only implication of this is that the sample locations on each line are not correlated vertically.

Functional Description

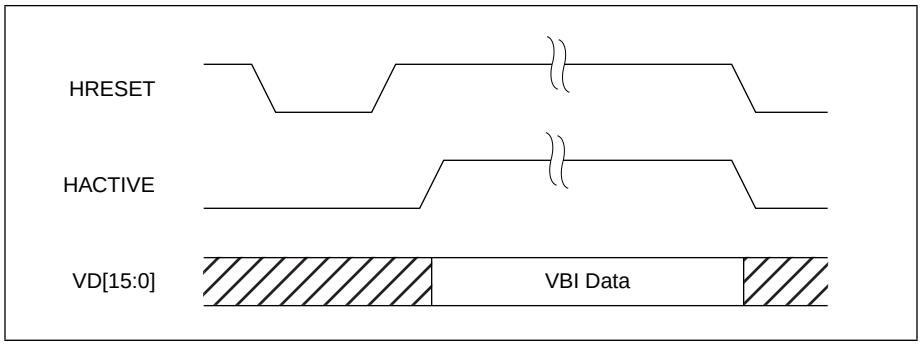
There are three modes of operation for the Bt829A VBI data pass-through feature:

1. VBI Data Pass-through Disabled. This is the default mode of operation for the Bt829A during which the device decodes composite video and generates a YCrCb 4:2:2 data stream.
2. VBI Line Output Mode. The device outputs unfiltered 8*Fsc data only during the vertical interval which is defined by the VACTIVE output signal provided by the Bt829A. Data is output between the trailing edge of the $\overline{\text{VRESET}}$ signal and the leading edge of VACTIVE. When VACTIVE is high, the Bt829A is outputting standard YCrCb 4:2:2 data. This mode of operation is intended to be used to enable capture of VBI lines containing ancillary data in addition to processing normal YCrCb 4:2:2 video image data.
3. VBI Frame Output Mode. In this mode the Bt829A treats every line in the video signal as if it were a vertical interval line and outputs only the unfiltered 8*Fsc data on every line (i.e., it does not output any image data). This mode of operation is designed for use in still-frame capture/processing applications.

VBI Line Output Mode

The VBI line output mode is enabled via the VBIEN bit in the VTC Register (0x1B). When enabled, the VBI data is output during the VBI active period. The VBI horizontal active period is defined as the interval between consecutive Bt829A $\overline{\text{HRESET}}$ signals. Specifically, it starts at a point one CLKx1 interval after the trailing edge of the first $\overline{\text{HRESET}}$ and ends with the leading edge of the following $\overline{\text{HRESET}}$. This interval is coincident with the HACTIVE signal as indicated in Figure 19.

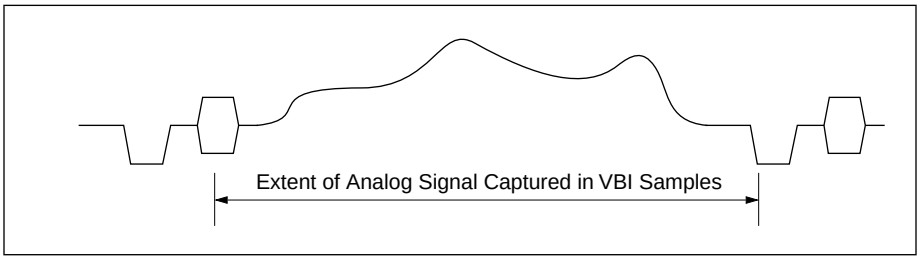
Figure 19. VBI Line Output Mode Timing



DVALID is always at a logical one during VBI. Also, QCLK is operating continuously at CLKx1 or CLKx2 rate during VBI. Valid VBI data is available one CLKx1 (or QCLK) interval after the trailing edge of $\overline{\text{HRESET}}$. When the Bt829A is configured in VBI line output mode, it is generating invalid data outside of the VBI horizontal active period. In standard YCrCb output mode, the horizontal active period starts at a time point delayed from the leading edge of $\overline{\text{HRESET}}$ as defined by the value programmed in the HDELAY register.

The VBI data sample stream which is output during the VBI horizontal active period represents an 8*Fsc sampled version of the analog video signal starting in the vicinity of the sub-carrier burst and ending after the leading edge of the horizontal synchronization pulse as illustrated in Figure 20.

Figure 20. VBI Sample Region

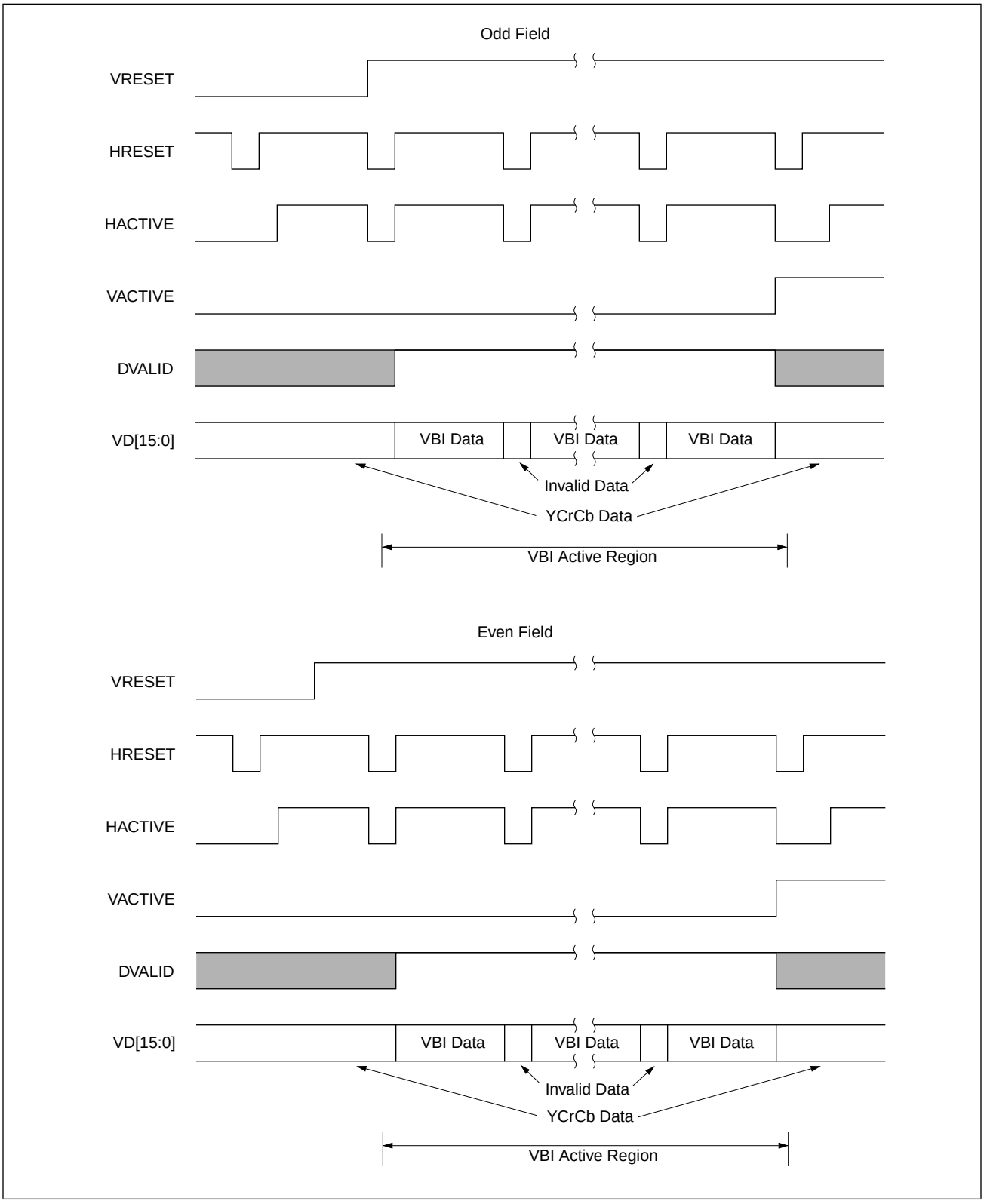


The number of VBI data samples generated on each line may vary depending on the stability of the analog composite video signal input to the Bt829A. The Bt829A will generate 845 16-bit VBI data words for NTSC and 1070 16-bit VBI data words for PAL/SECAM on each VBI line at a CLKx1 rate assuming a nominal or ideal video input signal (i.e., the analog video signal has a stable horizontal time base). This is also equivalent to 1690 8-bit VBI data samples for NTSC and 2140 8-bit VBI data samples for PAL/SECAM. These values can deviate from the nominal depending on the actual line length of the analog video signal.

The VBI vertical active period is defined as the period between the trailing edge of the Bt829A $\overline{\text{VRESET}}$ signal and the leading edge of VACTIVE. Note that the extent of the VBI vertical active region can be controlled by setting different values in the VDELAY register. This provides the flexibility to configure the VBI vertical active region as any group of consecutive lines starting with line 10 and extending to the line number set by the equivalent line count value in the VDELAY register (i.e., the VBI vertical active region can be extended into the video image region of the video signal).

The VBI horizontal active period starts with the trailing edge of an $\overline{\text{HRESET}}$; therefore, if a rising edge of $\overline{\text{VRESET}}$ occurs after the horizontal active period has already started, the VBI active period starts on the following line. The HACTIVE pin is held at a logical one during the VBI horizontal active period. DVALID is held high during both the VBI horizontal active and horizontal inactive periods (i.e., it is held high during the whole VBI scan line.) These relationships are illustrated in Figure 21.

Figure 21. Location of VBI Data

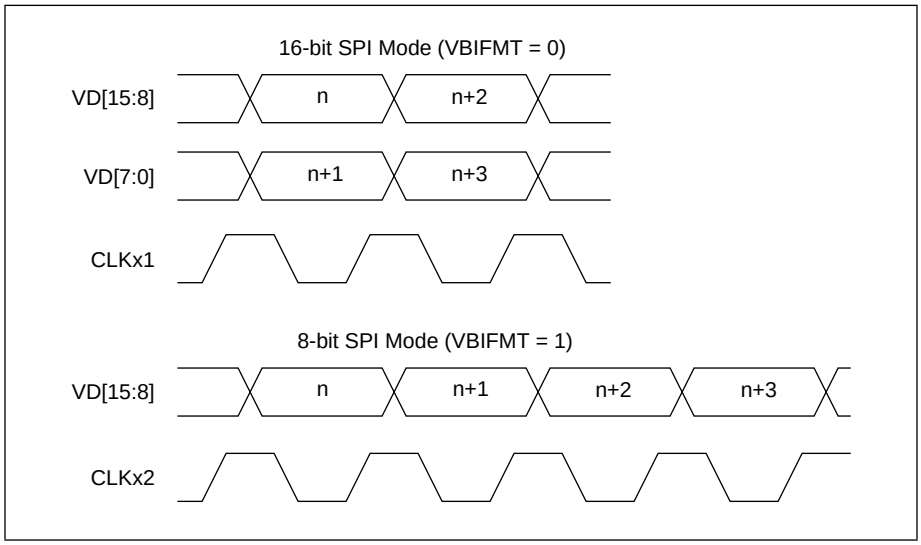


The Bt829A can provide VBI data in all the pixel port output configurations (i.e., 16-bit SPI, 8-bit SPI, and ByteStream™ modes). The range of the VBI data can be controlled with the RANGE bit in the OFORM Register (0x12). It is necessary to limit the range of VBI data for ByteStream™ output mode.

There must be a video signal present on the Bt829A analog input as defined by the status of the VPRES bit in the STATUS register in order for the Bt829A to generate VBI data. If the status of the VPRES bit reflects no analog input, then the Bt829A generates YCrCb data to create a flat blue field image.

The order in which the VBI data is presented on the output pins is programmable. Setting the VBIFMT bit in the VTC register to a logical zero places the nth data sample on VD[15:8] and the nth+1 sample on VD[7:0]. Setting VBIFMT to a logical one reverses the above. Similarly, in ByteStream™ and 8-bit output modes, setting VBIFMT = 0 generates a VBI sample stream with an ordering sequence of n+1, n, n+3, n+2, n+5, n+4, etc. Setting VBIFMT = 1 for ByteStream™/8-bit output generates an n, n+1, n+2, n+3, etc. sequence as shown in Figure 22.

Figure 22. VBI Sample Ordering



A video processor/controller should be able to do the following to capture VBI data output by the Bt829A:

- Keep track of the line count in order to select a limited number of specific lines for processing of VBI data.
- Handle data type transitioning on the fly from the vertical interval to the active video image region. For example, during the vertical interval with VBI data pass-through enabled, it must grab every byte pair while HACTIVE is high using the 4*Fsc clock or QCLK. However, when the data stream transitions into YCrCb 4:2:2 data mode with VACTIVE going high, the video processor must interpret the DVALID signal (or use QCLK for the data load clock) from the Bt829A for pixel qualification and use only valid pixel cycles to load image data (default Bt829A operation).
- Handle a large and varying number of horizontal pixels per line in the VBI region as compared to the active image region.

VBI Frame Output Mode

In VBI frame output mode, the Bt829A is generating VBI data all the time (i.e., there is no VBI active interval). In essence, the Bt829A is acting as an ADC continuously sampling the entire video signal at 8*Fsc. The Bt829A generates $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$ and FIELD timing signals in addition to the VBI data, but the DVALID, HACTIVE, and VACTIVE signals are all held high during VBI frame output operation. The behavior of the $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$, and FIELD timing signals is the same as normal YCrCb 4:2:2 output operation. The $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$, and FIELD timing signals can be used by the video processor to detect the beginning of a video frame/field, at which point it can start to capture a full frame/field of VBI data.

The number of VBI data samples generated on each line may vary depending on the stability of the analog composite video signal input to the Bt829A. The Bt829A will generate 910 16-bit VBI data words for NTSC and 1135 16-bit VBI data words for PAL/SECAM for each line of analog video input at a CLKx1 rate assuming a nominal or ideal video input signal (i.e., analog video signal has a stable horizontal time base). This is also equivalent to 1820 8-bit VBI data samples for NTSC and 2270 8-bit VBI data samples for PAL/SECAM for each line of analog video input. These values can deviate from the nominal depending on the actual line length of the analog video signal.

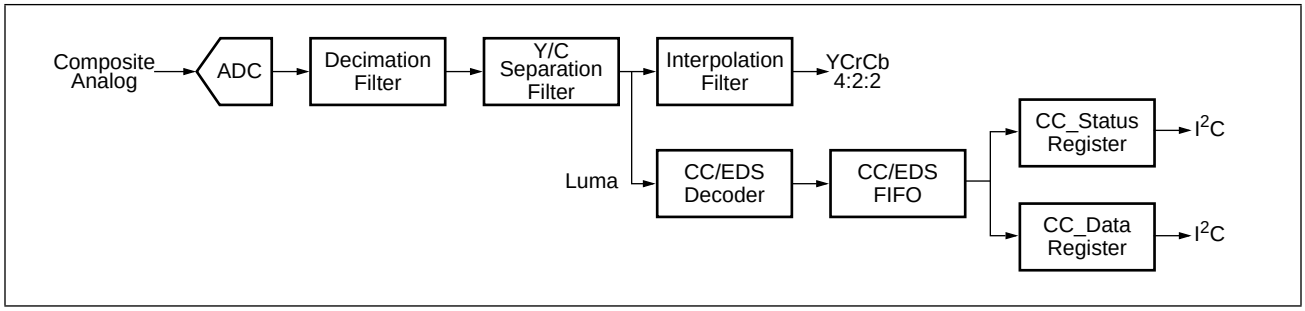
VBI frame output mode is enabled via the VBIFRM bit in the OFORM register. The output byte ordering may be controlled by the VBIFMT bit as described for VBI line output mode. If both VBI line output and VBI frame output modes are enabled at the same time, the VBI frame output mode takes precedence. The VBI data range in VBI frame output mode can be controlled using the RANGE bit in the OFORM register, and a video signal must be present on the Bt829A analog input for this mode to operate as defined by the status of the VPRES bit in the STATUS register (0x00).

Closed Captioning and Extended Data Services Decoding

In a system capable of capturing Closed Captioning (CC) and Extended Data Services (EDS) adhering to the EIA-608 standard, two bytes of information are presented to the video decoder on line 21 (odd field) for CC and an additional two bytes are presented on line 284 (even field) for EDS.

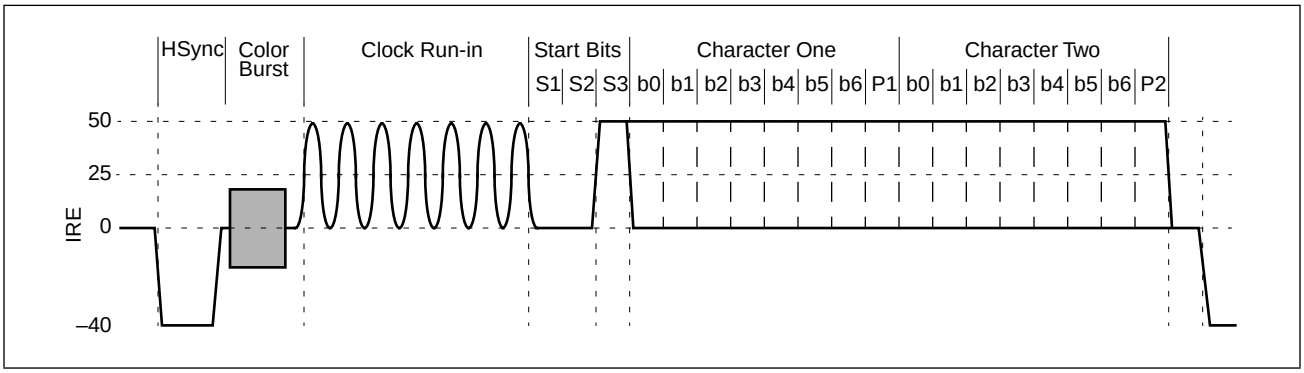
The data presented to the video decoder is an analog signal on the composite video input. The signal contains information identifying it as the CC/EDS data and is followed by a control code and two bytes of digital information transmitted by the analog signal. For the purposes of CC/EDS, only the luma component of the video signal is relevant. Therefore, the composite signal goes through the decimation and Y/C separation blocks of the Bt829A before any CC/EDS decoding takes place. See Figure 23 for a representation of this procedure.

Figure 23. CC/EDS Data Processing Path



The Bt829A can be programmed to decode CC/EDS data via the corresponding bits in the Extended Data Services/Closed Caption Status Register (CC_STATUS;0X1C). The CC and EDS are independent and the video decoder may capture one or both in a given frame. The CC/EDS signal is displayed in Figure 24. In CC/EDS decode mode, once Bt829A has detected that line 21 of the field is being displayed, the decoder looks for the Clock Run-In signal. If the Clock Run-In signal is present and the correct start code (001) is recognized by Bt829A, then the CC/EDS data capture commences. Each of the two bytes of data transmitted to the video decoder per field contains a 7-bit ASCII code and a parity bit. The convention for CC/EDS data is odd parity.

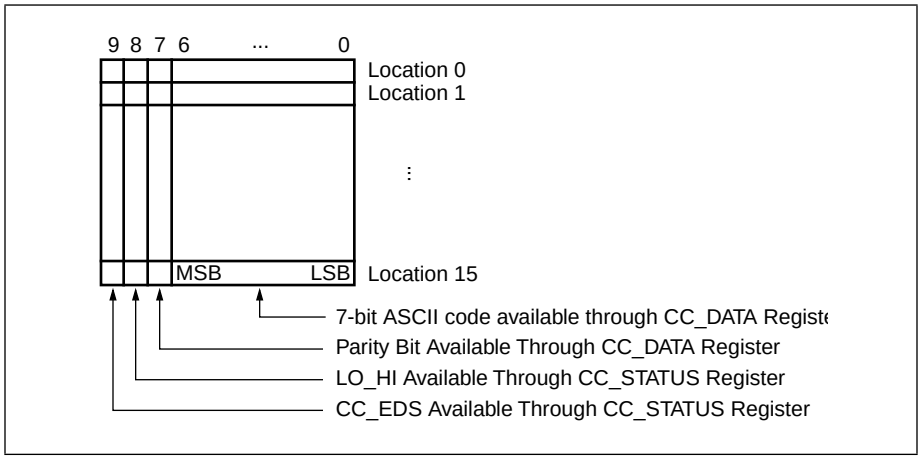
Figure 24. CC/EDS Incoming Signal



The Bt829A provides a 16 x 10 location FIFO for storing CC/EDS data. Once the video decoder detects the start signal in the CC/EDS signal, it captures the low byte of CC/EDS data first and checks to see if the FIFO is full. If the FIFO is not full, then the data is stored in the FIFO, and is available to the user through the CC_DATA register (0x1D). The high byte of CC/EDS data is captured next and placed in the FIFO. Upon being placed in the 10-bit FIFO, two additional bits are attached to the CC/EDS data byte by Bt829A's CC/EDS decoder. These two bits indicate whether the given byte stored in the FIFO corresponds to CC or EDS data and whether it is the high or low byte of CC/EDS. These two bits are available to the user through the CC_STATUS register bits CC_EDS and LO_HI, respectively.

The parity bit is stored in the FIFO as shown in Figure 25. Additionally, the Bt829A stores the results of the parity check in the PARITY_ERR bit in the CC_STATUS register.

Figure 25. Closed Captioning/Extended Data Services FIFO



The 16-location FIFO can hold eight lines worth of CC/EDS data, at two bytes per line. Initially when the FIFO is empty, bit DA in the CC_STATUS register (0x1C) is set low and indicates that no data is available in the FIFO. Subsequently, when data has been stored in the FIFO, the DA bit is set to logical high. Once the FIFO is half full, the CC_VALID interrupts pin signals to the system that the FIFO contents should be read in the near future. The CC_VALID pin is enabled via a bit in the CC_STATUS register (0x1C). The system controller can then poll the CC_VALID bit in the STATUS register (0x00) to ensure that it was the Bt829A that initiated the CC_VALID interrupt. This bit can also be used in applications where the CC_VALID pin is disabled by the user.

When the first byte of CC/EDS data is decoded and stored in the FIFO, the data is immediately placed in the CC_DATA and CC_STATUS registers and is available to be read. Once the data is read from the CC_DATA register, the information in the next location of the FIFO is placed in the CC_DATA and CC_STATUS registers.

If the controller in the system ignores the Bt829A CC_VALID interrupts pin for a sufficiently long period of time, then the CC/EDS FIFO will become full and the Bt829A will not be able to write additional data to the FIFO. Any incoming bytes of data will be lost and an overflow condition will occur; bit OR in the CC_STATUS register will be set to a logical one. The system may clear the overflow condition by reading the CC/EDS data and creating space in the FIFO for new information. As a result, the overflow bit is reset to a logical zero.

There will routinely be asynchronous reads and writes to the CC/EDS FIFO. The writes will be from the CC/EDS circuitry and the reads will occur as the system controller reads the CC/EDS data from Bt829A. These reads and writes will sometimes occur simultaneously, and the Bt829A is designed to give priority to the read operations. In the case where the CC_DATA register data is specifically being read to clear an overflow condition, the simultaneous occurrence of a read and a write will not cause the overflow bit to be reset, even though the read has priority. An additional read must be made to the CC_DATA register in order to clear the overflow condition. As always, the write data will be lost while the FIFO is in overflow condition.

The FIFO is reset when both CC and EDS bits are disabled in the CC_STATUS register; any data in the FIFO is lost.

Automatic Chrominance Gain Control

The Automatic Chrominance Gain Control compensates for reduced chrominance and color-burst amplitude. This can be caused by high-frequency loss in cabling. Here, the color-burst amplitude is calculated and compared to nominal. The color-difference signals are then increased or decreased in amplitude according to the color-burst amplitude difference from nominal. The maximum amount of chrominance gain is 0.5–2 times the original amplitude. This compensation coefficient is then multiplied by the value in the Saturation Adjust Register for a total chrominance gain range of 0–2 times the original signal. Automatic chrominance gain control may be disabled by setting the CAGC bit in the SCLOOP register to a logical zero.

Low Color Detection and Removal

If a color burst of 25 percent (NTSC) or 35 percent (PAL/SECAM) or less of the nominal amplitude is detected for 127 consecutive scan lines, the color-difference signals U and V are set to zero. When the low color detection is active, the reduced chrominance signal is still separated from the composite signal to generate the luminance portion of the signal. The resulting Cr and Cb values are 128. Output of the chrominance signal is re-enabled when a color burst of 43 percent (NTSC) or 60 percent (PAL/SECAM) or greater of nominal amplitude is detected for 127 consecutive scan lines.

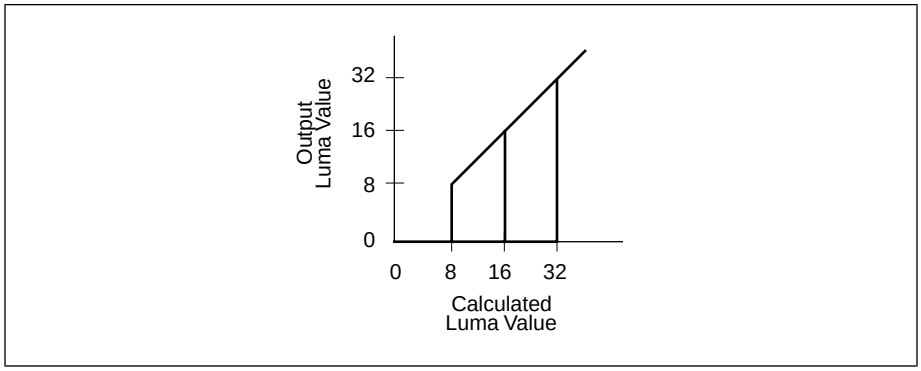
Low color detection and removal may be disabled by setting the CKILL bit in the SCLOOP register (0x10) to a logical zero.

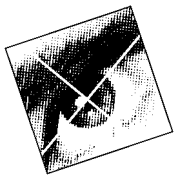
Coring

The Bt829A video decoder can perform a coring function, in which it forces all values below a programmed level to be zero. This is useful because the human eye is more sensitive to variations in black images. By taking near-black images and turning them into black, the image appears clearer to the eye.

Four coring values can be selected by the Output Format Register (OFORM; 0x12): 0, 8, 16, or 32 above black. If the total luminance level is below the selected limit, the luminance signal is truncated to the black value. If the luma range is limited (i.e., black is 16), then the coring circuitry automatically takes this into account and references the appropriate value for black. This is illustrated in Figure 26.

Figure 26. Coring Map





ELECTRICAL INTERFACES

Input Interface

Analog Signal Selection

The Bt829A/827A contains an on-chip 4:1 MUX. For the Bt829A and Bt827A, this multiplexer can be used to switch between four composite sources or three composite sources and one S-Video source. In the first configuration, connect the inputs of the multiplexer (MUX[0], MUX[1], MUX[2] and MUX[3]) to the four composite sources. In the second configuration, connect three inputs to the composite sources and the other input to the luma component of the S-Video connector. In both configurations the output of the multiplexer (MUXOUT) should be connected to the input to the luma A/D (YIN) and the input to the sync detection circuitry (SYNCDET) through a optional 0.1 µF capacitor (to maintain compatibility with the Bt829/827). When implementing S-Video, the input to the chroma A/D (CIN) should be connected to the chroma signal of the S-Video connector.

Use of the multiplexer is not a requirement for operation. If digitization of only one video source is required, the source may be connected directly to YIN.

Multiplexer Considerations

The multiplexer is not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω .

The multiplexers cannot be switched on a real-time pixel-by-pixel basis.

Autodetection of NTSC or PAL/SECAM Video

If the Bt829A is configured to decode both NTSC and PAL/SECAM, the Bt829A can be programmed to automatically detect which format is being input to the chip. Autodetection will select the proper clock source for the format detected. If NTSC/PAL–M is detected, XTAL0 is selected. If PAL/SECAM is detected, XTAL1 is selected. For PAL-N combination the user must manually select the XTAL0 crystal. Full control of the decoding configuration can be programmed by writing to the Input Format Register (0x01).

The Bt829A determines the video source input to the chip by counting the number of lines in a frame. Bit NUML indicates the result in the STATUS register. Based on this bit, the format of the video is determined, and XT0 or XT1 is selected for the clock source. Automatic format detection will select the clock source, but it will not program the required registers. The scaling and cropping registers (VSCALE, HSCALE, VDELAY, HDELAY, VACTIVE, and HACTIVE) as well as the burst delay and AGC delay registers (BDELAY and ADELAY) must be programmed accordingly.

Flash A/D Converters

The Bt829A and Bt827A use two on-chip flash A/D converters to digitize the video signals. YREF+, CREF+ and YREF–, CREF– are the respective top and bottom of the internal resistor ladder.

The input video is always ac-coupled to the decoder. CREF– and YREF– are connected to analog ground. The voltage levels for YREF+ and CREF+ are controlled by the gain control circuitry. If the input video momentarily exceeds the corresponding REF+ voltage it is indicated by LOF and COF in the STATUS register.

A/D Clamping

An internally generated clamp control signal is used to clamp the inputs of the A/D converter for DC restoration of the video signals. Clamping for both the YIN and CIN analog inputs occurs within the horizontal sync tip. The YIN input is always restored to ground while the CIN input is always restored to CLEVEL. CLEVEL can be set with an optional external resistor network so that it is biased to the midpoint between CREF– and CREF+. This insures backward compatibility with Bt819A/7A/5A but is not required for the Bt829A/827A. External clamping is not required because internal clamping is automatically performed.

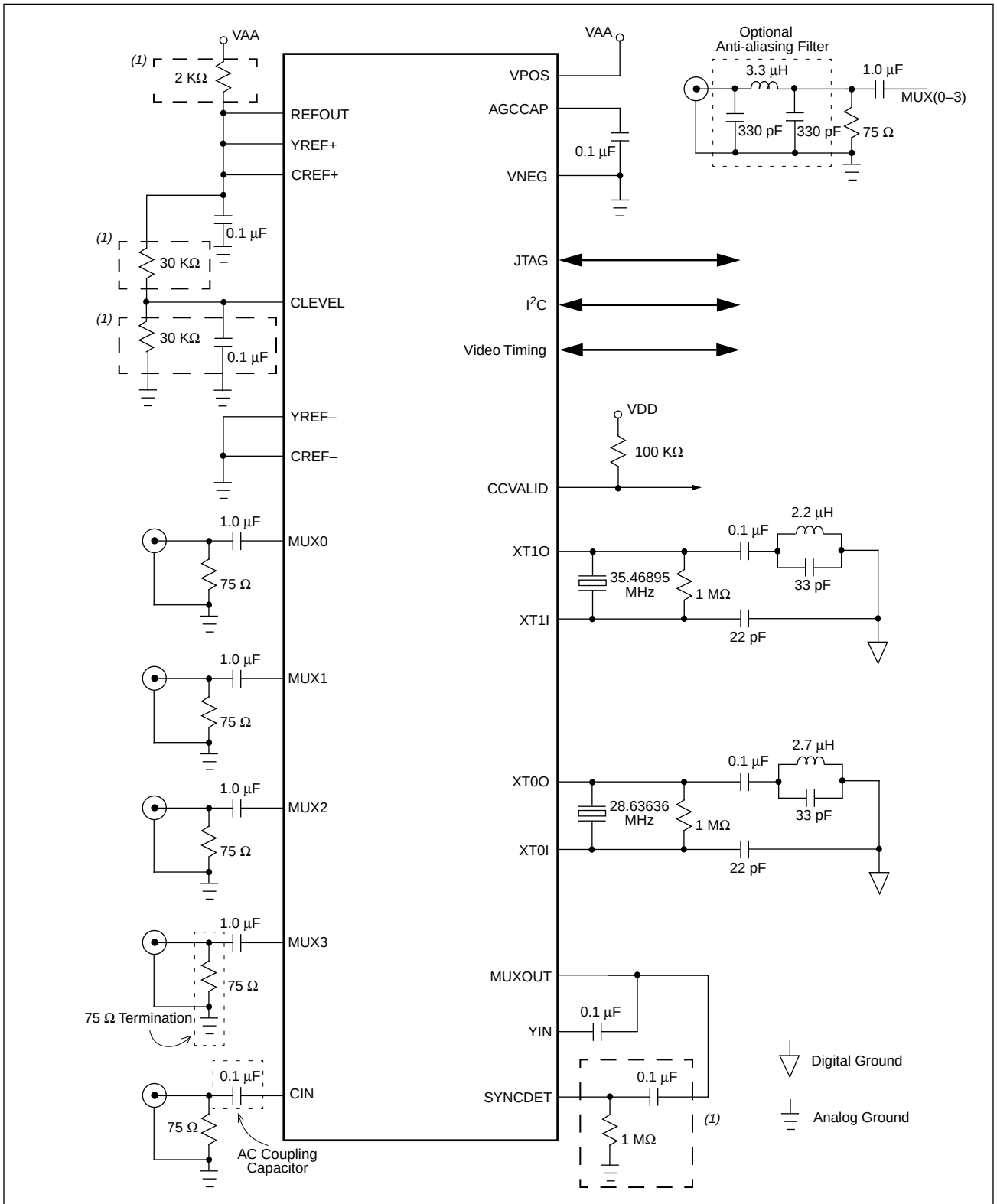
Power-up Operation

Upon power-up, the status of the Bt829A's registers is indeterminate. The $\overline{\text{RST}}$ signal must be asserted to set the register bits to their default values. The Bt829A device defaults to NTSC-M format upon reset. If pin 85 (OEPOLE) is a logical high and the $\overline{\text{RST}}$ signal is asserted then the video pixel bus, sync signals, and output clocks will be three-stated.

Automatic Gain Controls

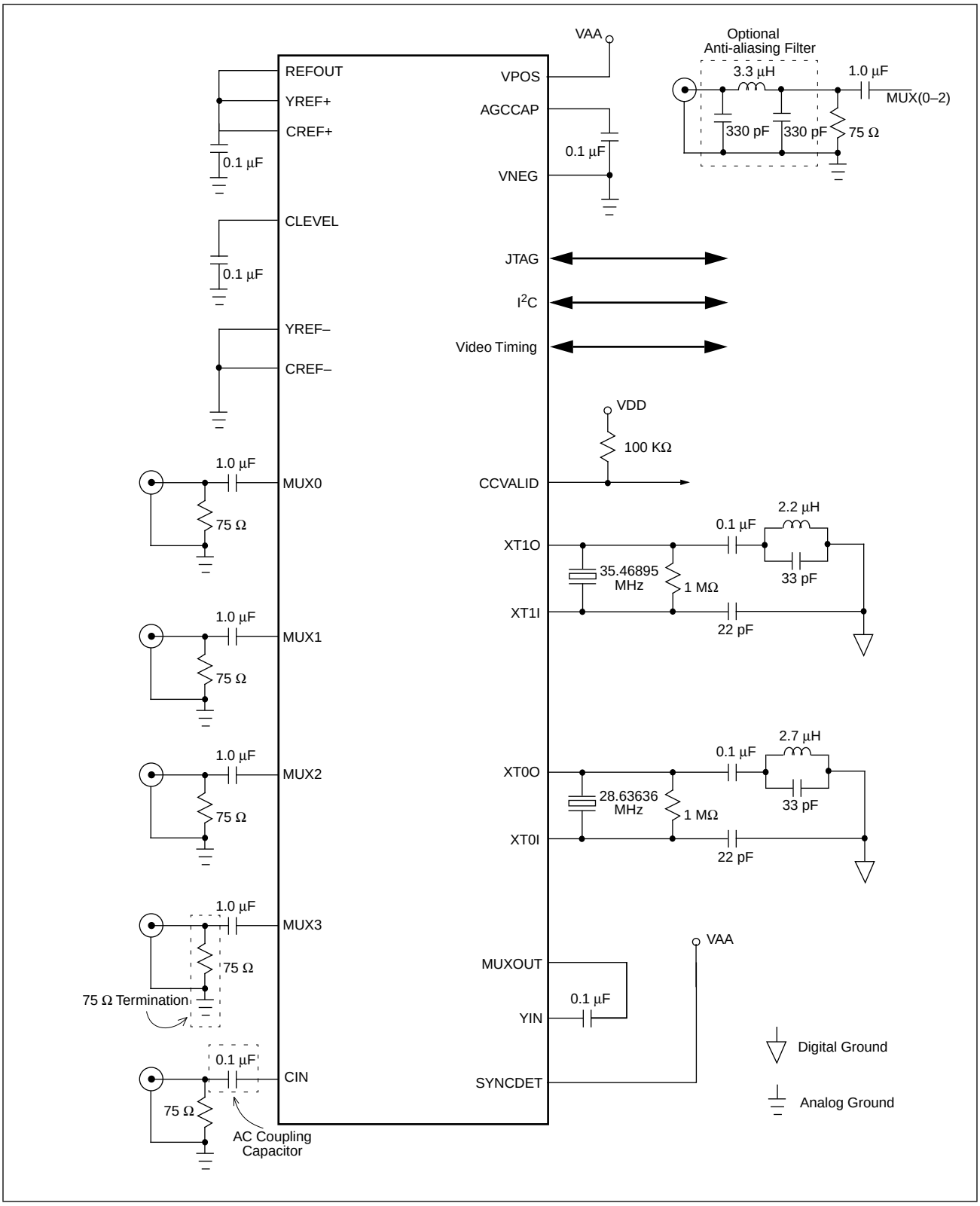
The REFOUT, CREF+ and YREF+ pins should be connected together as shown in Figure 27. In this configuration, the Bt829A controls the voltage for the top of the reference ladder for each A/D. The automatic gain control adjusts the YREF+ and CREF+ voltage levels until the back porch of the Y video input generates a digital code 0x38 from the A/D. If the video being digitized has a non-standard sync height to video height ratio, the digital code used for AGC may be changed by programming the ADC Interface Register (0x1A). Figure 28 illustrates Bt829A external circuitry with reduced passive components.

Figure 27. Bt829A Typical External Circuitry for Backward Compatibility with Bt829/827



Notes: (1). Not required for Bt829A/827A. Shown for backward compatibility with the Bt829/7.

Figure 28. Bt829A Typical External Circuitry (Reduced Passive Components)



Crystal Inputs and Clock Generation

The Bt829A has two pairs of pins: XT0I/XT0O and XT1I/XT1O. They are used to input a clock source. If both NTSC and PAL video are being digitized, both clock inputs must be implemented. The XT0 port is used to decode NTSC video and must be configured with a 28.63636 MHz source. The XT1 port is used to decode PAL video and must be configured with a 35.46895 MHz source.

If the Bt829A is configured to decode either NTSC or PAL but not both, then only one clock source must be provided to the chip and it must be connected to the XT0I/XT0O port. If a crystal input is not used, the crystal amplifiers are internally shut down to save power.

Crystals are specified as follows:

- 28.636363 MHz or 35.468950 MHz
- Third overtone
- Parallel resonant
- 30 pF load capacitance
- 50 ppm
- Series resistance 40 Ω or less

The following crystals are recommended for use with the Bt829A:

1 Standard Crystal
(818) 443-2121
2BAK28M636363GLE30A
2BAK35M468950GLE30A

2 MMD
(714) 444-1402
A30AA3-28.63636 MHz
A30AA3-35.46895 MHz

3 GED
(619) 591-4170
PKHC49-28.63636-.030-005-40R, 3rd overtone crystal
PKHC49-35.46895-.030-005-40R, 3rd overtone crystal

4 M-Tron
(800) 762-8800
MP-1 28.63636, 3rd overtone crystal
MP-1 35.46895, 3rd overtone crystal

5 Monitor
(619) 433-4510
MM49X3C3A-28.63636, 3rd overtone crystal
MM49X3C3A-35.46895, 3rd overtone crystal

6 CTS
(815) 786-8411
R3B55A30-28.63636, 3rd overtone crystal
R3B55A30-35.46895, 3rd overtone crystal

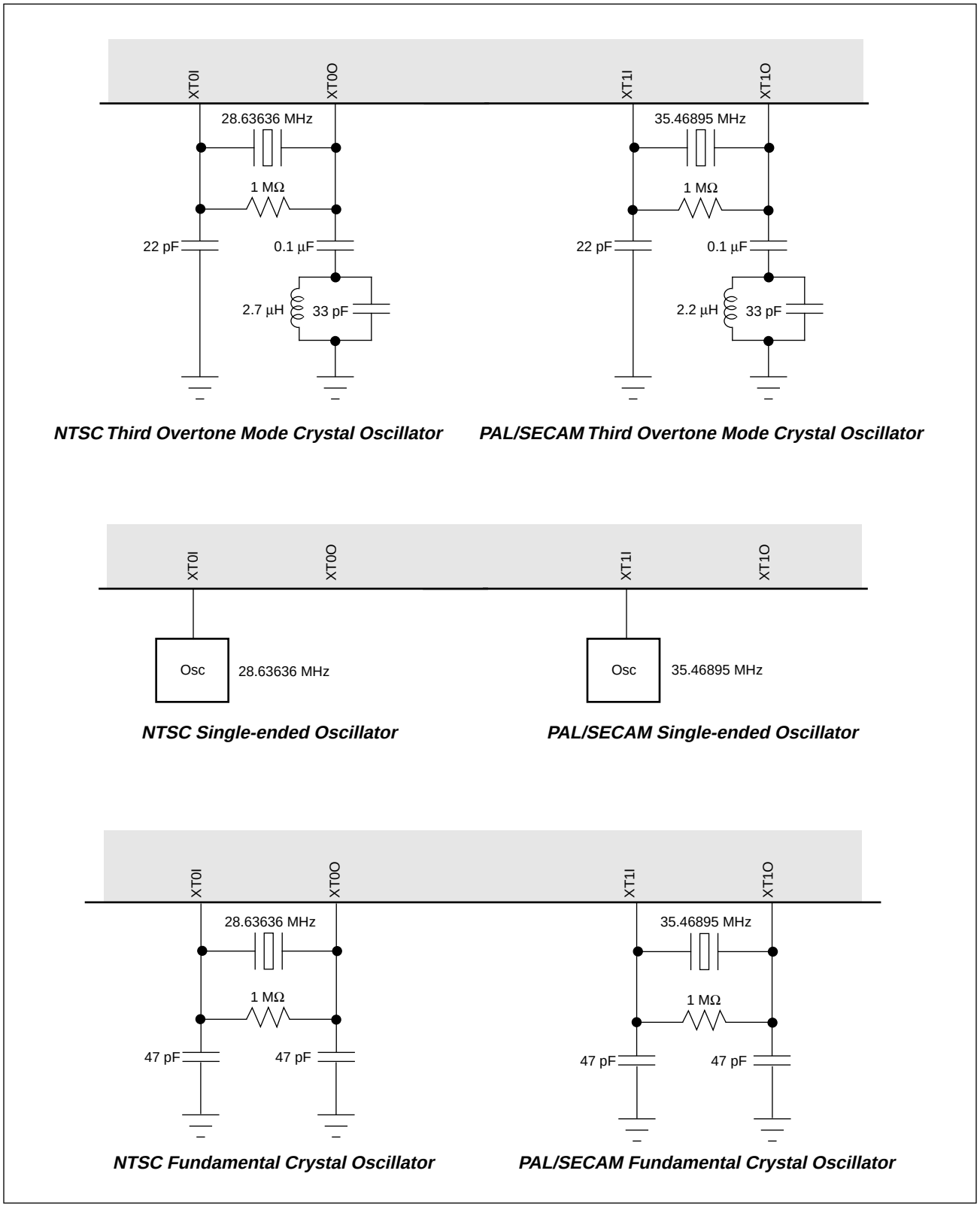
7 Fox
(813) 693-0099
HC49U-28.63636, 3rd overtone crystal
HC49U-35.46895, 3rd overtone crystal

The two clock sources may be configured with either single-ended oscillators, fundamental cut crystals or third overtone mode crystals, with parallel resonant. If single-ended oscillators are used they must be connected to XT0I and XT1I. The clock source options and circuit requirements are shown in Figure 29.

The clock source tolerance should be 50 parts-per-million (ppm) or less, but 100 ppm is acceptable. Devices that output CMOS voltage levels are required. The load capacitance in the crystal configurations may vary depending on the magnitude of board parasitic capacitance. The Bt829A is dynamic, and, to ensure proper operation, the clocks must always be running with a minimum frequency of 28.64 MHz.

The CLKx1 and CLKx2 outputs from the Bt829A are generated from XT0 and XT1 clock sources. CLKx2 operates at the crystal frequency (8xFsc) while CLKx1 operates at half the crystal frequency (4xFsc).

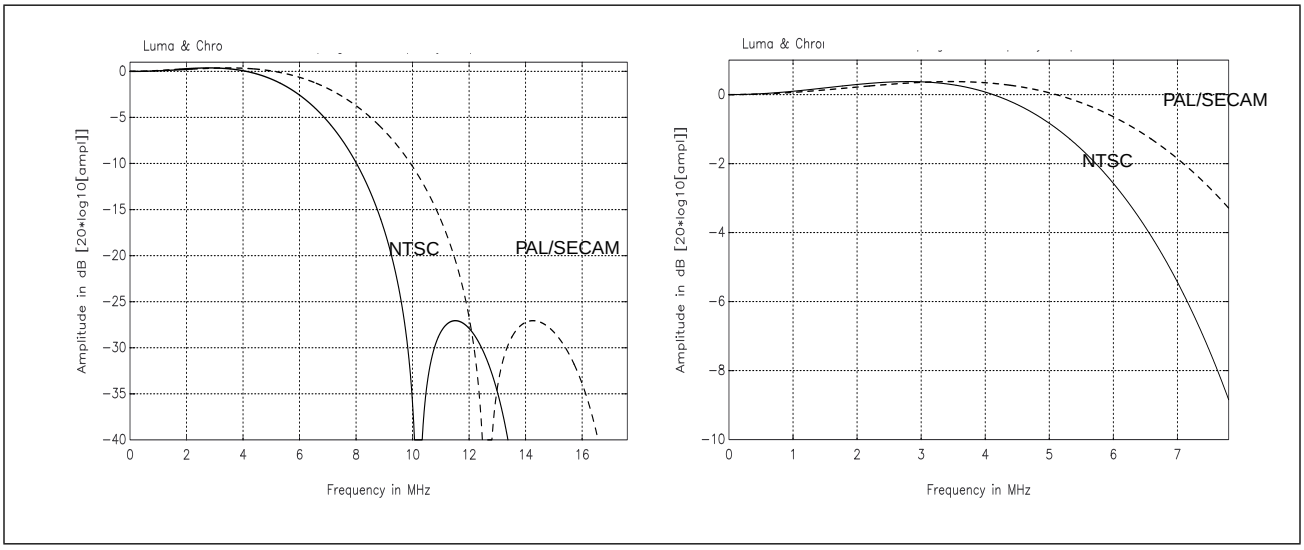
Figure 29. Clock Options



2X Oversampling and Input Filtering

To avoid aliasing artifacts, digitized video needs to be band-limited. Because the Bt829A samples at CLKx2 (8xFsc—over twice the normal rate), no filtering is required at the input to the A/Ds. The analog video needs to be band-limited to 14.32 MHz in NTSC and 17.73 MHz in PAL/SECAM mode. Normal video signals do not require additional external filtering. However, if noise or other signal content is expected above these frequencies, the optional anti-aliasing filter shown in Figure 27 may be included in the input signal path. After digitization, the samples are digitally low-pass filtered and then decimated to CLKx1. The response of the digital low-pass filter is shown in Figure 30. The digital low-pass filter provides the digital bandwidth reduction to limit the video to 6 MHz.

Figure 30. Luma and Chroma 2x Oversampling Filter



Output Interface

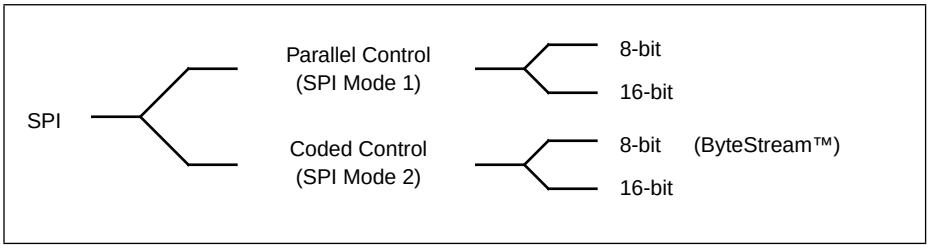
Output Interfaces

The Bt829A supports a Synchronous Pixel Interface (SPI). SPI can support 8-bit or 16-bit YCrCb 4:2:2 data streams.

Bt829A outputs all pixel and control data synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). Events such as $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ may also be encoded as control codes in the data stream to enable a reduced pin interface (ByteStream™).

Mode selections are controlled by the state of the OFORM register (0x12). Figure 31 shows a diagram summarizing the different operating modes. Each mode will be covered in detail individually. On power-up, the Bt829A automatically initializes to SPI mode 1, 16 bits wide.

Figure 31. Output Mode Summary



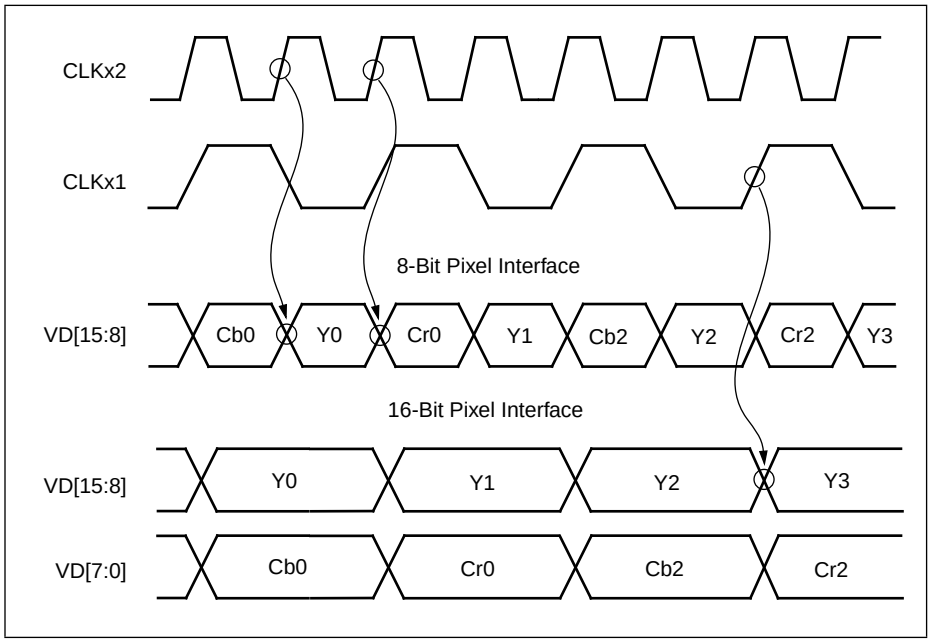
YCrCb Pixel Stream Format, SPI Mode 8- and 16-bit Formats

When the output is configured for an 8-bit pixel interface, the data is output on pins VD[15:8] with eight bits of chrominance data preceding eight bits of luminance data for each pixel. New pixel data is output on the pixel port after each rising edge of CLKx2. When the output is configured for the 16-bit pixel interface, the luminance data is output on VD[15:8], and the chrominance data is output on VD[7:0]. In 16-bit mode, the data is output with respect to CLKx1. See Table 7 for a summary of output interface configurations. The YCrCb 4:2:2 pixel stream follows the CCIR recommendation as illustrated in Figure 32.

Table 7. Pixel/Pin Map

16-bit Pixel Interface																
Pin Name	VD 15	VD 14	VD 13	VD 12	VD 11	VD 10	VD 9	VD 8	VD 7	VD 6	VD 5	VD 4	VD 3	VD 2	VD 1	VD 0
Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cr Cb 7	Cr Cb 6	Cr Cb 5	Cr Cb 4	Cr Cb 3	Cr Cb 2	Cr Cb 1	Cr Cb 0
8-bit Pixel Interface																
Pin Name	VD 15	VD 14	VD 13	VD 12	VD 11	VD 10	VD 9	VD 8	VD 7	VD 6	VD 5	VD 4	VD 3	VD 2	VD 1	VD 0
Y Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
C Data Bit	Cr Cb 7	Cr Cb 6	Cr Cb 5	Cr Cb 4	Cr Cb 3	Cr Cb 2	Cr Cb 1	Cr Cb 0								

Figure 32. YCrCb 4:2:2 Pixel Stream Format (SPI Mode, 8 and 16 Bits)



Synchronous Pixel Interface (SPI, Mode 1)

Upon reset, the Bt829A initializes to the SPI output Mode 1. In this mode, Bt829A outputs all horizontal and vertical blanking interval pixels in addition to the active pixels synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). Figure 33 illustrates Bt829A SPI-1. The basic timing relationships remain the same for the 16-bit or 8-bit modes. The 16-bit modes use CLKx1 as the reference, and the 8-bit modes use CLKx2. Figure 34 shows the video timing for SPI Mode 1.

Figure 33. Bt829A/827A Synchronous Pixel Interface, Mode 1 (SPI-1)

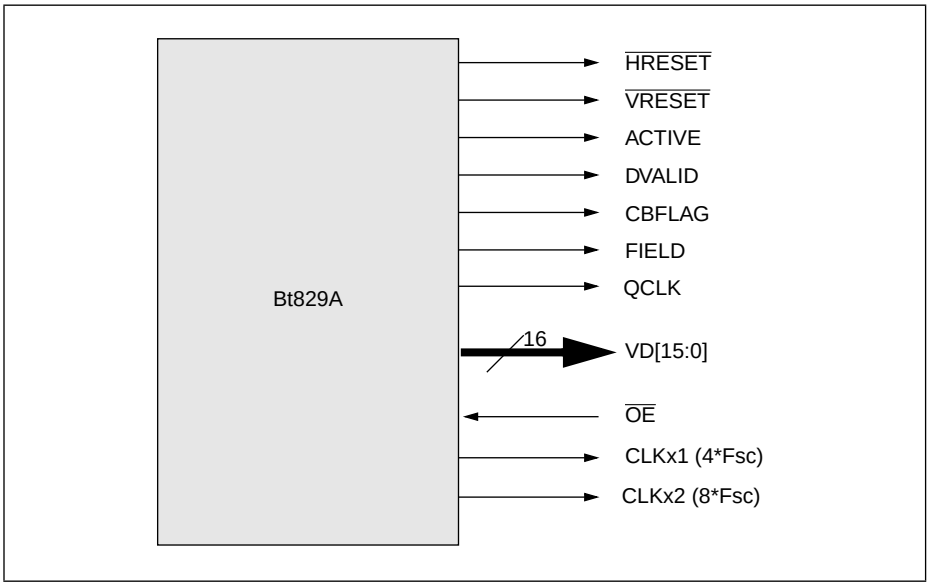
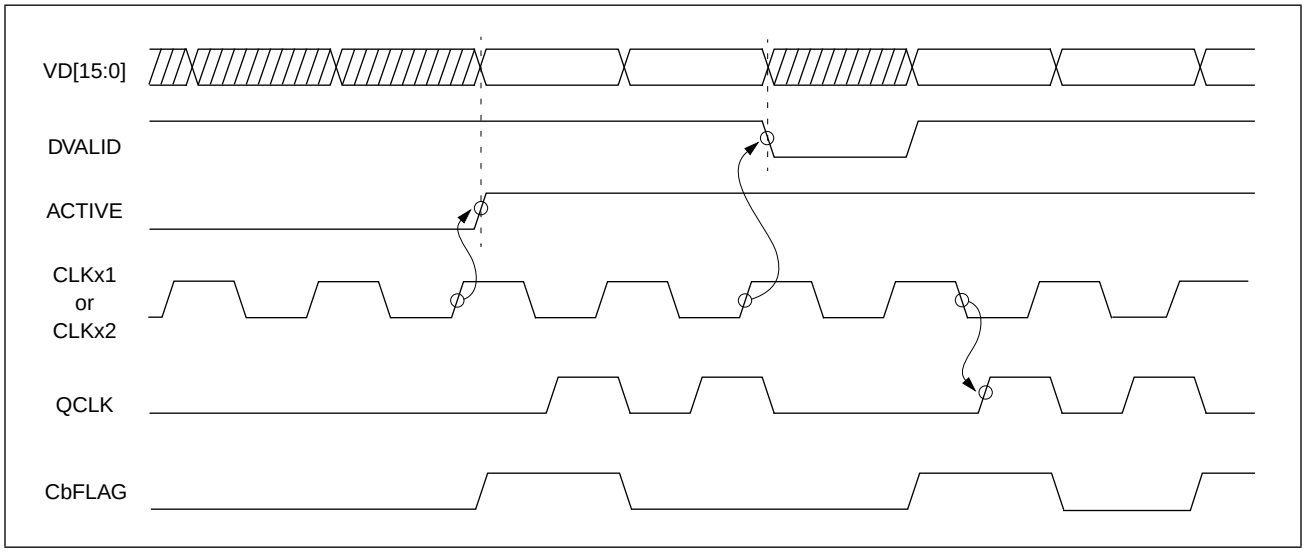


Figure 34. Basic Timing Relationships for SPI Mode 1



Synchronous Pixel Interface (SPI, Mode 2, ByteStream™)

In SPI Mode 2, the Bt829A encodes all video timing control signals onto the pixel data bus. ByteStream™ is the 8-bit version of this configuration. Because all timing data is included on the data bus, a complete interface to a video controller can be implemented in only nine pins: one for CLKx2 and eight for data.

When using coded control, the RANGE bit and the CODE bit must be programmed high. When the RANGE bit is high, the chrominance pixels (both Cr and Cb) are saturated to the range 2 to 253, and the luminance range is limited to the range 16 to 253. In SPI Mode 2, the chroma values of 255 and 254, and the luminance values of 0 to 15 are inserted as control codes to indicate video events (Table 8). A chroma value of 255 is used to indicate that the associated luma pixel is a control code; a pixel value of 255 also indicates that the CbFlag is high (i.e., the current pixel is a Cb pixel). Similarly, a pixel value of 254 indicates that the luma value is a control code, and the CbFlag is low (Cr pixel).

The first pixel of a line is guaranteed to be a Cb flag, however, due to code precedence relationships, the $\overline{\text{HRESET}}$ code may be delayed by one pixel, so $\overline{\text{HRESET}}$ can occur on a Cr or a Cb pixel. Also, at the beginning of a new field the relationship between $\overline{\text{VRESET}}$ and $\overline{\text{HRESET}}$ may be lost, typically with video from a VCR. As a result, $\overline{\text{VRESET}}$ can occur during either a Cb or a Cr pixel. Figure 35 demonstrates coded control for SPI mode 2 (ByteStream™).

Pixel data output ranges are shown in Table 9. Independent of RANGE, decimal 128 indicates zero color information for Cr and Cb. Black is decimal 16 when RANGE = 0, and code 0 when RANGE = 1.

Figures 36 and 37 illustrate videotiming for both SPI Modes 1 and 2.

Table 8. Description of the Control Codes in the Pixel Stream

Luma Value	Chroma Value	Video Event Description
0x00	0xFF 0xFE	This is an invalid pixel; last valid pixel was a Cb pixel. This is an invalid pixel; last valid pixel was a Cr pixel.
0x01	0xFF 0xFE	Cb pixel; last pixel was the last active pixel of the line. Cr pixel; last pixel was the last active pixel of the line.
0x02	0xFF 0xFE	Cb pixel; next pixel is the first active pixel of the line. Cr pixel; next pixel is the first active pixel of the line.
0x03	0xFF 0xFE	Cb pixel; HRESET of a vertical active line. Cr pixel; HRESET of a vertical active line.
0x04	0xFF 0xFE	Cb pixel; HRESET of a vertical blank line. Cr pixel; HRESET of a vertical blank line.
0x05	0xFF 0xFE	Cb pixel; VRESET followed by an even field. Cr pixel; VRESET followed by an even field.
0x06	0xFF 0xFE	Cb pixel; VRESET followed by an odd field. Cr pixel; VRESET followed by an odd field.

Figure 35. Data Output in SPI Mode 2 (ByteStream™)

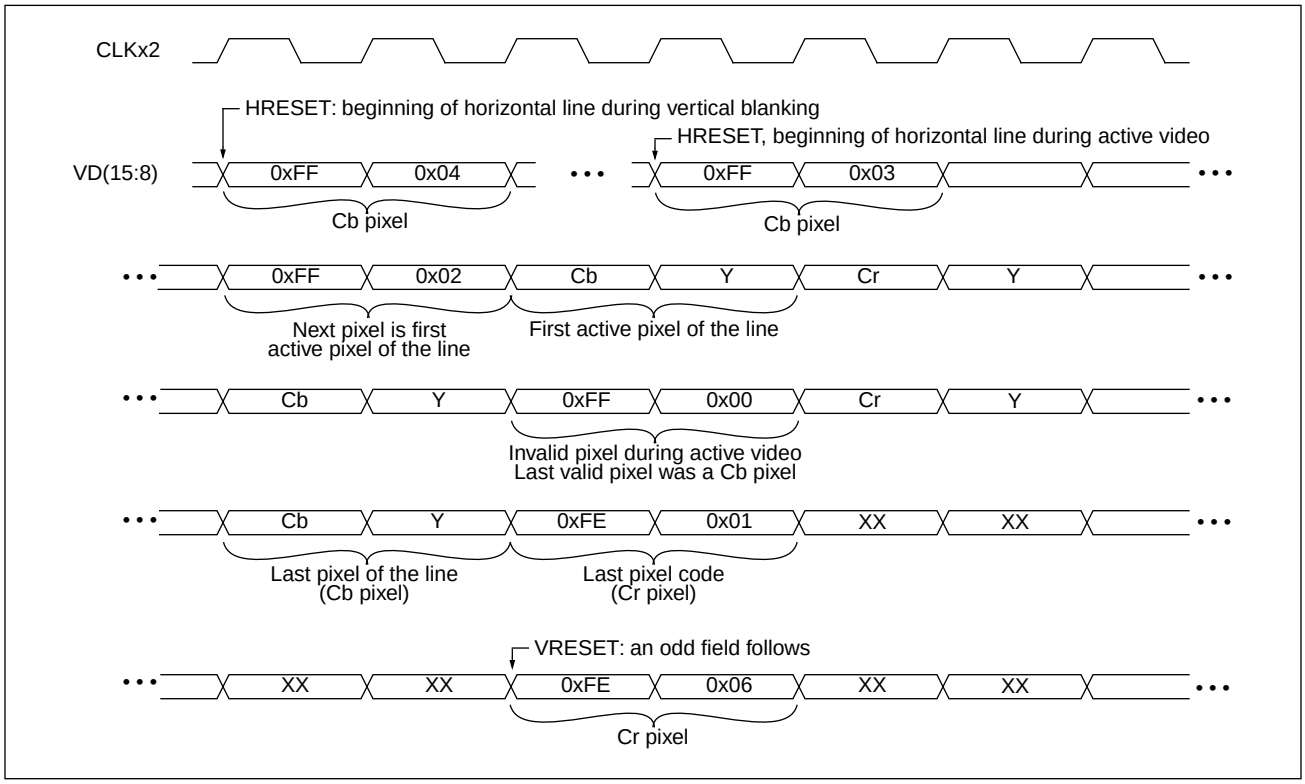
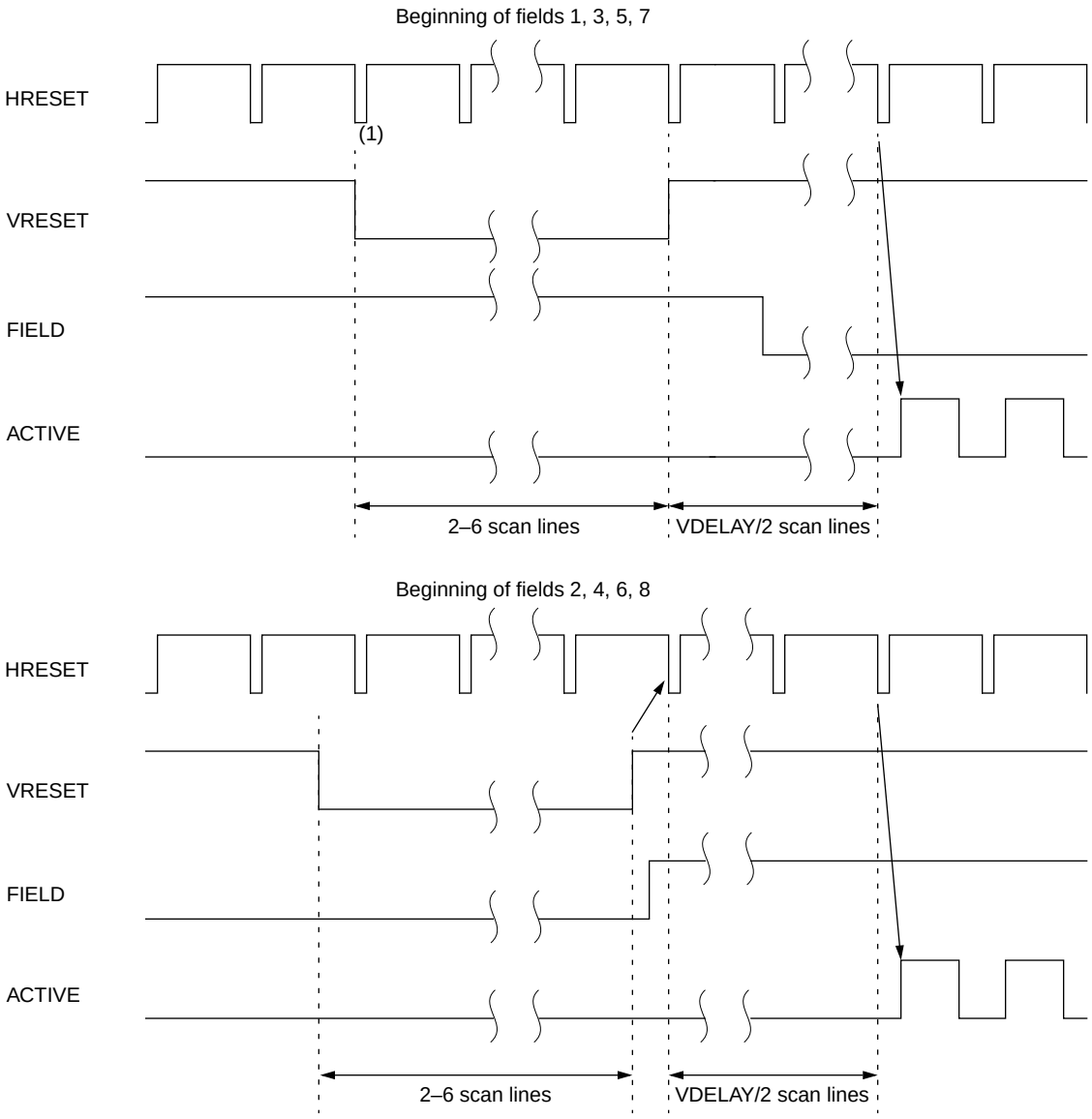


Figure 36. Video Timing in SPI Modes 1 and 2



Notes: (1). $\overline{\text{HRESET}}$ precedes $\overline{\text{VRESET}}$ by two clock cycles at the beginning of fields 1, 3, 5 and 7 to facilitate external field generation.
2. ACTIVE pin may be programmed to be composite ACTIVE or horizontal ACTIVE.
3. ACTIVE, $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$ and FIELD are shown here with their default polarity. The polarity is programmable via the VPOLE register.
4. FIELD transitions with the end of horizontal active video defined by HDELAY and HACTIVE.

Figure 37. Horizontal Timing Signals in the SPI Modes

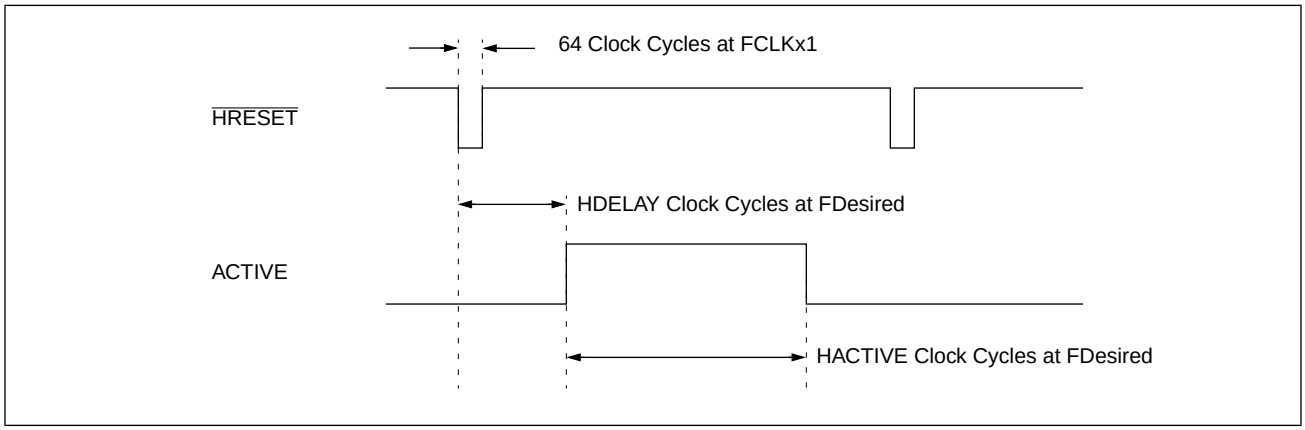


Table 9. Data Output Ranges

	RANGE = 0	RANGE = 1
Y	16 —> 235	0 —> 255
Cr	2 —> 253	2 —> 253
Cb	2 —> 253	2 —> 253

CCIR601 Compliance

When the RANGE bit is set to zero, the output levels are fully compliant with the CCIR601 recommendation. CCIR601 specifies that nominal video will have Y values ranging from 16 to 235, and Cr and Cb values ranging from 16 to 240. However, excursions outside this range are allowed to handle non-standard video. The only mandatory requirement is that 0 and 255 be reserved for timing information.

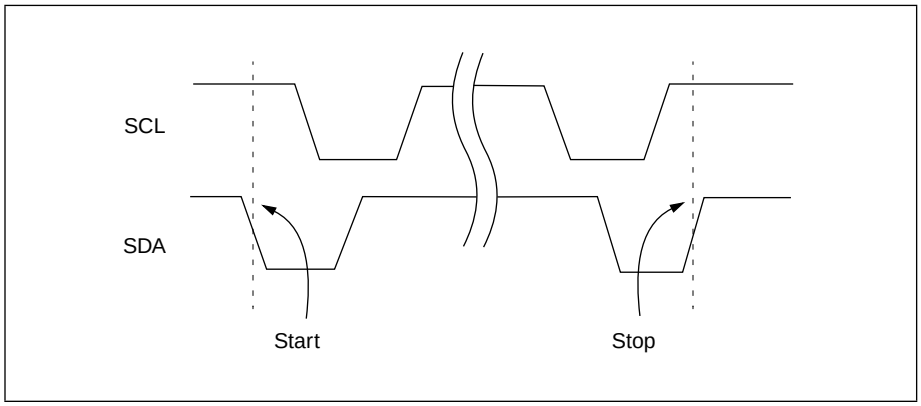
I²C Interface

The Inter-Integrated Circuit bus is a two-wire serial interface. Serial Clock (SCL) and Data Lines (SDA), are used to transfer data between the bus master and the slave device. The Bt829A can transfer data at a maximum rate of 100 kbits/s. The Bt829A operates as a slave device.

Starting and Stopping

The relationship between SCL and SDA is decoded to provide both a start and stop condition on the bus. To initiate a transfer on the I²C bus, the master must transmit a start pulse to the slave device. This is accomplished by taking the SDA line low while the SCL line is held high. The master should only generate a start pulse at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SDA line high while the SCL line is held high. The master may issue a stop pulse at any time during an I²C cycle. Since the I²C bus will interpret any transition on the SDA line during the high phase of the SCL line as a start or stop pulse, care must be taken to ensure that data is stable during the high phase of the clock. This is illustrated in Figure 38.

Figure 38. The Relationship between SCL and SDA



Addressing the Bt829A

An I²C slave address consists of two parts: a 7-bit base address and a single bit R/$\overline{W}$ command. The R/$\overline{W}$ bit is appended to the base address to form the transmitted I²C address, as shown in Figure 39 and Table 10.

Figure 39. I²C Slave Address Configuration

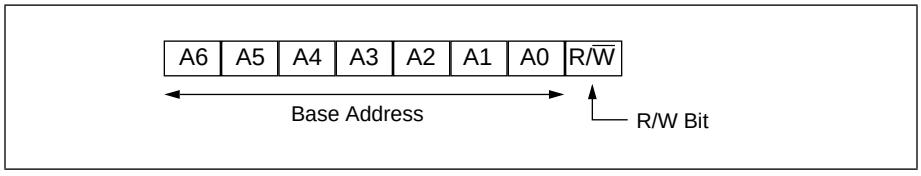


Table 10. Bt829A Address Matrix

I2CCS Pin	Bt829A Base	R/$\overline{W}$ Bit	Action
0	1000100	0	Write
	1000100	1	Read
1	1000101	0	Write
	1000101	1	Read

Reading and Writing

After transmitting a start pulse to initiate a cycle, the master must address the Bt829A. To do this, the master must transmit one of the four valid Bt829A addresses, Most Significant Bit (MSB) first. After transmitting the address, the master must release the SDA line during the low phase of the SCL and wait for an acknowledge. If the transmitted address matches the selected Bt829A address, the Bt829A will respond by driving the SDA line low, generating an acknowledge to the master. The master will sample the SDA line at the rising edge of the SCL line, and proceed with the cycle. If no device responds, including the Bt829A, the master transmits a stop pulse and ends the cycle.

If the slave address R/$\overline{W}$ bit was low (indicating a write) the master will transmit an 8-bit byte to the Bt829A, MSB first. The Bt829A will acknowledge the transfer and load the data into its internal address register. The master can now issue a stop command, a start command, or transfer another 8-bit byte, MSB first, to be loaded into the register pointed to by the internal address register. The Bt829A will then acknowledge the transfer and increment the address register in preparation for the next transfer. As before, the master may now issue a stop command, a start command, or transfer another 8 bits to be loaded into the next location.

If the slave address R/$\overline{W}$ bit was high (indicating a read) the Bt829A will transfer the contents of the register pointed to by its internal address register, MSB first. The master should acknowledge the receipt of the data and pull the SDA line low. As with the write cycle, the address register will be auto-incremented in preparation for the next read.

To stop a read transfer, the host must *not* acknowledge the last read cycle. The Bt829A will then release the data bus in preparation for a stop command. If an acknowledge is received, the Bt829A will proceed to transfer the next register.

When the master generates a read from the Bt829A, the Bt829A will start its transfer from whatever location is currently loaded in the address register. Since the address register might not contain the address of the desired register, the master should execute a write cycle, setting the address register to the desired location. After receiving an acknowledge for the transfer of the data into the address register, the master should initiate a read of the Bt829A by starting a new I^2C cycle with an appropriate read address. The Bt829A now transfers the contents of the desired register.

For example, to read register 0x0A, Brightness Control, the master should start a write cycle with an I²C address of 0x88 or 0x8A. After receiving an acknowledge from the Bt829A, the master should transmit the desired address, 0x0A. After receiving an acknowledge, the master should then start a read cycle with an I²C slave address of 0x89 or 0x8B. The Bt829A will then acknowledge and transfer the contents of register 0x0A. There is no need to issue a stop command after the write cycle. The Bt829A will detect the repeated start command, and start a new I²C cycle. This process is illustrated in Table 11 and Figure 40.

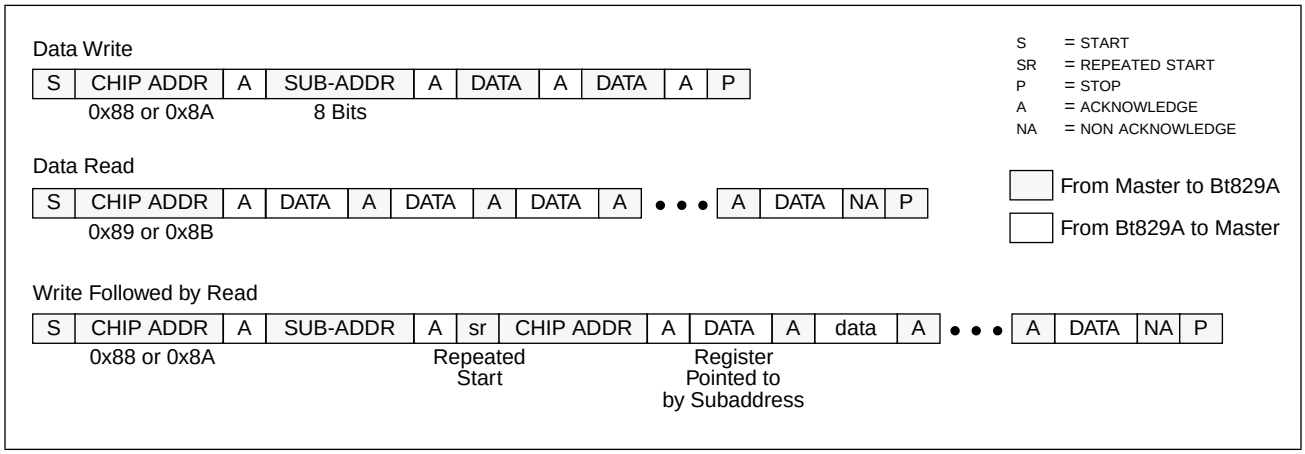
For detailed information on the I²C bus, refer to *"The I²C-Bus Reference Guide,"* reprinted by Rockwell.

Table 11. Example I²C Data Transactions

Master	Data Flow	Bt829A	Comment
Write to Bt829A			
I²C Start	——>		Master sends Bt829A chip address, i.e., 0x88 or 0x8A.
		ACK	Bt829A generates ACK on successful receipt of chip address.
Sub-address	——>		Master sends sub-address to Bt829A.
		ACK	Bt829A generates ACK on successful receipt of sub-address.
Data(0)	——>		Master sends first data byte to Bt829A.
		ACK(0)	Bt829A generates ACK on successful receipt of 1st data byte.
.	——>	.	
.	——>	.	
.	——>	.	
Data(n)	——>		Master sends nth data byte to Bt829A.
		ACK(n)	Bt829A generates ACK on successful receipt of nth data byte.
I²C Stop			Master generates STOP to end transfer.
Read from Bt829A			
I²C Start	——>		Master sends Bt829A chip address, i.e., 0x89 or 0x8B.
		ACK	Bt829A generates ACK on successful receipt of chip address.
	<——	Data(0)	Bt829A sends first data byte to Master.
ACK(0)			Master generates ACK on successful receipt of 1st data byte.
.	<——	.	
.	<——	.	
.	<——	.	
	<——	Data(n-1)	Bt829A sends (n-1)th data byte to Master.
ACK(n-1)			Master generates ACK on successful receipt of (n-1)th data byte.
	<——	Data(n)	Bt829A sends nth data byte to Master.
NO ACK			Master does not acknowledge nth data byte.
I²C Stop			Master generates STOP to end transfer.

where: I²C Start = I²C start condition and Bt829A chip address (including the R/$\overline{W}$ bit).
Sub-address = the 8-bit sub-address of the Bt829A register, MSB first.
Data(n) = the data to be transferred to/from the addressed register.
I²C Stop = I²C stop condition.

Figure 40. I²C Protocol Diagram



Software Reset

The contents of the control registers may be reset to their default values by issuing a software reset. A software reset can be accomplished by writing any value to subaddress 0x1F. A read of this location will return an undefined value.

JTAG Interface

Need for Functional Verification

As the complexity of imaging chips increases, the need to easily access individual chips for functional verification is becoming vital. The Bt829A has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group. Conforming to IEEE P1149.1 “Standard Test Access Port and Boundary Scan Architecture,” the Bt829A has dedicated pins that are used for testability purposes only.

JTAG Approach to Testability

JTAG’s approach to testability utilizes boundary scan cells placed at each digital pin and digital interface (a digital interface is the boundary between an analog block and a digital block within the Bt829A). All cells are interconnected into a boundary scan register that applies or captures test data to verify functionality of the integrated circuit. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of five dedicated pins comprising the Test Access Port (TAP). These pins are Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), Test Data Out (TDO) and Test Reset ($\overline{\text{TRST}}$). The $\overline{\text{TRST}}$ pin will reset the JTAG controller when pulled low at any time. Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these five TAP pins. With boundary scan cells at each digital interface and pin, the Bt829A has the capability to apply and capture the respective logic levels. Because all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt829A from other components on the board, the user has easy access to all Bt829A digital pins and digital interfaces through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

Optional Device ID Register

The Bt829A has the optional device identification register defined by the JTAG specification. This register contains information concerning the revision, actual part number, and manufacturers identification code specific to Rockwell. This register can be accessed through the TAP controller via an optional JTAG instruction. Refer to Table 12.

Table 12. Device Identification Register

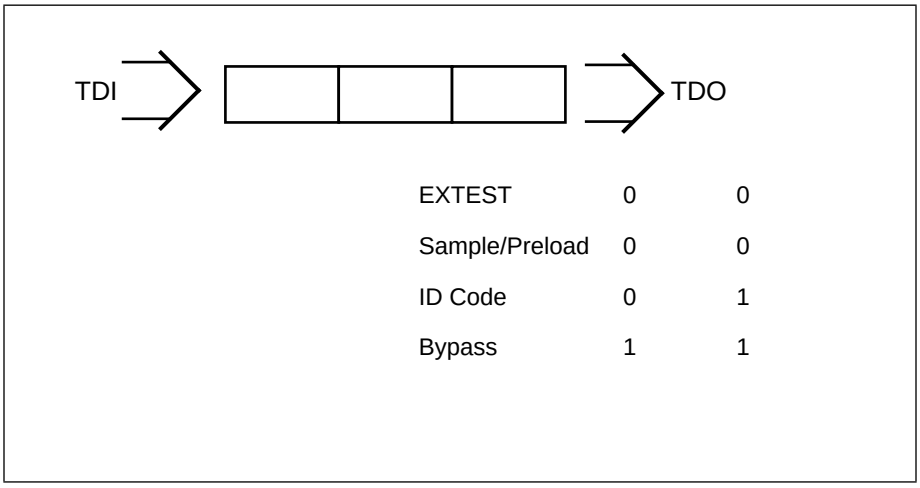
Version	Part Number	Manufacturer ID	
X X X X	0 0 0 0 0 0 1 1 0 0 1 1 1 1 0 1	0 0 0 1 1 0 1 0 1 1 0 1	
0	0829, 0x033D	0x0D6	
4 Bits	16 Bits	11 Bits	
Note: The part number remains the same for both parts: Bt829A and Bt827A.			

Verification with the Tap Controller

A variety of verification procedures can be performed through the TAP controller. Using a set of four instructions, the Bt829A can verify board connectivity at all digital interfaces and pins. The instructions can be accessed by using a state machine standard to all JTAG controllers and are Sample/Preload, Extest, ID Code, and Bypass (see Figure 41). Refer to the IEEE P1149.1 specification for details concerning the Instruction Register and JTAG state machine.

Rockwell has created a BSDL with the AT&T BSD Editor. Should JTAG testing be implemented, a disk with an ASCII version of the complete BSDL file can be obtained by contacting your local Rockwell sales office.

Figure 41. Instruction Register

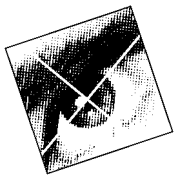


Example BSDL Listing

```
attribute BOUNDARY_REGISTER of Bt829A : entity is
        "   0 (BC_1, *, control, 1)," &
        "   1 (BC_1, *, internal, 1)," &
        "   2 (BC_1, *, control, 1)," &
        "   3 (BC_1, *, internal, X)," &
        "   4 (BC_1, *, internal, X)," &
        "   5 (BC_1, *, internal, X)," &
        "   6 (BC_1, *, internal, X)," &
        "   7 (BC_1, *, internal, X)," &
        "   8 (BC_1, *, internal, X)," &
        "   9 (BC_1, *, internal, X)," &
        "  10 (BC_1, *, internal, X)," &
        "  11 (BC_1, *, internal, X)," &
        "  12 (BC_1, *, internal, X)," &
        "  13 (BC_1, *, internal, 0)," &
        "  14 (BC_1, *, internal, 0)," &
        "  15 (BC_1, *, internal, 0)," &
        "  16 (BC_1, *, internal, 0)," &
        "  17 (BC_1, *, internal, 0)," &
        "  18 (BC_1, *, internal, 0)," &
        "  19 (BC_1, *, internal, 0)," &
        "  20 (BC_1, *, internal, 0)," &
        "  21 (BC_1, *, internal, 0)," &
        "  22 (BC_1, *, internal, 0)," &
        "  23 (BC_1, *, internal, 0)," &
        "  24 (BC_1, *, internal, 0)," &
        "  25 (BC_1, *, internal, 0)," &
        "  26 (BC_1, *, internal, 0)," &
        "  27 (BC_1, *, internal, 0)," &
        "  28 (BC_1, *, control, 0)," &
        "  29 (BC_1, FIELD, output3, X, 28, 0, Z)," &
        "  30 (BC_1, NVRESET, output3, X, 28, 0, Z)," &
        "  31 (BC_1, XTFMT, input, X)," &
        "  32 (BC_1, NHRESET, output3, X, 28, 0, Z)," &
        "  33 (BC_1, ACTIVE, output3, X, 28, 0, Z)," &
        "  34 (BC_1, DVALID, output3, X, 28, 0, Z)," &
        "  35 (BC_1, VACTIVE, output3, X, 28, 0, Z)," &
        "  36 (BC_1, TST, output2, 0, 36, 0, Weak1)," &
        "  37 (BC_1, *, internal, X)," &
        "  38 (BC_1, CBFLAG, output3, X, 28, 0, Z)," &
        "  39 (BC_3, NVSEN, input, X)," &
        "  40 (BC_1, PWRDN, input, X)," &
        "  41 (BC_1, QCLK, output3, X, 28, 0, Z)," &
        "  42 (BC_1, CLKX1, output3, X, 28, 0, Z)," &
        "  43 (BC_1, NOE, input, 1)," &
        "  44 (BC_1, CLKX2, output3, X, 28, 0, Z)," &
        "  45 (BC_1, VDB(13), output3, X, 28, 0, Z)," &
```

```
                    “  46 (BC_1, VDB(14), output3, X, 28, 0, Z),” &
                    “  47 (BC_1, VDB(15), output3, X, 28, 0, Z),” &
                    “  48 (BC_1, VDB(8), output3, X, 28, 0, Z),” &
                    “  49 (BC_1, VDB(9), output3, X, 28, 0, Z),” &
                    “  50 (BC_1, VDB(10), output3, X, 28, 0, Z),” &
                    “  51 (BC_1, VDB(11), output3, X, 28, 0, Z),” &
                    “  52 (BC_1, VDB(12), output3, X, 28, 0, Z),” &
                    “  53 (BC_1, *, internal, X),” &
                    “  54 (BC_1, XT0I, input, X),” &
                    “  55 (BC_1, I2CCS, input, X),” &
                    “  56 (BC_1, NRST, input, X),” &
                    “  57 (BC_1, *, internal, X),” &
                    “  58 (BC_1, XT1I, input, X),” &
                    “  59 (BC_1, SDA, output2, 0, 59, 1, Pull1),” &
                    “  60 (BC_1, SDA, input, X),” &
                    “  61 (BC_1, SCL, input, X),” &
                    “  62 (BC_1, VDA(3), output3, X, 0, 1, Z),” &
                    “  63 (BC_1, VDA(3), input, X),” &
                    “  64 (BC_1, VDA(4), output3, X, 2, 1, Z),” &
                    “  65 (BC_1, VDA(4), input, X),” &
                    “  66 (BC_1, VDA(5), output3, X, 2, 1, Z),” &
                    “  67 (BC_1, VDA(5), input, X),” &
                    “  68 (BC_1, VDA(6), output3, X, 2, 1, Z),” &
                    “  69 (BC_1, VDA(6), input, X),” &
                    “  70 (BC_1, VDA(7), output3, X, 2, 1, Z),” &
                    “  71 (BC_1, VDA(7), input, X),” &
                    “  72 (BC_1, VDA(0), output3, X, 0, 1, Z),” &
                    “  73 (BC_1, VDA(0), input, X),” &
                    “  74 (BC_1, VDA(1), output3, X, 0, 1, Z),” &
                    “  75 (BC_1, VDA(1), input, X),” &
                    “  76 (BC_1, VDA(2), output3, X, 0, 1, Z),” &
                    “  77 (BC_1, VDA(2), input, X),” &
                    “  78 (BC_1, TWREN, input, X),” &
                    “  79 (BC_0, *, internal, 0),” &
                    “  80 (BC_0, *, internal, 0)”;

end Bt829A;
```



PC BOARD LAYOUT CONSIDERATIONS

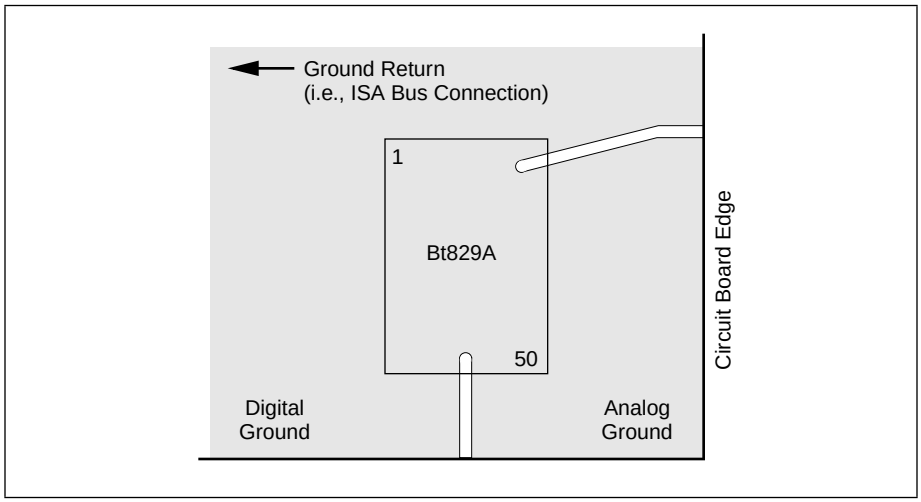
The layout should be optimized for lowest noise on the Bt829A power and ground lines by shielding the digital inputs and outputs and providing good decoupling. The lead length between groups of power and ground pins should be minimized to reduce inductive ringing.

Ground Planes

The ground plane area should encompass all Bt829A ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt829A, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt829A.

The Bt829A has digital grounds (GND) and analog grounds (AGND and VNEG). The layout for the ground plane should be such that the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. Also, the return path for the current should be through the digital plane. See Figure 42 for an example of ground plane layout.

Figure 42. Example Ground Plane Layout

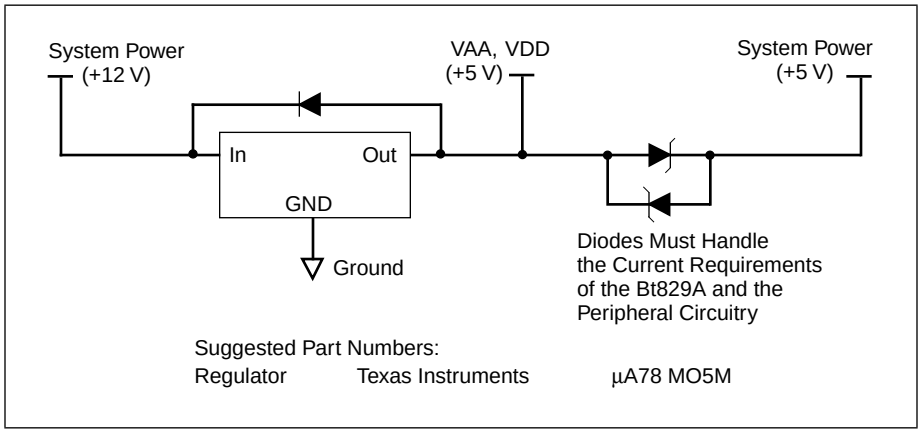


Power Planes

The power plane area should encompass all Bt829A power pins, voltage reference circuitry, power supply bypass circuitry for the Bt829A, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt829A.

The Bt829A has digital power (VDD) and analog power (VAA and VPOS). The layout for the power plane should be such that the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. Also, the return path for the current should be through the digital plane. This is the same layout as shown for the ground plane (Figure 42). When using a regulator, circuitry must be included to ensure proper power sequencing. The circuitry shown in Figure 43 illustrates this circuitry layout.

Figure 43. Optional Regulator Circuitry



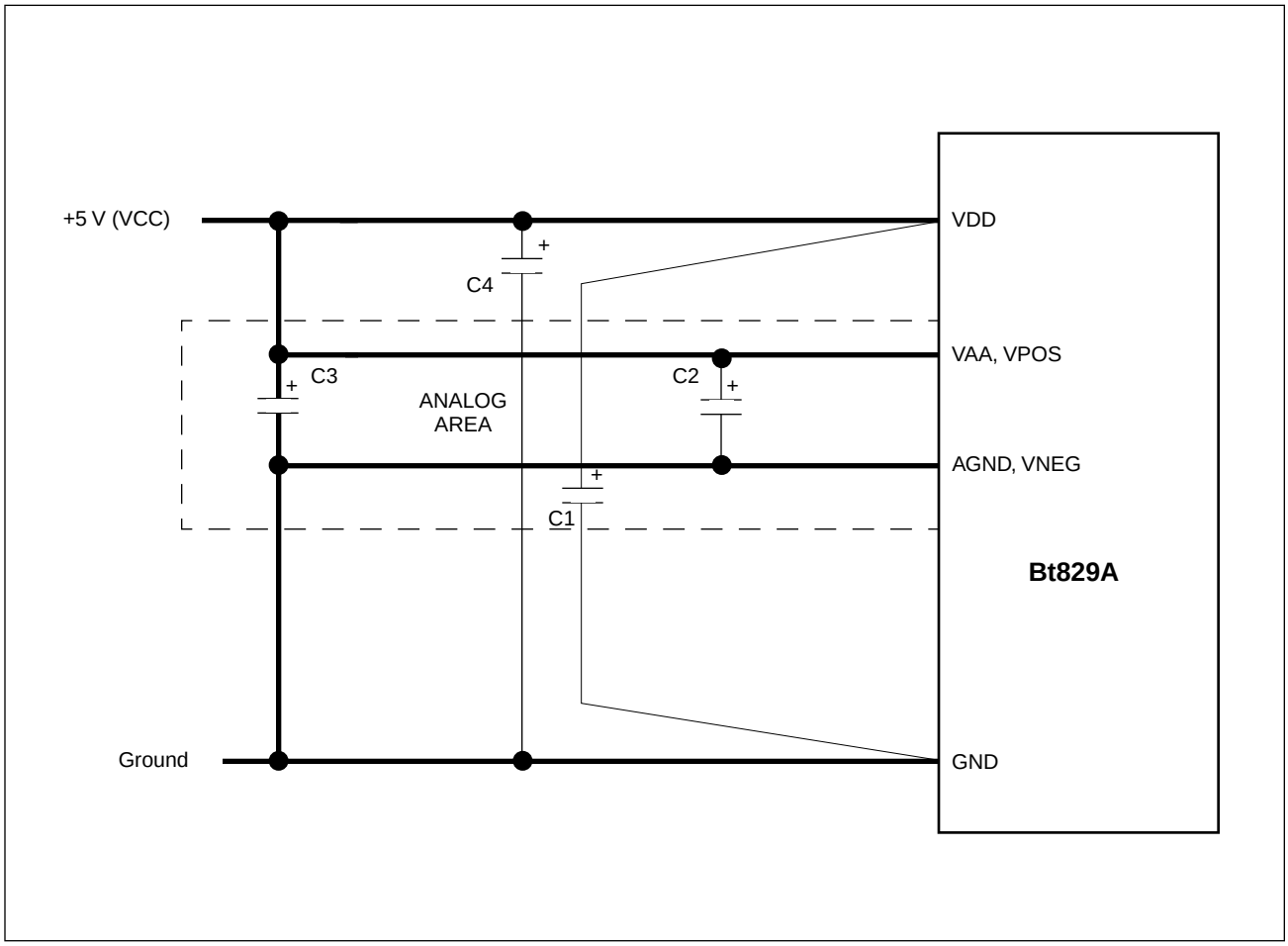
Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

Each group of VAA and VDD pins should have a 0.1 µF ceramic bypass capacitor to ground, located as close as possible to the device.

Additionally, 10 µF capacitors should be connected between the analog power and ground planes, as well as between the digital power and ground planes. These capacitors are at the same electrical potential, but provide additional decoupling by being physically close to the Bt829A power and ground planes. See Figure 44 for additional information about power supply decoupling.

Figure 44. Typical Power and Ground Connection Diagram and Parts List



Location	Description	Vendor Part Number
C1, C2(1)	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3, C4(2)	10 µF tantalum capacitor	Mallory CSR13G106KM

Notes: (1). A 0.1 µF capacitor should be connected between each group of power pins and ground as close to the device as possible (ceramic chip capacitors are preferred).
(2). The 10 µF capacitors should be connected between the analog supply and the analog ground, as well as the digital supply and the digital ground. These should be connected as close to the Bt829A as possible.
3. Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt829A.

Digital Signal Interconnect

The digital signals of the Bt829A should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the YIN and CIN inputs.

Also, high-speed TTL signals should not be routed close to the analog signals to minimize noise coupling.

Latch-up Avoidance

Latch-up is a failure mechanism inherent to any CMOS device. It is triggered by static or impulse voltages on any signal input pin exceeding the voltage on the power pins by more than 0.5 V, or falling below the GND pins by more than 0.5 V. Latch-up can also occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

In some cases, devices with mixed signal interfaces, such as the Bt829A, can appear more sensitive to latch-up. In reality, this is not the case. However, mixed signal devices tend to interact with peripheral devices such as video monitors or cameras that are referenced to different ground potentials, or apply voltages to the device prior to the time that its power system is stable. This interaction sometimes creates conditions amenable to the onset of latch-up.

To maintain a robust design with the Bt829A, the following precautions should be taken:

- Apply power to the device before or at the same time as the interface circuitry.
- Do not apply voltages below GND–0.5 V, or higher than VAA+0.5 V to any pin on the device. Do not use negative supply op-amps or any other negative voltage interface circuitry. All logic inputs should be held low until power to the device has settled to the specified tolerance.
- Connect all VDD, VAA and VPOS pins together through a low impedance plane.
- Connect all GND, AGND and VNEG pins together through a low impedance plane.

Sample Schematics

Figures 45 through 47c are example schematics which detail the interface of the Bt829A to Cirrus Logic, S3, and Trident VGA controllers. For interfacing to ATI VGA controllers, please contact ATI Technologies. For interfacing to all other VGA controllers, please contact your local Rockwell Semiconductor sales office.

Figure 45. Bt829/Cirrus Logic 544x VGA Interface Schematic

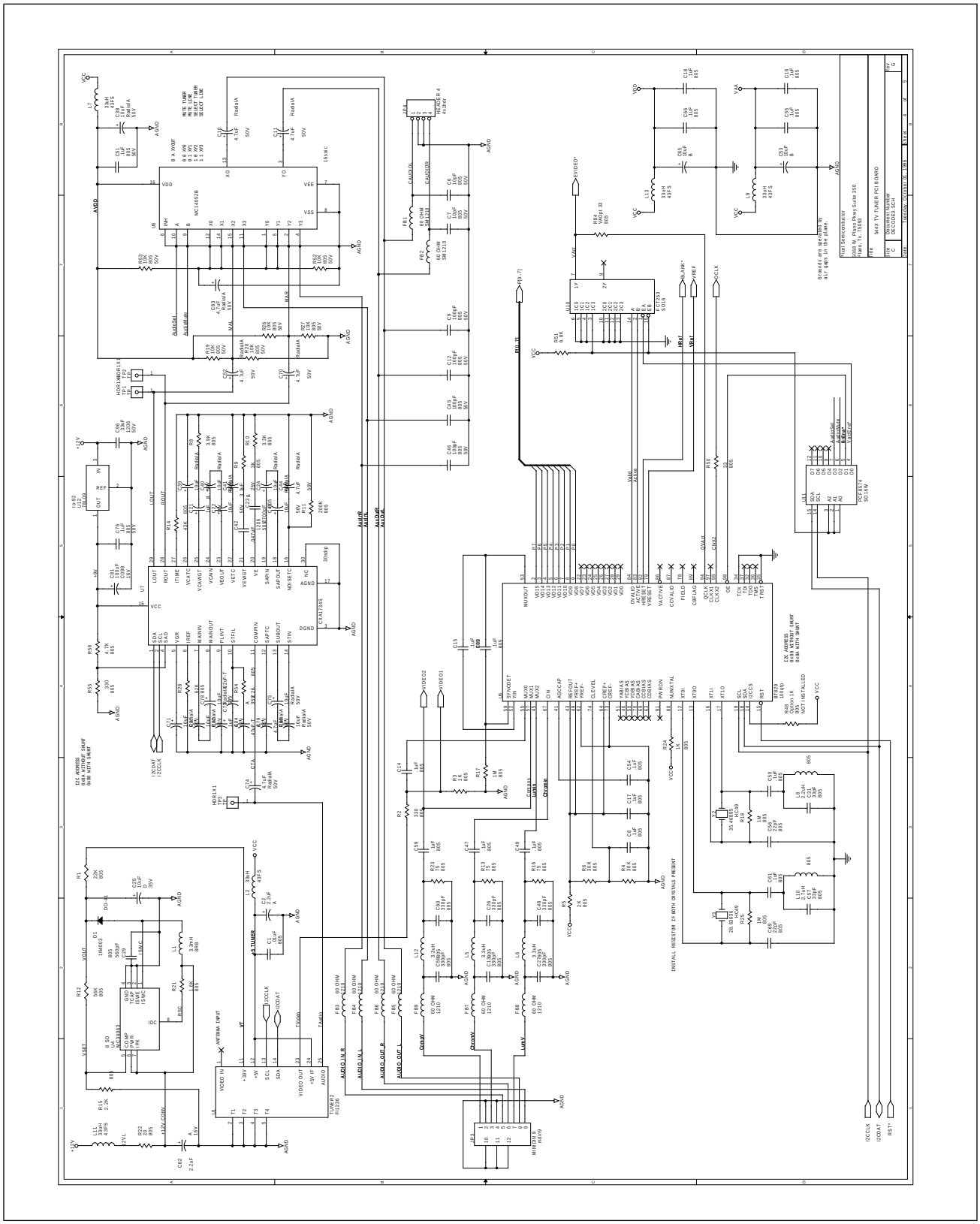


Figure 46a.Bt829/S3 Virge 8-Bit Interface Schematic - Video Input Detail

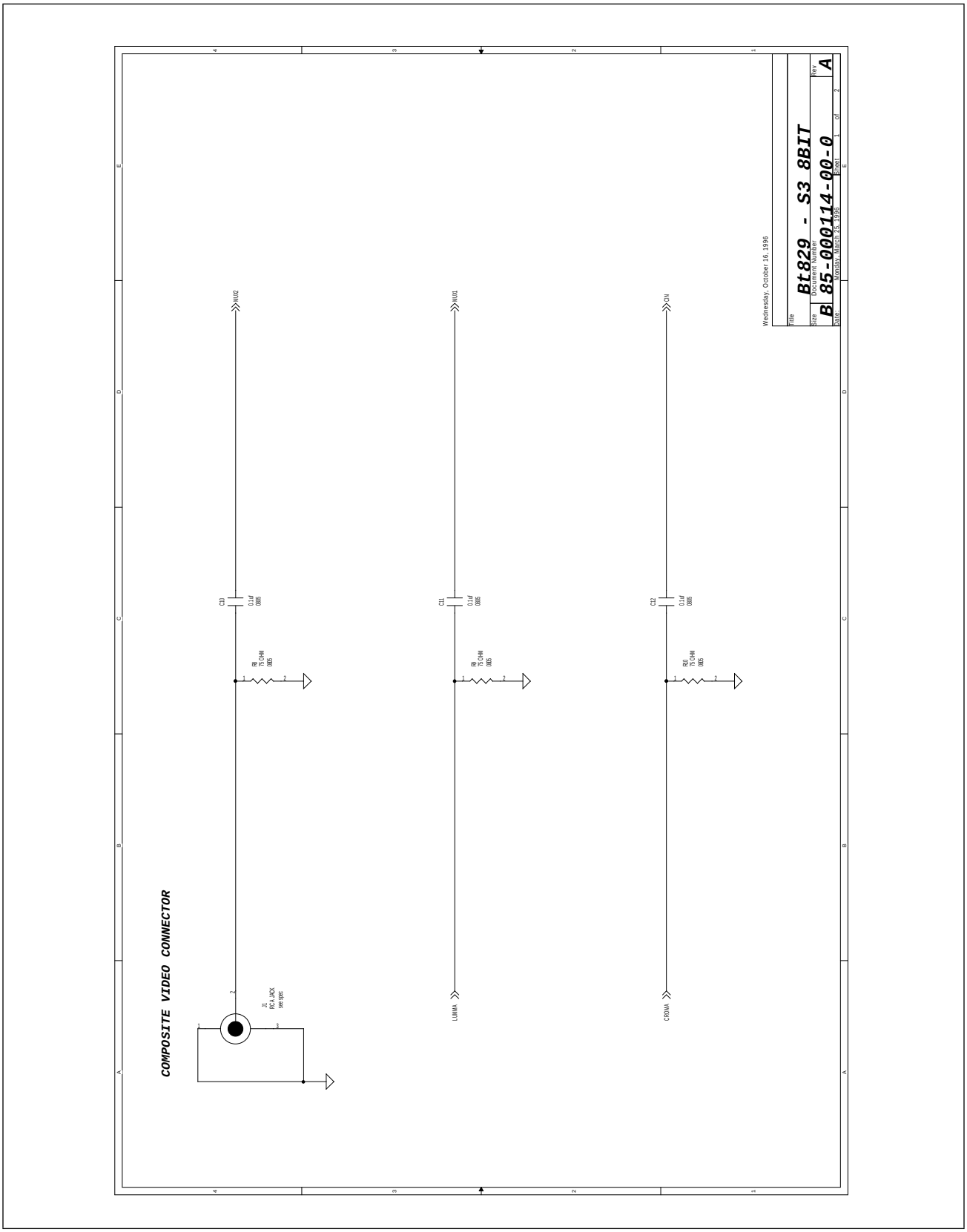


Figure 46b.Bt829/S3 Virge 8-Bit Interface Schematic - Bt829 Detail

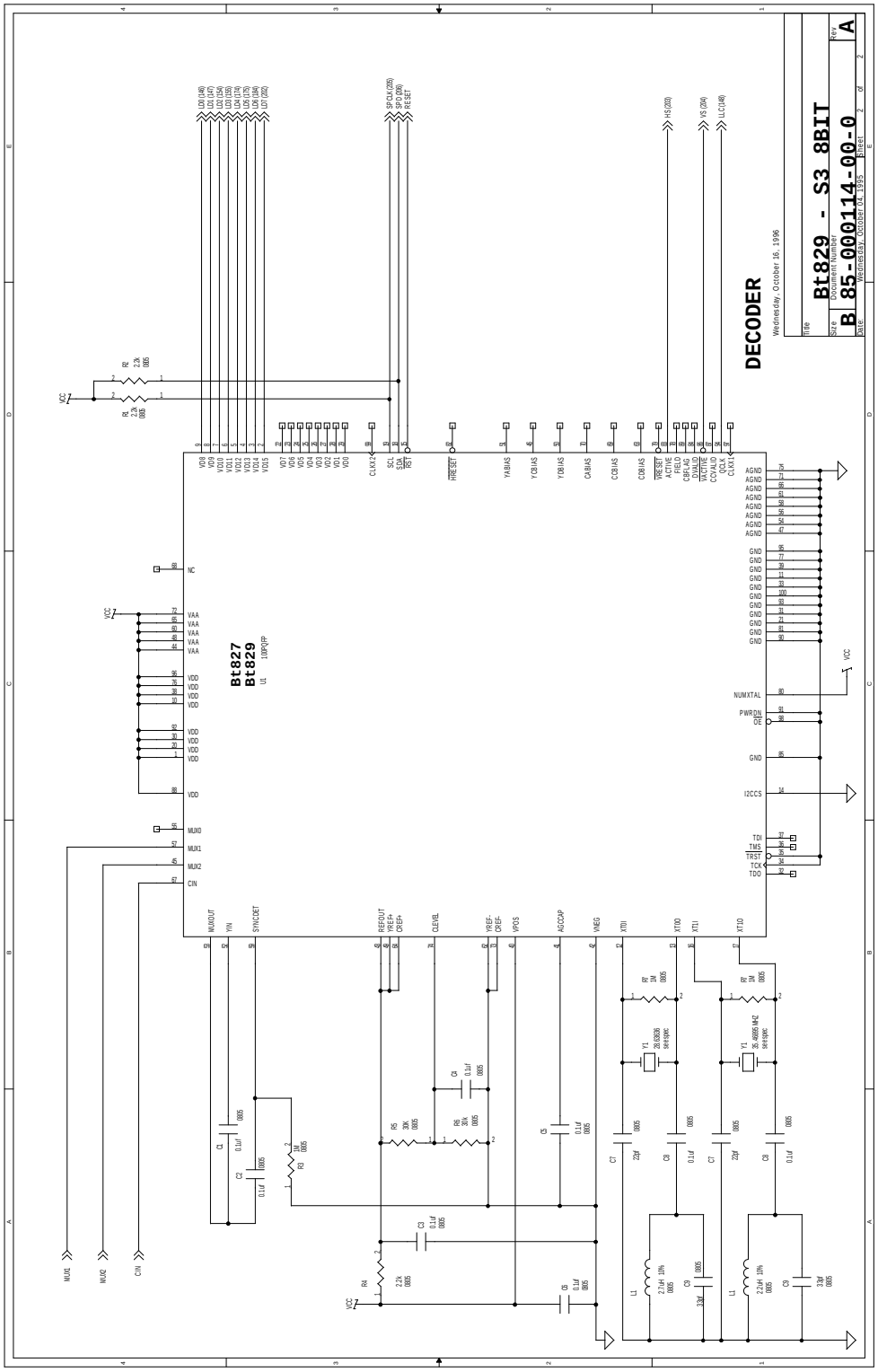


Figure 47a.Bt829/Trident VGA Interface Schematic - TV Tuner and Video Input Detail

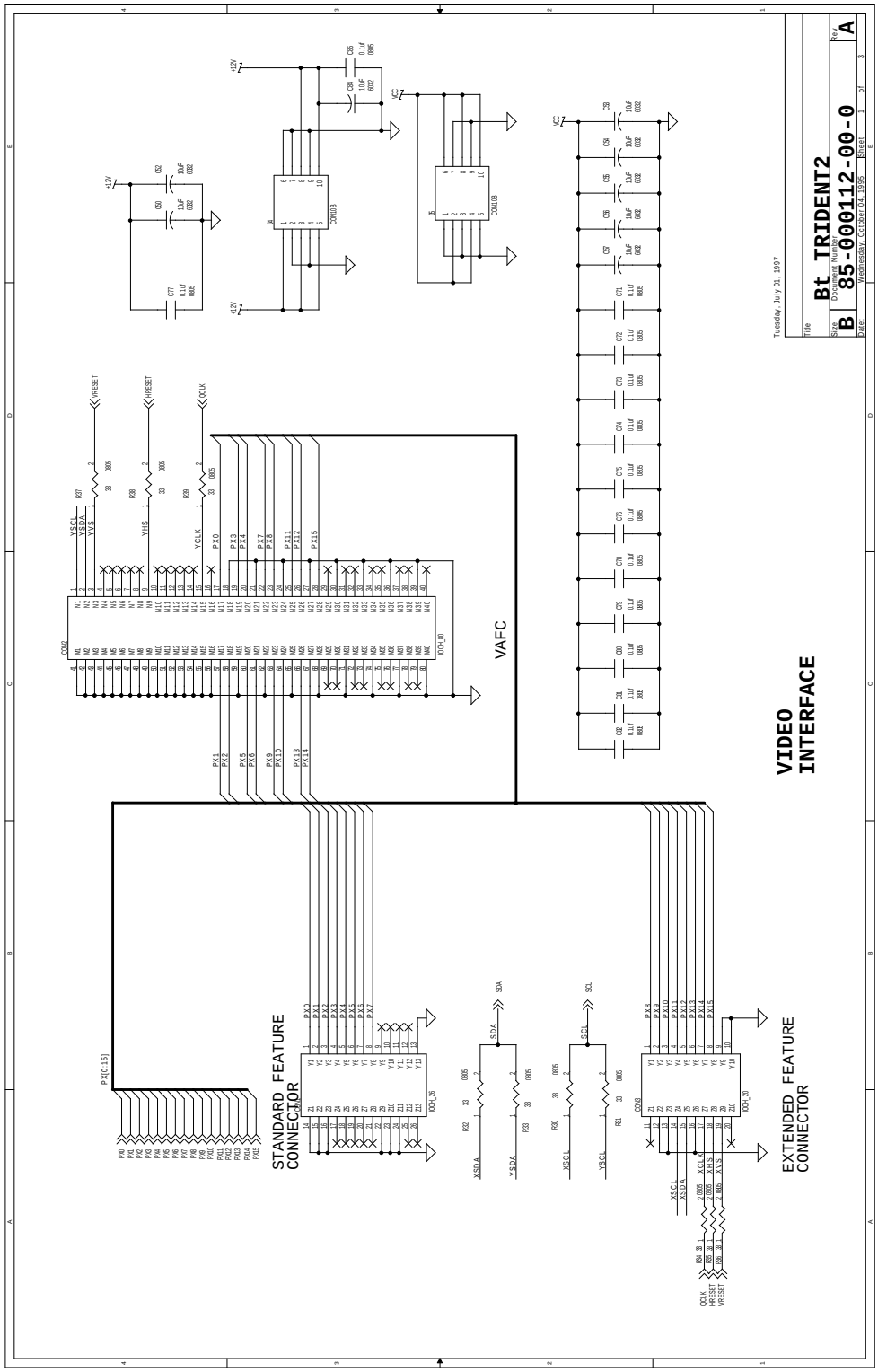


Figure 47b.Bt829/Trident VGA Interface Schematic - Bt829 Detail

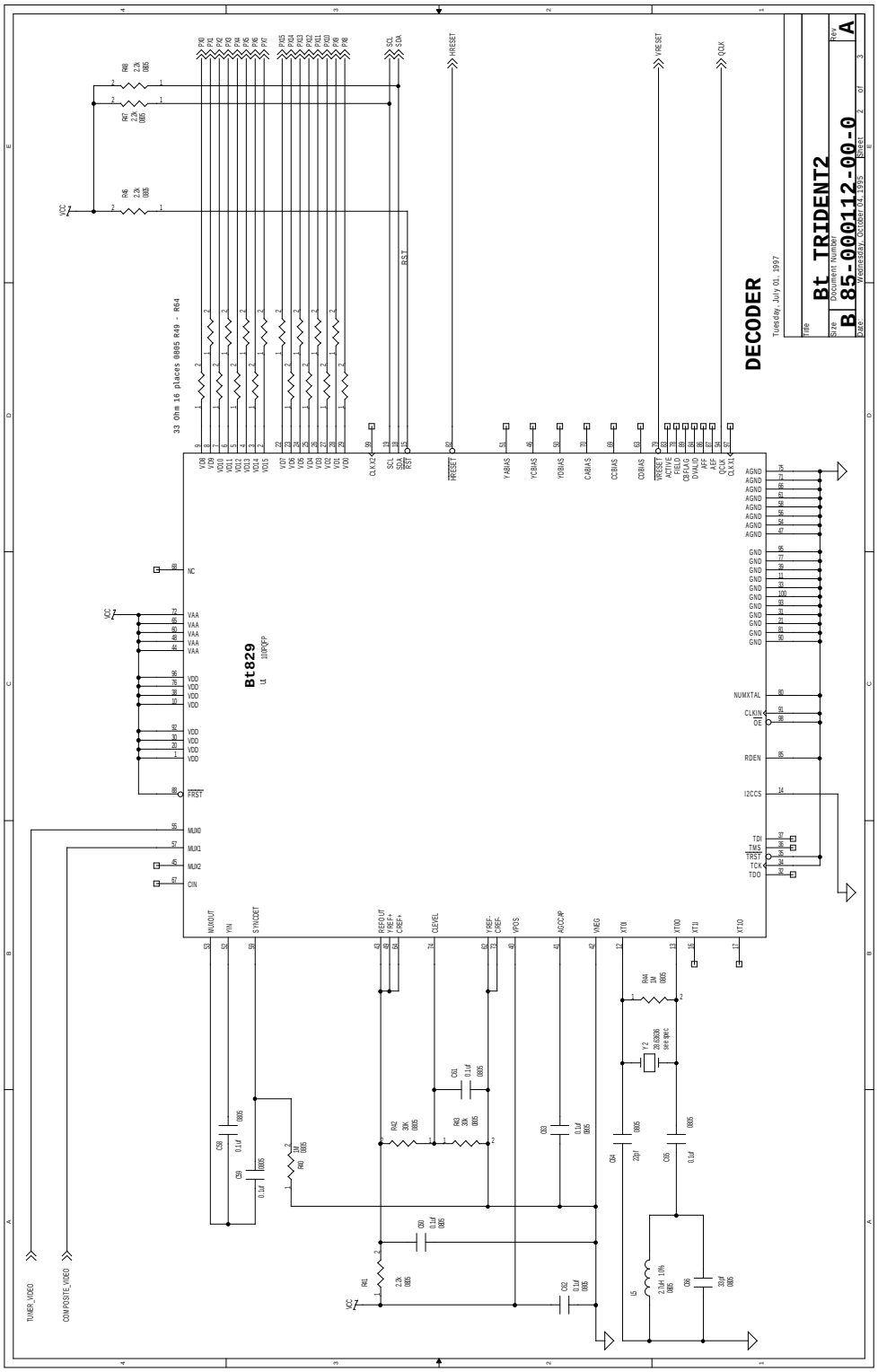
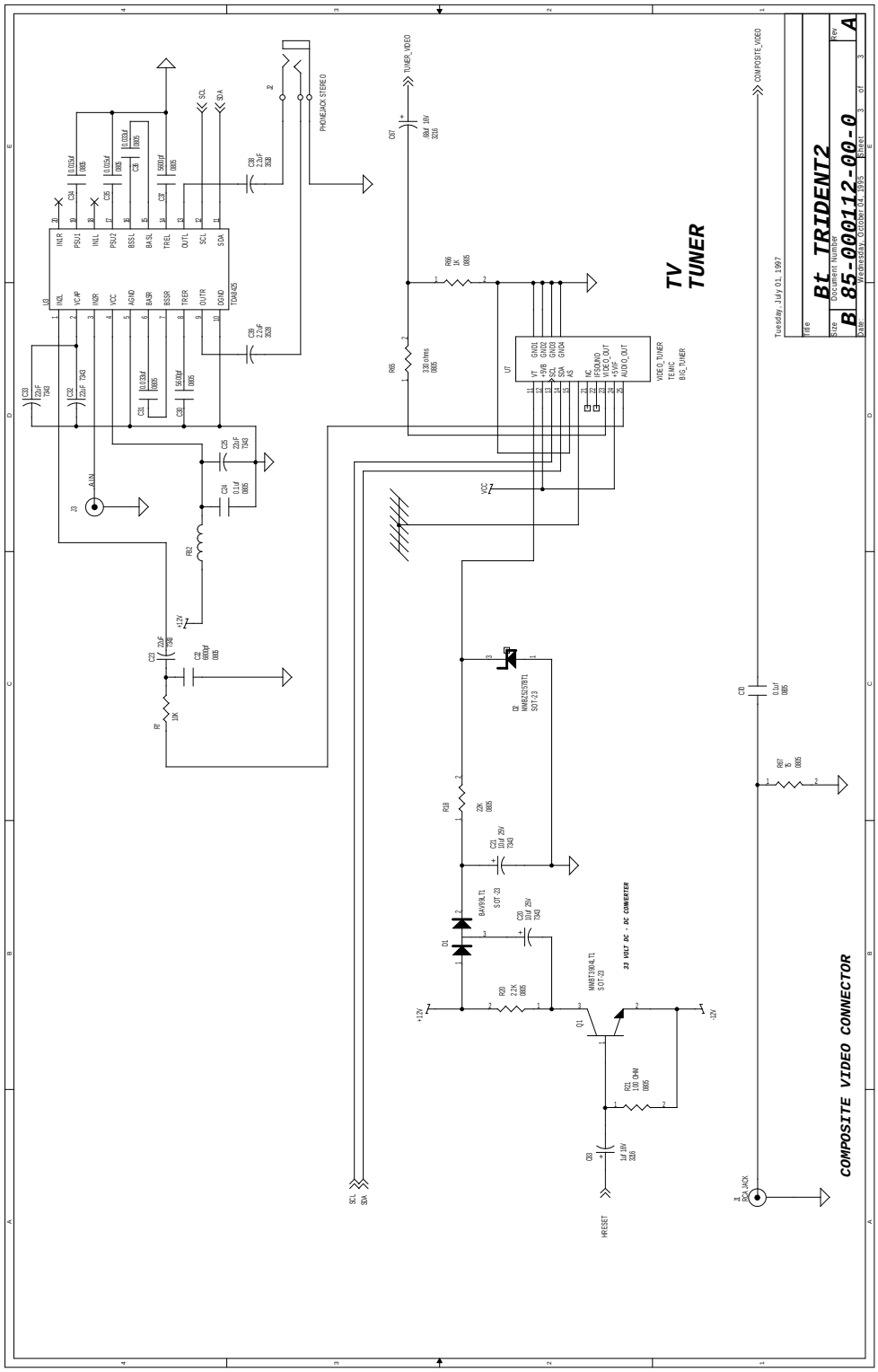
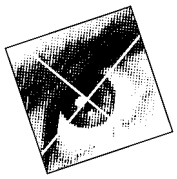


Figure 47c.Bt829/Trident VGA Interface Schematic - Feature Connector Detail





CONTROL REGISTER DEFINITIONS

This section describes the function of the various control registers. Table 13 summarizes of the register functions and follows with details of each register.

Table 13. Register Map *(1 of 2)*

Register Name	Mnemonic	Register Address	640 x 480 Square Pixel NTSC (Default)	768 x 576 Square Pixel PAL/SECAM	720 x 480 CCIR NTSC	720 x 576 CCIR PAL/SECAM	320 x 240 2:1 NTSC (Square Pixel, CIF)	320 x 288 2:1 PAL/SECAM (Square Pixel, CIF)
Device Status	STATUS	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Input Format	IFORM	0x01	0x58	0x78	0x58	0x78	0x58	0x78
Temporal Decimation	TDEC	0x02	0x00	0x00	0x00	0x00	0x00	0x00
MSB Cropping	CROP	0x03	0x12	0x23	0x12	0x23	0x11	0x21
Vertical Delay, Lower Byte	VDELAY_LO	0x04	0x16	0x16	0x16	0x16	0x16	0x16
Vertical Active, Lower Byte	VACTIVE_LO	0x05	0xE0	0x40	0xE0	0x40	0xE0	0x40
Horizontal Delay, Lower Byte	HDELAY_LO	0x06	0x78	0x9A	0x80	0x90	0x40	0x48
Horizontal Active, Lower Byte	HACTIVE_LO	0x07	0x80	0x00	0xD0	0xD0	0x40	0x80
Horizontal Scaling, Upper Byte	HSCALE_HI	0x08	0x02	0x03	0x00	0x05	0x11	0x1A
Horizontal Scaling, Lower Byte	HSCALE_LO	0x09	0xAC	0x3C	0xF8	0x04	0xF0	0x09
Brightness Control	BRIGHT	0x0A	0x00	0x00	0x00	0x00	0x00	0x00
Miscellaneous Control	CONTROL	0x0B	0x20	0x20*(1)*	0x20	0x20*(1)*	0x20	0x20
Luma Gain, Lower Byte (Contrast)	CONTRAST_LO	0x0C	0xD8	0xD8	0xD8	0xD8	0xD8	0xD8
Chroma (U) Gain, Lower Byte (Saturation)	SAT_U_LO	0x0D	0xFE	0xFE	0xFE	0xFE	0xFE	0xFE
Chroma (V) Gain, Upper Byte (Saturation)	SAT_V_LO	0x0E	0xB4	0xB4	0xB4	0xB4	0xB4	0xB4
Hue Control	HUE	0x0F	0x00	0x00	0x00	0x00	0x00	0x00
SC Loop Control	SCLOOP	0x10	0x00	0x00*(1)*	0x00	0x00*(1)*	0x00	0x00

Table 13. Register Map *(2 of 2)*

Register Name	Mnemonic	Register Address	640 x 480 Square Pixel NTSC (Default)	768 x 576 Square Pixel PAL/SECAM	720 x 480 CCIR NTSC	720 x 576 CCIR PAL/SECAM	320 x 240 2:1 NTSC (Square Pixel, CIF)	320 x 288 2:1 PAL/SECAM (Square Pixel, CIF)
White Crush Up Count	WC_UP	0x11	0xCF	0xCF	0xCF	0xCF	0xCF	0xCF
Output Format	OFORM	0x12	0x06	0x06	0x06	0x06	0x06	0x06
Vertical Scaling, Upper Byte	VSCALE_HI	0x13	0x60	0x60	0x60	0x60	0x40(2)	0x40(2)
Vertical Scaling, Lower Byte	VSCALE_LO	0x14	0x00	0x00	0x00	0x00	0x00	0x00
Test Control	TEST	0x15	0x01	0x01	0x01	0x01	0x01	0x01
Video Timing Polarity Register	VPOLE	0x16	0x00	0x00	0x00	0x00	0x00	0x00
ID Code	IDCODE	0x17	0x70	0x70	0x70	0x70	0x70	0x70
AGC Delay	ADELAY	0x18	0x68	0x7F	0x68	0x7F	0x68	0x7F
Burst Gate Delay	BDELAY	0x19	0x5D	0x72(1)	0x5D	0x72(1)	0x5D	0x72
ADC Interface	ADC	0x1A	0x82	0x82	0x82	0x82	0x82	0x82
Video Timing Control	VTC	0x1B	0x00	0x00	0x00	0x00	0x00	0x00
Extended Data Services/Closed Caption Status	CC_STATUS	0x1C	0x00	0x00	0x00	0x00	0x00	0x00
Extended Data Services/Closed Caption Data	CC_DATA	0x1D	0x00	0x00	0x00	0x00	0x00	0x00
White Crush Down Count	WC_DN	0x1E	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
Software Reset	SRESET	0x1F	—	—	—	—	—	—
Programmable I/O	P_IO	0x3F	—	—	—	—	—	—
SECAM Video Register Differences								
Miscellaneous Control	CONTROL	—	—	0x00	—	0x00	—	—
SC Loop Control	SCLOOP	—	—	0x10	—	0x10	—	—
Burst Gate Delay	BDELAY	—	—	0xA0	—	0xA0	—	—

Notes: (1). SECAM Video Register differences to PAL video.
(2). When using one field, no additional vertical scaling is necessary for CIF resolutions. The INT bit in register 0xB(VSCALE_HI) should be set to a logical zero when scaling from only one field.

0x00 — Device Status Register (STATUS)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. COF is the least significant bit. The COF and LOF status bits hold their values until reset to their default values by writing to them. The other six bits do not hold their values, but continually output the status. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
PRES	HLOC	FIELD	NUML	CSEL	CCVALID	LOF	COF
0	0	0	0	0	0	0	0

PRES Video Present Status. Video is determined as not present when an input sync is not detected in 31 consecutive line periods.

0* = Video not present
1 = Video present

HLOC Device in H-lock. If HSYNC is found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 1. Once set, if HSYNC is not found within ±1 clock cycle of the expected position of HSYNC for 32 consecutive lines, this bit is set to a logical 0. MPU writes to this bit are ignored. This bit indicates the stability of the incoming video. While it is an indicator of horizontal locking, some video sources will characteristically vary from line to line by more than one clock cycle so that this bit will never be set. Consumer VCRs are examples of sources that will tend to never set this bit.

0* = Device not in H-lock
1 = Device in H-lock

FIELD Field Status. This bit reflects whether an odd or even field is being decoded. The FIELD bit is determined by the relationship between $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$.

0* = Odd field
1 = Even field

NUML Number of Lines. This bit identifies the number of lines found in the video stream. This bit is used to determine the type of video input to the Bt829A. Thirty-two consecutive fields with the same number of lines is required before this status bit will change.

0* = 525 line format (NTSC/PAL-M)
1 = 625 line format (PAL/SECAM)

CSEL Crystal Select. This bit identifies which crystal port is selected. When automatic format detection is enabled, this bit will be the same as NUML.

0* = XTAL0 input selected
1 = XTAL1 input selected

CCVALID Valid Closed Caption Data. This bit indicates that valid closed caption or extended data services (EDS) sample pairs have been stored in the closed caption data registers. This bit indicates that the closed caption data FIFO is half full. It is reset after being written into or a chip reset occurs.

LOF Luma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs. The state of this bit is not valid and should be ignored when the ADC is in power-down mode (Y_SLEEP = 1). When the luma A/D is in sleep mode, LOF is set to 1.

COF Chroma ADC Overflow. On power-up, this bit is set to 0. If an ADC overflow occurs, the bit is set to a logical 1. It is reset after being written to or a chip reset occurs. The state of this bit is not valid and should be ignored when the ADC is in power-down mode (C_SLEEP = 1). When the chroma A/D is in sleep mode, COF is set to 1.

0x01 — Input Format Register (IFORM)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x58. FORMAT(0) is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
HACTIVE	MUXSEL		XTSEL		FORMAT		
0	1	0	1	1	0	0	0

HACTIVE When using the Bt829A with a packed memory architecture, for example, with field memories, this bit should be programmed with a logical 1. When implementing a VRAM based architecture, program with a logical 0.

0* = Reset HACTIVE with HRESET
1 = Extend HACTIVE beyond HRESET

MUXSEL Used for software control of video input selection. The Bt829A can select between four composite video sources, or three composite and one S-Video source.

00 = Select MUX3 input to MUXOUT
01 = Select MUX2 input to MUXOUT
10* = Select MUX0 input to MUXOUT
11 = Select MUX1 input to MUXOUT

XTSEL If automatic format detection is required, logical 11 must be loaded. Logical 01 and 10 are used if software format selection is desired.

00 = Reserved
01 = Select XT0 input (only XT0 present)
10 = Select XT1 input (both XTs present)
11* = Auto XT select enabled (both XTs present)

FORMAT Automatic format detection may be enabled or disabled. The NUML bit is used to determine the input format when automatic format detection is enabled.

000*= Auto format detect enabled
001 = NTSC (M) input format
010 = NTSC with no pedestal format
011 = PAL (B, D, G, H, I) input format
100 = PAL (M) input format
101 = PAL (N) input format
110 = SECAM input format
111 = PAL (Ncombination) input format

0x02 — Temporal Decimation Register (TDEC)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. DEC_RAT(0) is the least significant bit. This register enables temporal decimation by discarding a finite number of fields or frames from the incoming video. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
DEC_FIELD	FLDALIGN	DEC_RAT					
0	0	0	0	0	0	0	0

DEC_FIELD Defines whether decimation is by fields or frames.

0* = Decimate frames
1 = Decimate fields

FLDALIGN This bit aligns the start of decimation with an even or odd field.

0* = Start decimation on the odd field (an odd field is the first field dropped).
1 = Start decimation on the even field (an even field is the first field dropped).

DEC_RAT DEC_RAT is the number of fields or frames dropped out of 60 NTSC or 50 PAL/SECAM fields or frames. 0x00 value disables decimation (all video frames and fields are output).

NOTE: Use caution when changing the programming in the TDEC register. 0x00 must be loaded before the decimation value. This will ensure decimation does not start on the wrong field or frame. The register should not be loaded with greater than 60 (0x3C) for NTSC, or 50 (0x34) for PAL/SECAM.

xx00 0000–xx11 1111 = Number of fields/frames dropped.

0x03 — MSB Cropping Register (CROP)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x12. HACTIVE_MSB(0) is the least significant bit. See the VACTIVE, VDELAY, HACTIVE and HDELAY registers for descriptions on the operation of this register.

7	6	5	4	3	2	1	0
VDELAY_MSB		VACTIVE_MSB		HDELAY_MSB		HACTIVE_MSB	
0	0	0	1	0	0	1	0

VDELAY_MSB 00xx xxxx–11xx xxxx = The most significant two bits of vertical delay register.

VACTIVE_MSB xx00 xxxx–xx11 xxxx = The most significant two bits of vertical active register.

HDELAY_MSB xxxx 00xx–xxxx 11xx = The most significant two bits of horizontal delay register .

HACTIVE_MSB xxxx xx00–xxxx xx11 = The most significant two bits of horizontal active register.

0x04 — Vertical Delay Register, Lower Byte (VDELAY_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x16. VDELAY_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit VDELAY register. The two MSBs of VDELAY are contained in the CROP register. VDELAY defines the number of half lines between the trailing edge of VRESET and the start of active video.

7	6	5	4	3	2	1	0
VDELAY_LO							
0	0	0	1	0	1	1	0

VDELAY_LO 0x01–0xFF = The least significant byte of the vertical delay register.

0x05 — Vertical Active Register, Lower Byte (VACTIVE_LO)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0xE0. VACTIVE_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit VACTIVE register. The two MSBs of VACTIVE are contained in the CROP register. VACTIVE defines the number of lines used in the vertical scaling process. The actual number of lines output by the Bt829A is SCALING_RATIO * VACTIVE.

7	6	5	4	3	2	1	0
VACTIVE_LO							
1	1	1	0	0	0	0	0

VACTIVE_LO 0x00–0xFF = The least significant byte of the vertical active register.

0x06 — Horizontal Delay Register, Lower Byte (HDELAY_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x78. HDELAY_LO(0) is the least significant bit. This 8-bit register is the lower byte of the 10-bit HDELAY register. The two MSBs of HDELAY are contained in the CROP register. HDELAY defines the number of scaled pixels between the falling edge of HRESET and the start of active video.

7	6	5	4	3	2	1	0
HDELAY_LO							
0	1	1	1	1	0	0	0

HDELAY_LO 0x01–0xFF = The least significant byte of the horizontal delay register. HACTIVE pixels will be output by the chip starting at the fall of HRESET.

Caution: HDELAY must be programmed with an even number.

0x07 — Horizontal Active Register, Lower Byte (HACTIVE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x80. HACTIVE_LO(0) is the least significant bit. HACTIVE defines the number of horizontal active pixels per line output by the Bt829A.

7	6	5	4	3	2	1	0
HACTIVE_LO							
1	0	0	0	0	0	0	0

HACTIVE_LO 0x00–0xFF = The least significant byte of the horizontal active register. This 8-bit register is the lower byte of the 10-bit HACTIVE register. The two MSBs of HACTIVE are contained in the CROP register.

0x08 — Horizontal Scaling Register, Upper Byte (HSCALE_HI)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x02. This 8-bit register is the upper byte of the 16-bit HSCALE register.

7	6	5	4	3	2	1	0
HSCALE_HI							
0	0	0	0	0	0	1	0

HSCALE_HI 0x00–0xFF = The most significant byte of the horizontal scaling ratio.

0x09 — Horizontal Scaling Register, Lower Byte (HSCALE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xAC. This 8-bit register is the lower byte of the 16-bit HSCALE register.

7	6	5	4	3	2	1	0
HSCALE_LO							
1	0	1	0	1	1	0	0

HSCALE_LO 0x00–0xFF = The least significant byte of the horizontal scaling ratio.

0x0A — Brightness Control Register (BRIGHT)

The brightness control involves the addition of a two's complement number to the luma channel. Brightness can be adjusted in 255 steps, from –128 to +127. The resolution of brightness change is one LSB (0.39% with respect to the full luma range). An asterisk indicates the default option.

7	6	5	4	3	2	1	0
BRIGHT							
0	0	0	0	0	0	0	0

BRIGHT

Hex Value	Binary Value	Brightness Changed By	
		Number of LSBs	Percent of Full Scale
0x80	1000 0000	–128	–100%
0x81	1000 0001	–127	–99.22%
. .	. .	. .	
0xFF	1111 1111	–01	–0.78%
0x00*	0000 0000*	00	0%
0x01	0000 0001	+01	+0.78%
. .	. .	. .	
0x7E	0111 1110	+126	+99.2%
0x7F	0111 1111	+127	+100%

0x0B — Miscellaneous Control Register (CONTROL)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0x20. SAT_V_MSB is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
LNOTCH	COMP	LDEC	CBSENSE	Reserved	CON_MSB	SAT_U_MSB	SAT_V_MSB
0	0	1	0	0	0	0	0

LNOTCH This bit is used to include the luma notch filter. For monochrome video, the notch should not be used. This will output full bandwidth luminance.

0* = Enable the luma notch filter
1 = Disable the luma notch filter

COMP When COMP is set to logical one, the luma notch is disabled. When COMP is set to logical zero, the C ADC is disabled.

0* = Composite Video
1 = Y/C Component Video

LDEC The luma decimation filter is used to reduce the high-frequency component of the luma signal. Useful when scaling to CIF resolutions or lower.

0 = Enable luma decimation using selectable H filter
1* = Disable luma decimation

CBSENSE This bit controls whether the first pixel of a line is a Cb pixel or a Cr pixel. For example, if CBSENSE is low and HDELAY is an even number, the first active pixel output is a Cb pixel. If HDELAY is odd, CBSENSE may be programmed high to produce a Cb pixel as the first active pixel output.

0* = Normal Cb, Cr order
1 = Invert Cb, Cr order

Reserved This bit should only be written with a logical zero.

CON_MSB The most significant bit of the luma gain (contrast) value.

SAT_U_MSB The most significant bit of the chroma (u) gain value.

SAT_V_MSB The most significant bit of the chroma (v) gain value.

0x0C — Luma Gain Register, Lower Byte (CONTRAST_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xD8. CONTRAST_LO(0) is the least significant bit. The CON_L_MSB bit and the CONTRAST_LO register concatenate to form the 9-bit CONTRAST register. The value in this register is multiplied by the luminance value to provide contrast adjustment.

7	6	5	4	3	2	1	0
CONTRAST_LO							
1	1	0	1	1	0	0	0

CONTRAST_LO The least significant byte of the luma gain (contrast) value.

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	236.57%
510	0x1FE	236.13%
. .	. .	. .
217	0x0D9	100.46%
216	0x0D8	100.00%
. .	. .	. .
128	0x080	59.26%
. .	. .	. .
1	0x001	0.46%
0	0x000	0.00%

0x0D — Chroma (U) Gain Register, Lower Byte (SAT_U_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xFE. SAT_U_LO(0) is the least significant bit. SAT_U_MSB in the CONTROL register, and SAT_U_LO concatenate to give a 9-bit register (SAT_U). This register is used to add a gain adjustment to the U component of the video signal. By adjusting the U and V color components of the video stream by the same amount, the saturation is adjusted. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_U_MSB bit is altered, care must be taken to ensure that the other bits in the CONTROL register are not affected.

7	6	5	4	3	2	1	0
SAT_U_LO							
1	1	1	1	1	1	1	0

SAT_U_LO

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	201.18%
510	0x1FE	200.79%
. .	. .	. .
255	0x0FF	100.39%
254	0x0FE	100.00%
. .	. .	. .
128	0x080	50.39%
. .	. .	. .
1	0x001	0.39%
0	0x000	0.00%

0x0E — Chroma (V) Gain Register, Lower Byte (SAT_V_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0xB4. SAT_V_LO(0) is the least significant bit. SAT_V_MSB in the CONTROL register and SAT_V_LO concatenate to give a 9-bit register (SAT_V). This register is used to add a gain adjustment to the V component of the video signal. By adjusting the U and V color components of the video stream by the same amount, the saturation is adjusted. For normal saturation adjustment, the gain in both the color difference paths must be the same (i.e. the ratio between the value in the U gain register and the value in the V gain register should be kept constant at the default power-up ratio). When changing the saturation, if the SAT_V_MSB bit is altered, care must be taken to ensure that the other bits in the CONTROL register are not affected.

7	6	5	4	3	2	1	0
SAT_V_LO							
1	0	1	1	0	1	0	0

SAT_V_LO

Decimal Value	Hex Value	% of Original Signal
511	0x1FF	283.89%
510	0x1FE	283.33%
. .	. .	. .
181	0x0B5	100.56%
180	0x0B4	100.00%
. .	. .	. .
128	0x080	71.11%
. .	. .	. .
1	0x001	0.56%
0	0x000	0.00%

0x0F — Hue Control Register (HUE)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. HUE(0) is the least significant bit. Hue adjustment involves the addition of a two's complement number to the demodulating subcarrier phase. Hue can be adjusted in 256 steps in the range –90˚ to +89.3˚, in increments of 0.7˚. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
HUE							
0	0	0	0	0	0	0	0

HUE

Hex Value	Binary Value	Subcarrier Reference Changed By	Resulting Hue Changed By
0x80	1000 0000	–90˚	+90˚
0x81	1000 0001	–89.3˚	+89.3˚
. .	. .	. .	. .
0xFF	1111 1111	–0.7˚	+0.7˚
0x00*	0000 0000	00˚	00˚
0x01	0000 0001	+0.7˚	–0.7˚
. .	. .	. .	. .
0x7E	0111 1110	+88.6˚	–88.6˚
0x7F	0111 1111	+89.3˚	–89.3˚

0x10 — SC Loop Control (SCLOOP)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00. ACCEL is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
PEAK	CAGC	CKILL	HFILT		Reserved		
0	0	0	0	0	0	0	0

PEAK This bit determines if the normal luma low pass filters are implemented via the HFILT bits or if the peaking filters are implemented. The LDEC bit in the control register must be programmed to zero to use these filters.

0* = Normal luma low pass filtering
1 = Use luma peaking filters

CAGC This bit controls the Chroma AGC function. When enabled, Chroma AGC will compensate for non-standard chroma levels. The compensation is achieved by multiplying the incoming chroma signal by a value in the range of 0.5 to 2.0.

0* = Chroma AGC Disabled
1 = Chroma AGC Enabled

CKILL This bit determines whether the low color detector and removal circuitry is enabled.

0* = Low Color Detection and Removal Disabled
1 = Low Color Detection and Removal Enabled

HFILT These bits control the configuration of the optional 6-tap Horizontal Low-Pass Filter. The auto-format mode determines the appropriate low-pass filter based on the horizontal scaling ratio selected. The LDEC bit in the CONTROL register must be programmed to zero to use these filters.

00* = Auto Format. If auto format is selected when horizontally scaling between full resolution and half resolution, no filtering is selected. When scaling between one-half and one-third resolution, the CIF filter is used. When scaling between one-third and one-seventh resolution, the QCIF filter is used, and at less than one-seventh resolution, the ICON filter is used.
01 = CIF
10 = QCIF (When decoding SECAM video this filter must be enabled)
11 = ICON

If the PEAK bit is set to logical one, the HFILT bits determine which peaking filter is selected.

00 = Maximum peaking response
01 = Medium peaking response
10 = Low peaking response
11 = Minimum peaking response

Reserved These bits must be set to zero.

0x11 — White Crush Up Count Register (WC_UP)

This control register may be written to or read by the MPU at any time, and upon reset it is initialized to 0xCF. UPCNT(0) is the least significant bit.

7	6	5	4	3	2	1	0
MAJS		UPCNT					
1	1	0	0	1	1	1	1

MAJS These bits determine the majority comparison point for the White Crush Up function.

00 = 3/4 of maximum luma value
01 = 1/2 of maximum luma value
10 = 1/4 of maximum luma value
11* = Automatic

UPCNT The value programmed in these bits accumulates once per field or frame, in the case where the majority of the pixels in the active region of the image are below a selected value. The accumulated value determines the extent to which the AGC value needs to be raised in order to keep the SYNC level proportionate with the white level. The UPCNT value is assumed positive, i.e.,

3F = 63
3E = 62
: : :
. . .
00 = 0

0x12 — Output Format Register (OFORM)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x06. OES(0) is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
RANGE	CORE		VBI_FRAME	CODE	LEN	OES	
0	0	0	0	0	1	1	0

RANGE Luma Output Range: This bit determines the range for the luminance output on the Bt829A. The range must be limited when using the control codes as video timing.

0* = Normal operation (Luma range 16–253, chroma range 2–253).
Y=16 is black (pedestal)
Cr, Cb=128 is zero color information

1 = Full-range Output (Luma range 0–255, chroma range 2–253)
Y=0 is black (pedestal)
Cr, Cb=128 is zero color information

CORE Luma Coring: These bits control the coring value used by the Bt829A. When coring is active and the total luminance level is below the limit programmed into these bits, the luminance signal is truncated to zero.

00* = 0x00 no coring
01 = 8
10 = 16
11 = 32

VBI_FRAME This bit enables the VBI Frame output mode. In the VBI Frame output mode, every line consists of unfiltered 8*Fsc non-image data. This bit supersedes bit VBIEN in the VTC register. VBIFMT (also in VTC) works in both VBI Frame and Line output modes.

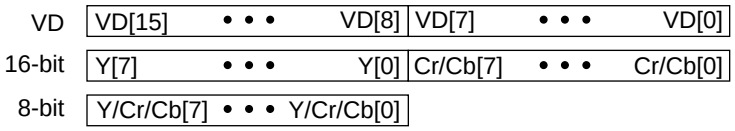
0* = VBI Frame output mode disabled
1 = VBI Frame output mode enabled

CODE Code Control Disable: This bit determines if control codes are output with the video data. SPI Mode 2 requires this bit to be programmed with a logical 1. When control codes are inserted into the data stream, the external control signals are still available.

0* = Disable control code insertion
1 = Enable control code insertion

LEN 8- or 16-Bit Format: This bit determines the output data format. In 8-bit mode, the data is output on VD[15:8].

0 = 8-bit YCrCb 4:2:2 output stream
1* = 16-Bit YCrCb 4:2:2 output stream



OES OES[1] and OES[0] control the output three-states when the $\overline{OE}$ pin or the OUTEN bit (VPOLE bit 7) is asserted. The pins are divided into three groups: timing ($\overline{HRESET}$, $\overline{VRESET}$, ACTIVE, VACTIVE, CBFLAG, DVALID and FIELD), clocks (CLKx1, CLKx2 and QCLK) and data (VD[15:0]). CCVALID cannot output three-states.

00 = Three-state timing and data only
01 = Three-state data only
10 = Three-state timing, data and clocks
11 = Three-state clocks and data only

0x13 — Vertical Scaling Register, Upper Byte (VSCALE_HI)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x60. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
YCOMB	COMB	INT	VSCALE_HI				
0	1	1	0	0	0	0	0

YCOMB Luma Comb Enable: When enabled, the luma comb filter performs a weighted average on 2, 3, 4, or 5 lines of luminance data. The coefficients used for the average are fixed and no interpolation is performed. The number of lines used for the luma comb filter is determined by the VFILT bits in the VTC register. When disabled by a logical zero, filtering and full vertical interpolation is performed based upon the value programmed into the VSCALE register. The LUMA comb filter cannot be enabled on the Bt827A.

0* = Vertical low-pass filtering and vertical interpolation
1 = Vertical low-pass filtering only

COMB Chroma Comb Enable: This bit determines if the chroma comb is included in the data path. If enabled, a full line store is used to average adjacent lines of color information, reducing cross-color artifacts.

0 = Chroma comb disabled
1* = Chroma comb enabled

INT Interlace: This bit is programmed to indicate if the incoming video is interlaced or non-interlaced. For example, if using the full frame as input for vertical scaling, this bit should be programmed high. If using a single field for vertical scaling, this bit should be programmed low. Single field scaling is normally used when scaling below CIF resolution and outputting to a non-interlaced monitor. Using a single field will reduce motion artifacts.

0 = Non-interlace VS
1* = Interlace VS

VSCALE_HI Vertical Scaling Ratio: These five bits represent the most significant portion of the 13-bit vertical scaling ratio register. The system must take care not to alter the contents of the LINE, COMB and INT bits while adjusting the scaling ratio.

0x14 — Vertical Scaling Register, Lower Byte (VSCALE_LO)

This control register may be written to or read by the MPU at any time. Upon reset it is initialized to 0x00.

7	6	5	4	3	2	1	0
VSCALE_LO							
0	0	0	0	0	0	0	0

VSCALE_LO Vertical Scaling Ratio: These eight bits represent the least significant byte of the 13-bit vertical scaling ratio register. They are concatenated with five bits in VSCALE_HI. The following equation should be used to determine the value for this register:

$$VSCALE = (0x10000 - \{ [(scaling\_ratio) - 1] * 512 \}) \& 0x1FFF$$

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of vertical lines is 156:

$$VSCALE = (0x10000 - \{ [(4/1) - 1] * 512 \}) \& 0x1FFF$$
$$= 0x1A00$$

0x15 — Test Control Register (TEST)

This control register is reserved for putting the part into test mode. Write operation to this register may cause undetermined behavior and should not be attempted. A read cycle from this register returns 0x01, and only a write of 0x01 is permitted.

0x16 — Video Timing Polarity Register (VPOLE)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x00. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
OUT_EN	DVALID	VACTIVE	CBFLAG	FIELD	ACTIVE	HRESET	VRESET
0	0	0	0	0	0	0	0

OUTEN Three-states the pins defined by OES in the OFORM register. The affected pins are: VD[15:0], $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$, ACTIVE, VACTIVE, DVALID, CBFLAG, FIELD, QCLK, CLKx1, and CLKx2.

When Pin 85 is a logical zero

0* = Enable outputs
1 = Three-state outputs

When Pin 85 is a logical one

0* = Three-state outputs
1 = Enable outputs

DVALID
0* = DVALID Pin: Active high
1 = DVALID Pin: Active low

VACTIVE
0* = VACTIVE Pin: Active high
1 = VACTIVE Pin: Active low

CBFLAG
0* = CBFLAG Pin: Active high
1 = CBFLAG Pin: Active low

FIELD
0* = FIELD Pin: High indicates odd field
1 = FIELD Pin: High indicates even field

ACTIVE
0* = ACTIVE Pin: Active high
1 = ACTIVE Pin: Active low

HRESET
0* = $\overline{\text{HRESET}}$ Pin: Active low
1 = $\overline{\text{HRESET}}$ Pin: Active high

VRESET
0* = $\overline{\text{VRESET}}$ Pin: Active low
1 = $\overline{\text{VRESET}}$ Pin: Active high

0x17 — ID Code Register (IDCODE)

This control register may be read by the MPU at any time. PART_REV(0) is the least significant bit.

7	6	5	4	3	2	1	0
PART_ID				PART_REV			
1	1	1	0	0	0	0	0

PART_ID 1110= Bt829A Part ID Code
1100= Bt827A Part ID Code

PART_REV 0x0 – 0xF = Current Revision ID Code

0x18 — AGC Delay Register (ADELAY)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x68.

7	6	5	4	3	2	1	0
ADELAY							
0	1	1	0	1	0	0	0

ADELAY AGC gate delay for back-porch sampling. The following equation should be used to determine the value for this register:

$$ADELAY = (6.8\ \mu S * f_{CLKx1}) + 7$$

For example, for an NTSC input signal:

$$ADELAY = (6.8\ \mu S * 14.32\ MHz) + 7$$
$$= 104\ (0x68)$$

0x19 — Burst Delay Register (BDELAY)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x5D. BDELAY(0) is the least significant bit.

7	6	5	4	3	2	1	0
BDELAY							
0	1	0	1	1	1	0	1

BDELAY The burst gate delay for sub-carrier sampling. The following equation should be used to determine the value for this register:

$$BDELAY = (6.5\ \mu S * f_{CLKx1})$$

For example, for an NTSC input signal:

$$BDELAY = (6.5\ \mu S * 14.32\ MHz)$$
$$= 93\ (0x5D)$$

0x1A — ADC Interface Register (ADC)

This control register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x82. Reserved is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
Reserved		SYNC_T	AGC_EN	CLK_SLEEP	Y_SLEEP	C_SLEEP	CRUSH
1	0	0	0	0	0	1	0

Reserved These bits should only be written with bit 7 a logical one and bit 6 a logical zero.

SYNC_T This bit defines the voltage level below which the SYNC signal can be detected.

0* = Analog SYNCDET threshold high (~125 mV)
1 = Analog SYNCDET threshold low (~75 mV)

AGC_EN This bit controls the AGC function. If disabled, REFOUT is not driven and an external reference voltage must be provided. If enabled, REFOUT is driven to control the A/D reference voltage.

0* = AGC Enabled
1 = AGC Disabled

CLK_SLEEP When this bit is at a logical one, the system clock is powered down, but the output clocks (CLKx1 and CLKx2) are still running, and the I^2C registers are still accessible. Recovery time is approximately one second.

0* = Normal Clock Operation
1 = Shut down the System Clock (Power Down)

Y_SLEEP This bit enables putting the luma ADC in sleep mode.

0* = Normal Y ADC operation
1 = Sleep Y ADC operation

C_SLEEP This bit enables putting the chroma ADC in sleep mode.

0 = Normal C ADC operation
1* = Sleep C ADC operation

CRUSH This bit enables white crush mode, and must be written with a logical zero.

0* = Normal SYNC level to white level
1 = Enable white CRUSH mode to compensate for nonstandard SYNC to white video relationship

0x1B — Video Timing Control (VTC)

This register may be written to or read by the MPU at any time. Upon reset, it is initialized to 0x00. VFILT(0) is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
HSFMT	ACTFMT	CLKGATE	VBIEN	VBIFMT	VALIDFMT	VFILT	
0	0	0	0	0	0	0	0

HSFMT This bit selects between a single-pixel-wide HRESET and the standard 64-clock-wide HRESET.

0* = $\overline{\text{HRESET}}$ is 64 CLKx1 cycles wide
1 = $\overline{\text{HRESET}}$ is 1 pixel wide

ACTFMT This bit selects whether composite ACTIVE (HACTIVE and VACTIVE) or HACTIVE only is output on the ACTIVE pin.

0* = ACTIVE is composite active
1 = ACTIVE is horizontal active

CLKGATE This bit selects the signals that are gated with CLK to create QCLK. If logical zero is selected, the ACTIVE pin (composite ACTIVE or HACTIVE) is used in gating CLK.

0* = CLKx1 and CLKx2 are gated with DVALID and ACTIVE to create QCLK.
1 = CLKx1 and CLKx2 are gated with DVALID to create QCLK.

VBIEN This bit enables VBI data to be captured.

0* = Do not capture VBI
1 = Capture VBI

VBIFMT This bit determines the byte ordering for VBI data.

0* = Pixel N on the VD[15:8] data bus, pixel N+1 on the VD[7:0] data bus.
1 = Pixel N+1 on the VD[15:8] data bus, Pixel N on the VD[7:0] data bus (Pixel N refers to the 1st, 3rd, 5th..., while pixel N+1 refers to the 2nd, 4th, 6th in a horizontal line of video.)

VALIDFMT

0* = Normal DVALID timing

1 = DVALID is the logical AND of VALID and ACTIVE, where ACTIVE is controlled by the ACTFMT bit. Also, the QCLK signal will free turn and is an inverted version of CLKx1 or CLKx2, depending upon whether 8- or 16-bit pixel output format is selected.

VFILT These bits control the number of taps in the Vertical Scaling Filter. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure the needed data does not overflow the internal FIFO.

If the YCOMB bit in the VSCALE_HI register is a logical one, the following settings and equations apply:

00* = 2-tap $\frac{1}{2}(1 + Z^{-1})$ Available at all resolutions.

01 = 3-tap $\frac{1}{4}(1 + 2Z^{-1} + Z^{-2})$ Only available if scaling to less than 385 horizontal active pixels for PAL or 361 for NTSC (CIF or smaller).

10 = 4-tap $\frac{1}{8}(1 + 3Z^{-1} + 3Z^{-2} + Z^{-3})$ Only available if scaling to less than 193 horizontal active pixels for PAL or 181 for NTSC (QCIF or smaller)

11 = 5-tap $\frac{1}{16}(1 + 4Z^{-1} + 6Z^{-2} + 4Z^{-3} + Z^{-4})$ Only available if scaling to less than 193 horizontal active pixels for PAL or 181 for NTSC (QCIF or smaller).

If the YCOMB bit in the VSCALE_HI register is a logical zero, the following settings and equations apply:

00* = 2-tap interpolation only. Available at all resolutions.

01 = 2-tap $\frac{1}{2}(1 + Z^{-1})$ and 2-tap interpolation. Only available if scaling to less than 385 horizontal active pixels for PAL or 361 for NTSC (CIF or smaller).

10 = 3-tap $\frac{1}{4}(1 + 2Z^{-1} + Z^{-2})$ and 2-tap interpolation. Only available if scaling to less than 193 horizontal active pixels for PAL or 181 for NTSC (QCIF or smaller).

11 = 4-tap $\frac{1}{8}(1 + 3Z^{-1} + 3Z^{-2} + Z^{-3})$ and 2-tap interpolation. Only available if scaling to less than 193 horizontal active pixels for PAL or 181 for NTSC (QCIF or smaller).

NOTE: The Bt827A can only be used with a VFILT value of 00, as it does not have a vertical scaling filter.

0x1C — Extended Data Service/Closed Caption Status Register (CC_STATUS)

This register may be written or read by the MPU at any time. Upon reset, the value of register bits 7, 1, and 0 are indeterminate because their status depends on the incoming CC/EDS data. Having register bits 6, 5 and 4 at their reset value causes the CC/EDS circuitry to be powered down. $\overline{LO}$_HI is the least significant bit. An asterisk indicates the default option.

7	6	5	4	3	2	1	0
PARITY_ERR	CCVALID_EN	EDS	CC	OR	DA	$\overline{CC}$_EDS	$\overline{LO}$_HI
X	1	0	0	0	0	X	X

PARITY_ERR This bit corresponds to the current word in CC_DATA.

0 = No error
1 = Odd parity error

NOTE: Closed caption data is transmitted using odd parity.

CCVALID_EN This bit serves as a mask for the CCVALID interrupts pin.

0 = Disabled CCVALID interrupts pin
1 = Enabled CCVALID interrupts pin

EDS This bit determines if EDS data is written into the CC_DATA FIFO.

0* = EDS data is not written into the CC_DATA FIFO
1 = EDS data is written into the CC_DATA FIFO

CC This bit determines if CC data is written into the CC_DATA FIFO.

0* = CC data is not written into the CC_DATA FIFO
1 = CC data is written into the CC_DATA FIFO

OR This bit indicates the CC_DATA FIFO is full and EDS or CC data has been lost. This bit is read only. On reset or read of CC_DATA this bid is set to zero.

0 = An overflow has not occurred since this bit was last reset
1 = An overflow has occurred

DA CC/EDS data available. This bit indicates if there is valid data in the CC_DATA FIFO. This bit is read only. On reset, this bit is set to zero.

0 = FIFO is empty
1 = One or more bytes available

$\overline{\text{CC}}$_EDS This bit indicates if a CC byte or an EDS byte is in the CC_DATA register. After the CC_DATA register is read, this bit is automatically updated. This bit is read only. On reset, this bit is not valid.

0 = Closed caption byte in CC_DATA
1 = Extended data service byte in CC_DATA

LO_HI CC/EDS data are output in 16-bit words. This bit indicates whether the low or high byte is in the CC_DATA register. This bit is read only. On reset, this bit is not valid.

0 = Low byte is in the CC_DATA register
1 = High byte is in the CC_DATA register

0x1D — Extended Data Service/Closed Caption Data Register (CC_DATA)

This register is read only. It may be read by the MPU at any time. Writes to this register will be ignored. Upon reset, the value of the bits in this register are indeterminate because their status depends on the incoming CC/EDS data. CC_DATA(0) is the least significant bit.

7	6	5	4	3	2	1	0
CC_DATA							
X	X	X	X	X	X	X	X

CC_DATA The low or high data byte transmitted in a closed caption or extended data service line.

0x1E — White Crush Down Count Register (WC_DN)

This control register may be written to or read by the MPU at any time, and upon reset is initialized to 0x7F. DNCNT(0) is the least significant bit. This register is programmed with a two's compliment number.

7	6	5	4	3	2	1	0
VERTEN	WCFRAME	DNCNT					
0	1	1	1	1	1	1	1

VERTEN
0* = Normal operation
1 = Adds vertical detection algorithm to reject noise causing false vertical syncs.

WCFRAME This bit programs the rate at which the DNCNT and UPCNT values are accumulated.

0 = Once per field
1 = Once per frame

DNCNT The value programmed in these bits accumulates once per field or frame. The accumulated value determines the extent to which the AGC value needs to be lowered in order to keep the SYNC level proportionate to the white level.

The DNCNT value is assumed negative, i.e.,

3F = –1
3E = –2
: : :
. . .
00 = –64

0x1F — Software Reset Register (SRESET)

This command register can be written at any time. Read cycles to this register return an undefined value. A data write cycle to this register resets the device to the default state (indicated in the command register definitions by an asterisk). Writing any data value into this address resets the device.

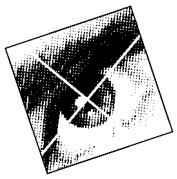
0x3F — Programmable I/O Register (P_IO)

This control register may be written to or read by the MPU at any time, and upon reset is initialized to 0x00. OUT_0 is the least significant bit. While in 8-bit output mode (SPI-8), the VD[7:0] pins are completely asynchronous. IN[3:0] represent the digital levels input on VD[7:4], while the values programmed into OUT[3:0] are output onto VD[3:0]

7	6	5	4	3	2	1	0
IN_3	IN_2	IN_1	IN_0	OUT_3	OUT_2	OUT_1	OUT_0
0	0	0	0	0	0	0	0

IN[3:0] These input bits can be used to monitor external signals from VD[7:4]. The Programmable I/O register is only accessible in the 8-bit 4:2:2 YCrCb output mode (LEN=0). If not in the 8-bit output mode, the values returned by the IN[3:0] bits are not valid.

OUT[3:0] These output bits can be programmed to output miscellaneous additional signals from the video decoder on VD[3:0]. The Programmable I/O register is only accessible in the 8-bit 4:2:2 YCrCb output mode. If not in the 8-bit output mode, the OUT[3:0] bits will be set to logical zero.



PARAMETRIC INFORMATION

DC Electrical Parameters

Table 14. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — Analog	V_{AA}	4.75	5.00	5.25	V
Power Supply — Digital	V_{DD}	4.75	5.00	5.25	V
Maximum $\Delta \lvert V_{DD} - V_{AA} \rvert$				0.5	V
MUX0, MUX1 and MUX2 Input Range (AC coupling required)		0.5	1.00	2.00	V
VIN Amplitude Range (ac coupling required)		0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	˚C

Table 15. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
V_{AA} (measured to AGND)				7.00	V
V_{DD} (measured to DGND)				7.00	V
Voltage on any signal pin (See the note below)		DGND – 0.5		V_{DD} + 0.5	V
Analog Input Voltage		AGND – 0.5		V_{AA} + 0.5	V
Storage Temperature	T_S	–65		+150	˚C
Junction Temperature	T_J			+125	˚C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			+220	˚C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latch-up.

Table 16. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		V_{DD} + 0.5	V
Input Low Voltage (TTL)	V_{IL}			0.8	V
Input High Voltage (XT0I, XT1I)	V_{IH}	3.5		V_{DD} + 0.5	V
Input Low Voltage (XT0I, XT1I)	V_{IL}	GND – 0.5		1.5	V
Input High Current (V_{IN}=V_{DD})	I_{IH}			10	µA
Input Low Current (V_{IN}=GND)	I_{IL}			–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}		5		pF
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4		V_{DD}	V
Output Low Voltage (I_{OL}= 3.2 mA)	V_{OL}			0.4	V
Three-State Current	I_{OZ}			10	µA
Output Capacitance	C_O		5		pF
Analog Pin Input Capacitance	C_A		5		pF

AC Electrical Parameters

Table 17. Clock Timing Parameters *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
NTSC: CLKx1 Rate CLKx2 Rate (50 PPM source required)	 F_{S1} F_{S2}		 14.318181 28.636363		 MHz MHz
PAL/SECAM: CLKx1 Rate CLKx2 Rate (50 PPM source required)	 F_{S1} F_{S2}		 17.734475 35.468950		 MHz MHz
XT0 and XT1 Inputs Cycle Time High Time Low Time	 1 2 3	 28.2 12 12			 ns ns ns

Table 17. Clock Timing Parameters *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
CLKx1 Duty Cycle		45		55	%
CLKx2 Duty Cycle		40		60	%
CLKx2 to CLKx1 Delay	4	0		2	ns
CLKx1 to Data Delay	5	3		11	ns
CLKx2 to Data Delay	6	3		11	ns
CLKx1 (Falling Edge) to QCLK (Rising Edge)	41	0		8	ns
CLKx2 (Falling Edge) to QCLK (Rising Edge)	42	0		8	ns
8-bit Mode(1)					
Data to QCLK (Rising Edge) Delay	7b	5			ns
QCLK (Rising Edge) to Data Delay	8b	15			ns
16-bit Mode(1)					
Data to QCLK (Rising Edge) Delay	7a	14			ns
QCLK (Rising Edge) to Data Delay	8a	25			ns

Notes: (1). Because QCLK is generated with a gated version of CLKx1 or CLKx2, the timing in symbols 7 and 8 are subject to changes in the duty cycle of CLKx1 and CLKx2. If crystals are used as clock sources for the Bt829A, the duty cycle is symmetric. This assumption is used to generate the timing numbers shown in 7 and 8. For non-symmetric clock sources, use the following equations:

Data to QCLK (setup) (16-bit mode)	xtal period + clkx1 to qclk (max) - clkx1 to data (max) or symbol 1 + symbol 41 (max) - symbol 5 (max) NTSC: 34.9 nS + 8 nS - 11 nS = 31.9 nS PAL: 28.2 nS + 8 nS -11 nS = 25.2 nS
QCLK to Data (hold) (16-bit mode)	xtal period - clkx1 to qclk (min) + clkx1 to data (min) or symbol 1 - symbol 41 (min) + symbol 5 (min) NTSC: 34.9 nS - 0 nS + 3 nS = 37.9 nS PAL: 28.3 nS - 0 nS + 3 nS = 31.3 nS
Data to QCLK (setup) (8-bit mode)	(xtal period)/2 + clkx2 to qclk (max) - clkx2 to data (max) or (symbol 1)/2 + symbol 42 (max) - symbol 6 (max) NTSC: 17.5 nS + 8nS - 11 nS = 14.5 nS PAL: 14.1 nS + 8 nS - 11 nS = 11.1 nS
QCLK to data (hold) (8-bit mode)	(xtal period)/2 - clkx2 to qclk (min) + clkx2 to data (min) or (symbol 1)/2 - symbol 42 (min) + symbol 6 (min) NTSC: 17.5 nS - 0 nS + 3 nS = 20.5 nS PAL: 14.1 nS - 0 nS + 3 nS = 17.1 nS

Figure 48. Clock Timing Diagram

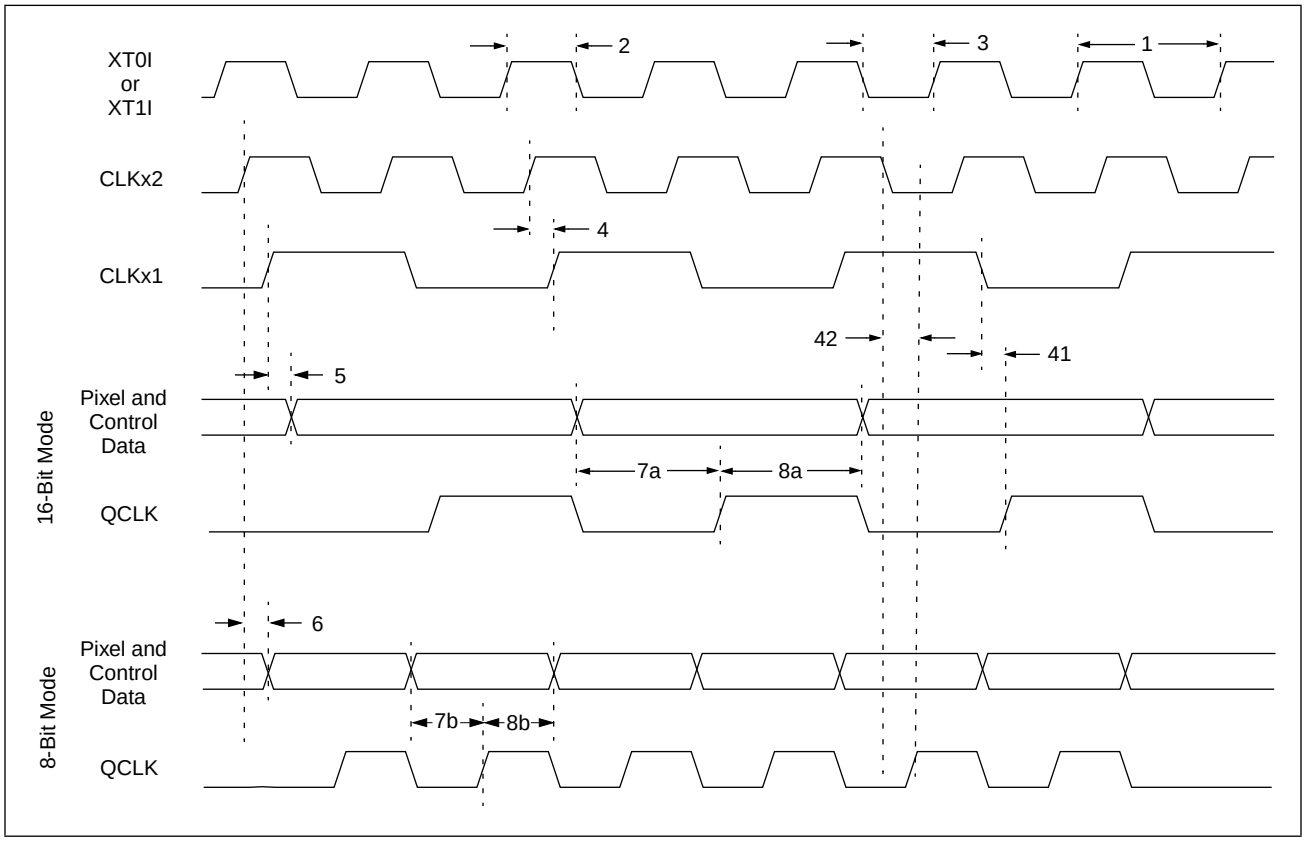


Table 18. Power Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I				
$V_{AA}=V_{DD}$=5.0V, F_{CLKx2}=28.64 MHz, T=25˚C			170		mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=70˚C				250	mA
$V_{AA}=V_{DD}$=5.25V, F_{CLKx2}=35.47 MHz, T=0˚C				280	mA
Supply Current, Power Down			65		mA

Table 19. Output Enable Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
$\overline{OE}$ Asserted to Data Bus Driven	9	0			nS
$\overline{OE}$ Asserted to Data Valid	10			100	nS
$\overline{OE}$ Negated to Data Bus Not Driven	11			100	nS
$\overline{RST}$ Low Time		8			XTAL cycles

Figure 49. Output Enable Timing Diagram

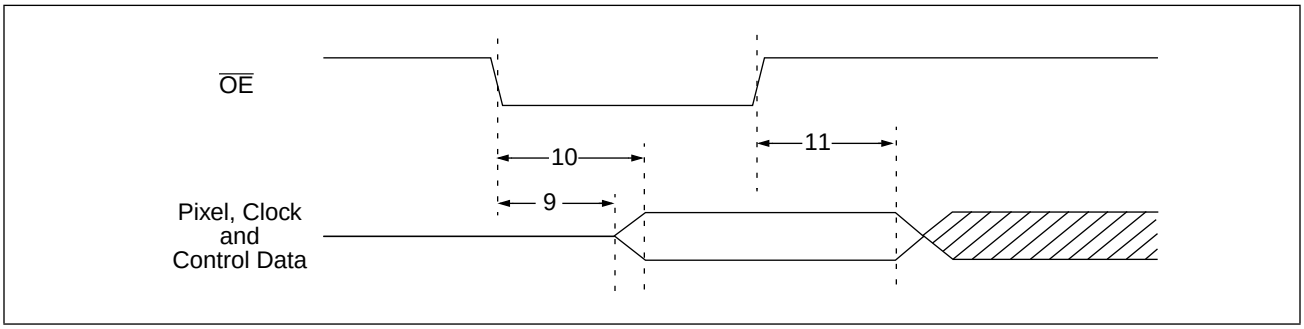


Table 20. JTAG Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
TMS, TDI Setup Time	12		10		ns
TMS, TDI Hold Time	13		10		ns
TCK Asserted to TDO Valid	14		60		ns
TCK Asserted to TDO Driven	15		5		ns
TCK Negated to TDO Three-stated	16		80		ns
TCK Low Time	17	25			ns
TCK High TIme	18	25			ns

Figure 50. JTAG Timing Diagram

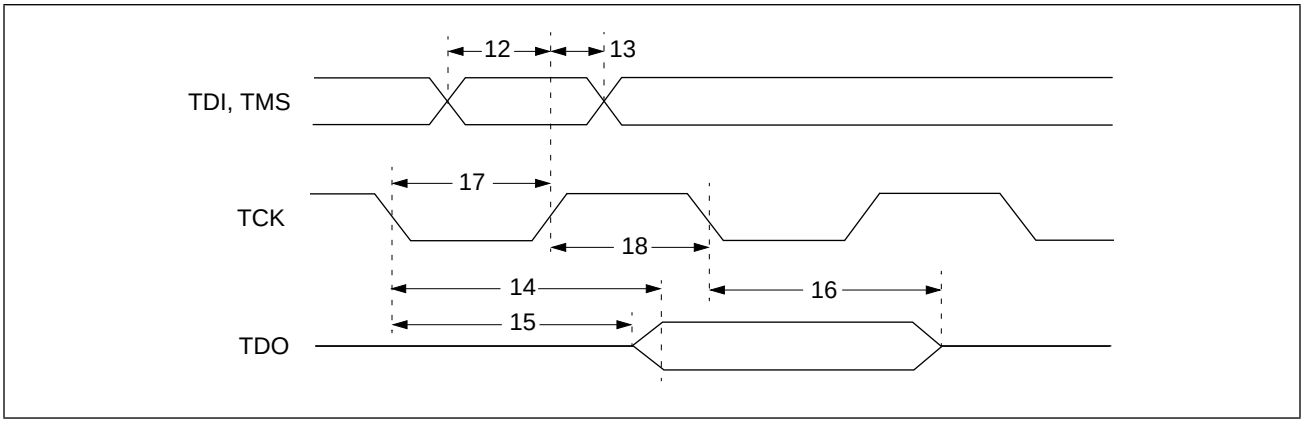


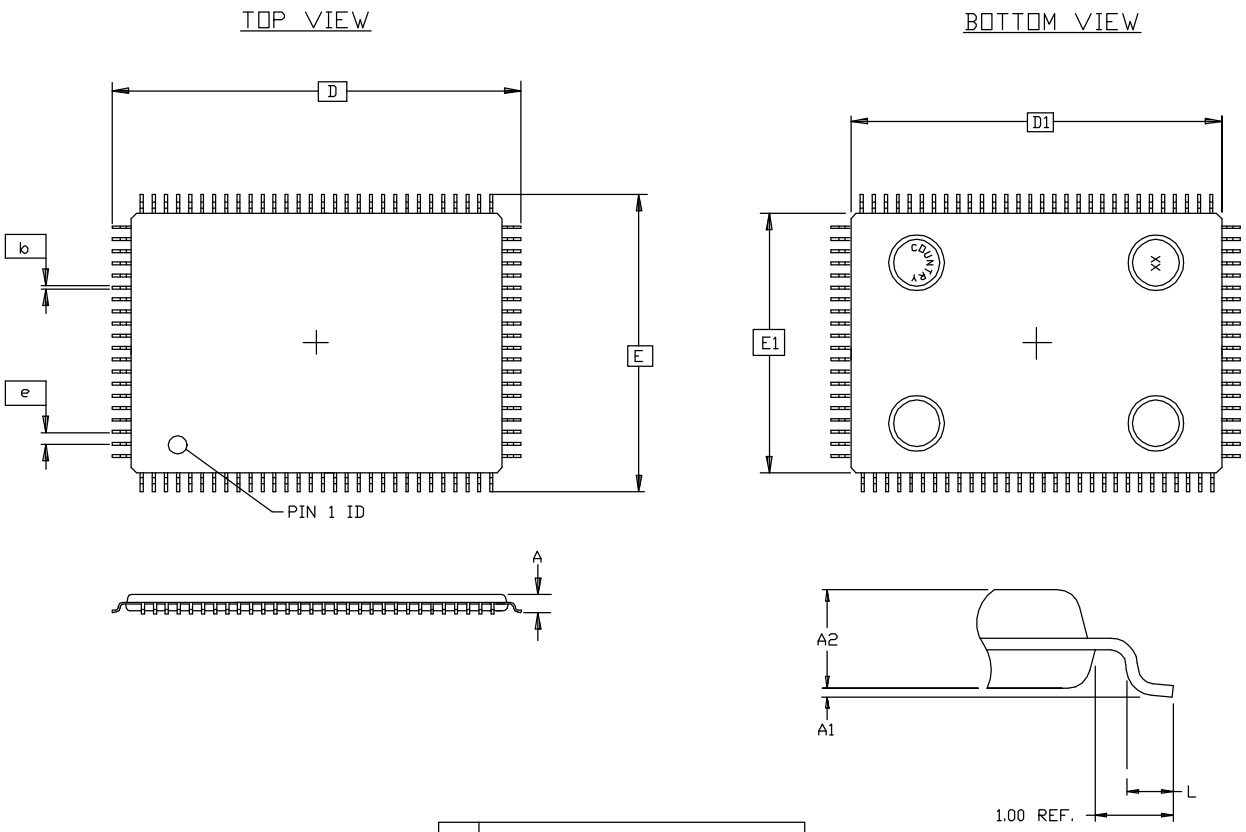
Table 21. Decoder Performance Parameters

Parameter	Symbol	Min	Typ	Max	Units
Horizontal Lock Range				±7	% of Line Length
Fsc, Lock-in Range		±800			Hz
Gain Range		–6		6	dB

Note: Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. Pixel and control data loads ≤ 30 pF and ≥10 pF. CLKx1 and CLKx2 loads ≤ 50 pF. Control data includes CBFLAG, DVALID, ACTIVE, VACTIVE, $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$ and FIELD.

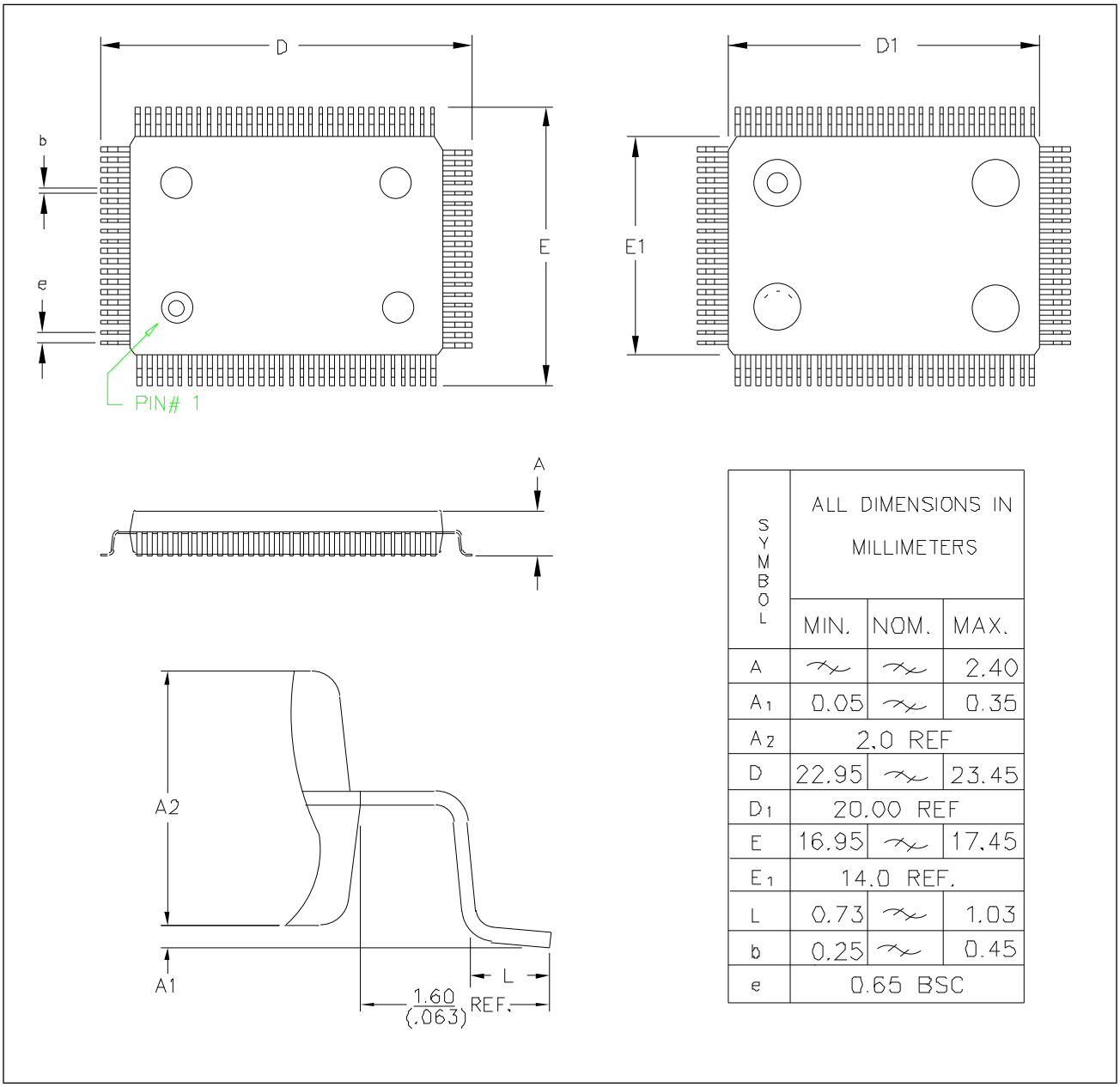
Package Mechanical Drawings

Figure 51. 100-pin TQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
D		22.00 BSC.	
D_1		20.00 BSC.	
E		16.00 BSC.	
E_1		14.00 BSC.	
L	0.45	0.60	0.75
e		0.65 BSC	
b	0.22	0.32	0.38

Figure 52. 100-Pin PQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			2.40
A_1	0.05		0.35
A_2	2.0 REF		
D	22.95		23.45
D_1	20.00 REF		
E	16.95		17.45
E_1	14.0 REF.		
L	0.73		1.03
b	0.25		0.45
e	0.65 BSC		

Revision History

Table 22. Bt829A Datasheet Revision History

Revision	Date	Description
A	01/24/97	Engineering Release
B	11/97	Clarification of functional differences between the Bt829A and Bt829 products. Removal of Bt825A video decoder information.

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