

*Designer's™ Data Sheet*  
**SWITCHMODE™**  
**NPN Bipolar Power Transistor**  
**For Switching Power Supply Applications**

The BUL44/BUL44F have an applications specific state-of-the-art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain  $h_{FE}$
  - Fast Switching
  - No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Full Characterization at 125°C
- Tight Parametric Distributions are Consistent Lot-to-Lot
- Two Package Choices: Standard TO-220 or Isolated TO-220
- BUL44F, Case 221D, is UL Recognized to 3500 V<sub>RMS</sub>: File #E69369

**MAXIMUM RATINGS**

Rating	Symbol	BUL44	BUL44F	Unit
Collector-Emitter Sustaining Voltage	V <sub>CEO</sub>	400		Vdc
Collector-Emitter Breakdown Voltage	V <sub>CES</sub>	700		Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	9.0		Vdc
Collector Current — Continuous	I <sub>C</sub>	2.0		Adc
— Peak(1)	I <sub>CM</sub>	5.0		
Base Current — Continuous	I <sub>B</sub>	1.0		Adc
— Peak(1)	I <sub>BM</sub>	2.0		
RMS Isolated Voltage(2)	V <sub>ISOL</sub>	—	4500	Volts
(for 1 sec, R.H. < 30%,	Test No. 1 Per Fig. 22a	—	3500	
T <sub>C</sub> = 25°C)	Test No. 2 Per Fig. 22b	—	1500	
Total Device Dissipation	P <sub>D</sub>	50	25	Watts
Derate above 25°C		0.4	0.2	W/°C
Operating and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 65 to 150		°C

**THERMAL CHARACTERISTICS**

Rating	Symbol	BUL44	BUL44F	Unit
Thermal Resistance — Junction to Case	R <sub>θJC</sub>	2.5	5.0	°C/W
— Junction to Ambient	R <sub>θJA</sub>	62.5	62.5	
Maximum Lead Temperature for Soldering	T <sub>L</sub>	260		°C
Purposes: 1/8" from Case for 5 Seconds				

**ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	400	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	—	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	—	—	100	μAdc
(T <sub>C</sub> = 125°C)		—	—	500	
(V <sub>CE</sub> = 500 V, V <sub>EB</sub> = 0)		—	—	100	
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(2) Proper strike and creepage distance must be provided.

(continued)

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**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

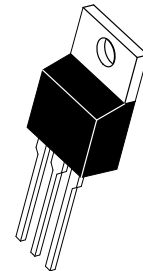
**Preferred** devices are Motorola recommended choices for future use and best overall value.

REV 1

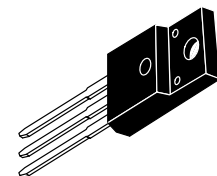
**BUL44\***  
**BUL44F\***

\*Motorola Preferred Device

**POWER TRANSISTOR**  
**2.0 AMPERES**  
**700 VOLTS**  
**40 and 100 WATTS**



**BUL44**  
**CASE 221A-06**  
**TO-220AB**



**BUL44F**  
**CASE 221D-02**  
**ISOLATED TO-220 TYPE**  
**UL RECOGNIZED**

# BUL44 BUL44F

## ELECTRICAL CHARACTERISTICS — continued (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Base–Emitter Saturation Voltage (I <sub>C</sub> = 0.4 Adc, I <sub>B</sub> = 40 mAcd) (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>BE(sat)</sub>	— —	0.85 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.4 Adc, I <sub>B</sub> = 40 mAcd)  (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>CE(sat)</sub>	— — — —	0.20 0.20 0.25 0.25	0.5 0.5 0.6 0.6	Vdc
DC Current Gain (I <sub>C</sub> = 0.2 Adc, V <sub>CE</sub> = 5.0 Vdc)  (I <sub>C</sub> = 0.4 Adc, V <sub>CE</sub> = 1.0 Vdc)  (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 1.0 Vdc)  (I <sub>C</sub> = 10 mAcd, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	14 — 12 12 8.0 7.0 10	— 32 20 20 14 13 22	34 — — — — — —	—

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	—	13	—	MHz		
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>OB</sub>	—	38	60	pF		
Input Capacitance (V <sub>EB</sub> = 8.0 V)	C <sub>IB</sub>	—	380	600	pF		
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub>	(I <sub>C</sub> = 0.4 Adc I <sub>B1</sub> = 40 mAcd V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	V <sub>CE(dsat)</sub>	—	2.5	—	Vdc
		3.0 μs (T <sub>C</sub> = 125°C)		—	2.7	—	
	(I <sub>C</sub> = 1.0 Adc I <sub>B1</sub> = 0.2 Adc V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)		—	1.3	—	
		3.0 μs (T <sub>C</sub> = 125°C)		—	1.15	—	
				—	3.2	—	
				—	7.5	—	
				—	1.25	—	
				—	1.6	—	

## SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn–On Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAcd I <sub>B2</sub> = 0.2 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	— —	40 40	100 —	ns
Turn–Off Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAcd I <sub>B2</sub> = 0.2 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>off</sub>	— —	1.5 2.0	2.5 —	μs
Turn–On Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>on</sub>	— —	85 85	150 —	ns
Turn–Off Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc, V <sub>CC</sub> = 300 V)	(T <sub>C</sub> = 125°C)	t <sub>off</sub>	— —	1.75 2.10	2.5 —	μs

## SWITCHING CHARACTERISTICS: Inductive Load (V<sub>clamp</sub> = 300 V, V<sub>CC</sub> = 15 V, L = 200 μH)

Fall Time	(I <sub>C</sub> = 0.4 Adc, I <sub>B1</sub> = 40 mAcd I <sub>B2</sub> = 0.2 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	— —	125 120	200 —	ns
Storage Time			t <sub>si</sub>	— —	0.7 0.8	1.25 —	μs
Crossover Time			t <sub>c</sub>	— —	110 110	200 —	ns
Fall Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.2 Adc I <sub>B2</sub> = 0.5 Adc)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	— —	110 120	175 —	ns
Storage Time			t <sub>si</sub>	— —	1.7 2.25	2.75 —	μs
Crossover Time			t <sub>c</sub>	— —	180 210	300 —	ns
Fall Time	(I <sub>C</sub> = 0.8 Adc, I <sub>B1</sub> = 160 mAcd I <sub>B2</sub> = 160 mAcd)	(T <sub>C</sub> = 125°C)	t <sub>fi</sub>	70 —	— 180	170 —	ns
Storage Time			t <sub>si</sub>	2.6 —	— 4.2	3.8 —	μs
Crossover Time			t <sub>c</sub>	— —	190 350	300 —	ns

TYPICAL STATIC CHARACTERISTICS

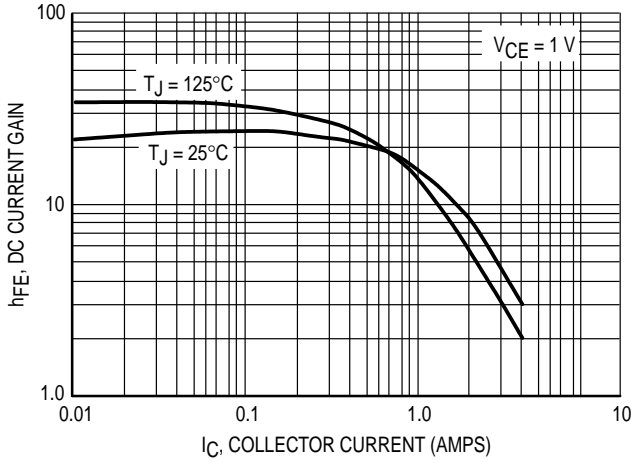


Figure 1. DC Current Gain at 1 Volt

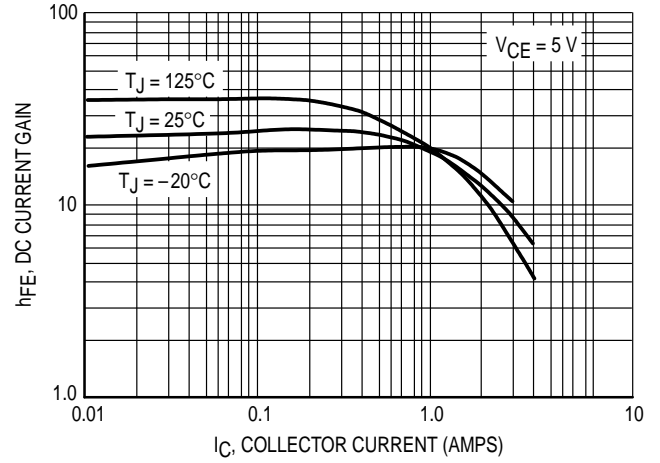


Figure 2. DC Current Gain at 5 Volts

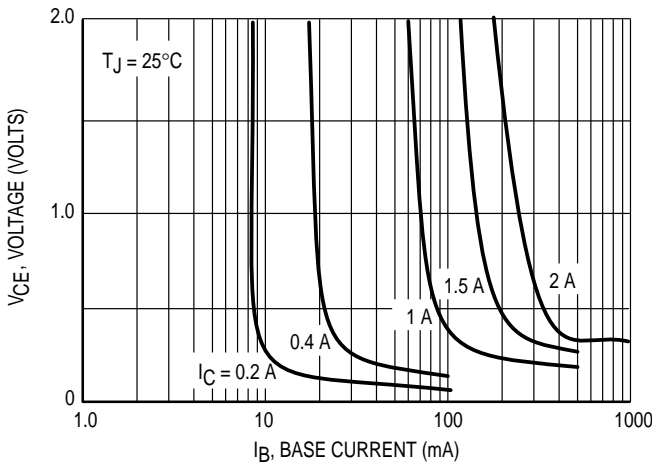


Figure 3. Collector Saturation Region

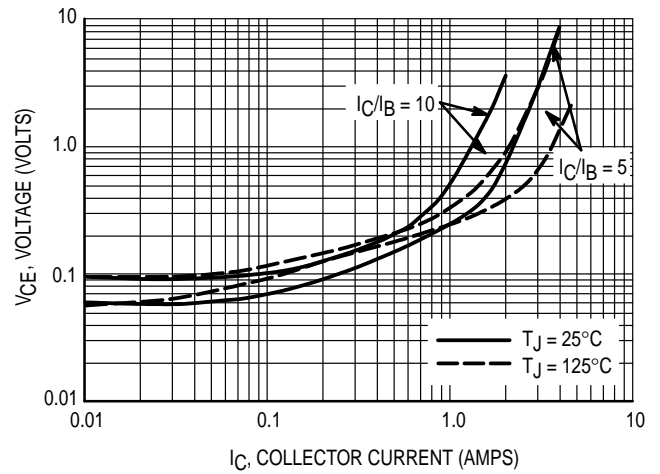


Figure 4. Collector-Emitter Saturation Voltage

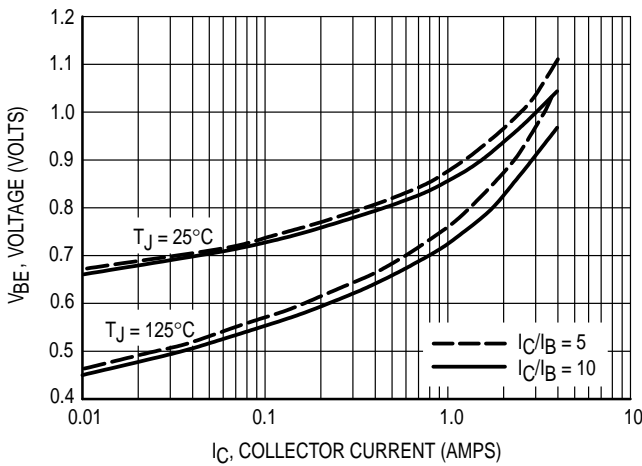


Figure 5. Base-Emitter Saturation Region

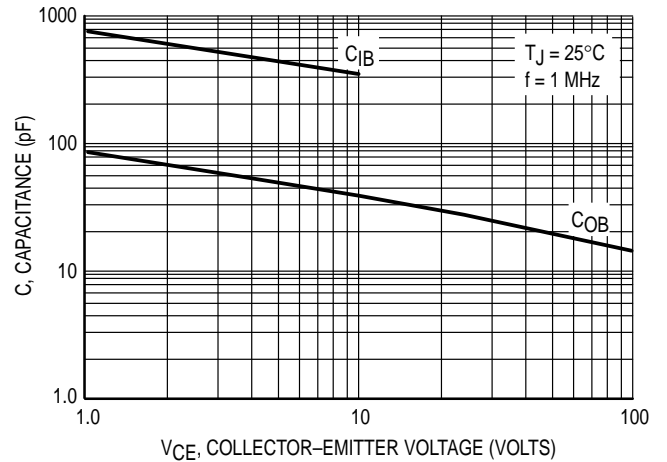


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS  
( $I_{B2} = I_C/2$  for all switching)

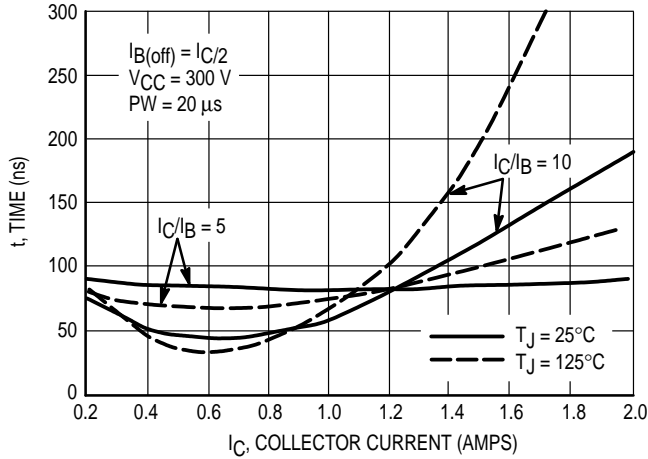


Figure 7. Resistive Switching,  $t_{on}$

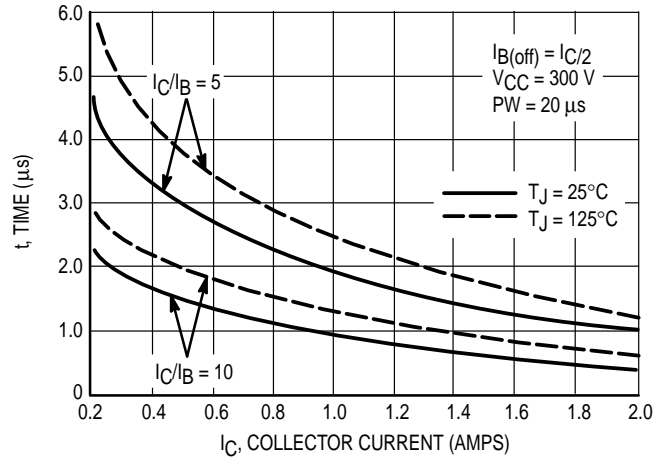


Figure 8. Resistive Switching,  $t_{off}$

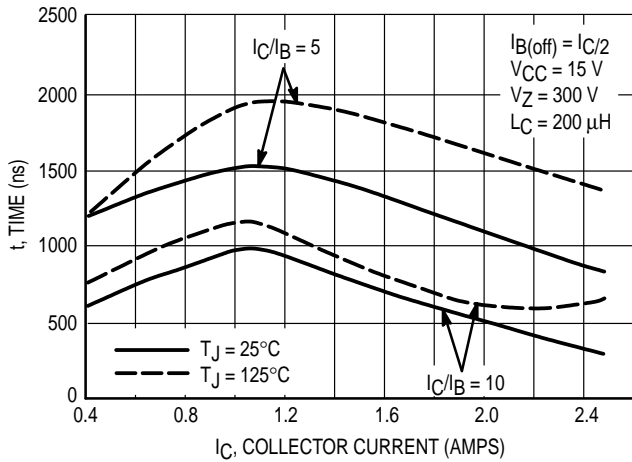


Figure 9. Inductive Storage Time,  $t_{si}$

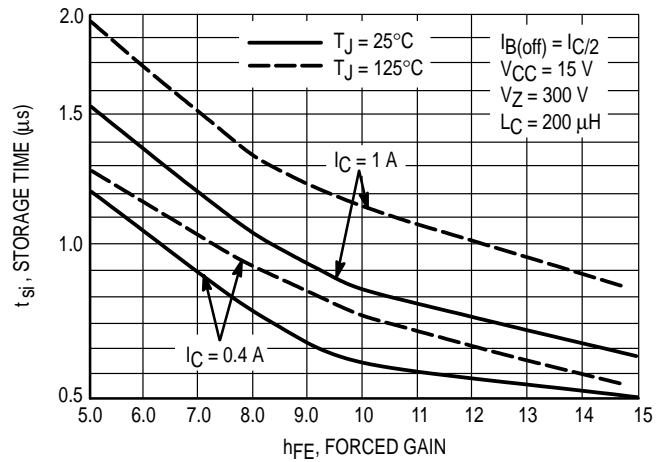


Figure 10. Inductive Storage Time

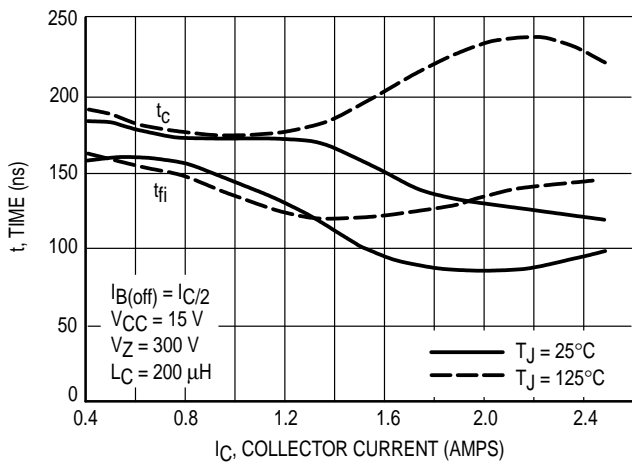


Figure 11. Inductive Switching,  $t_c$  and  $t_{fi}$   $I_C/I_B = 5$

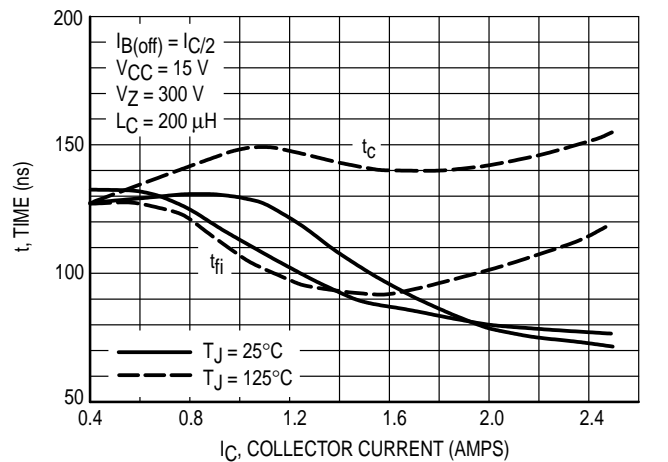


Figure 12. Inductive Switching,  $t_c$  and  $t_{fi}$   $I_C/I_B = 10$

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

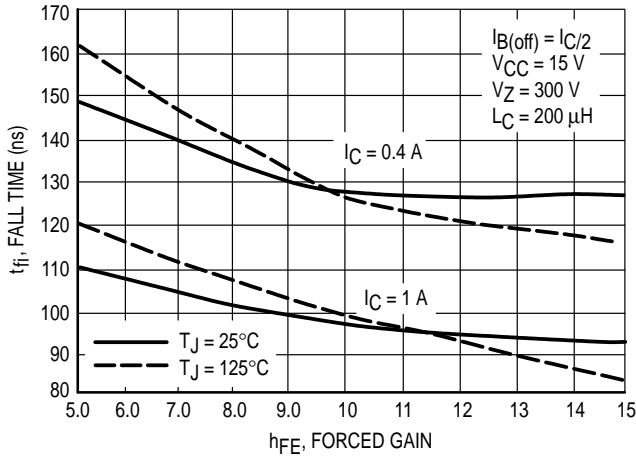


Figure 13. Inductive Fall Time

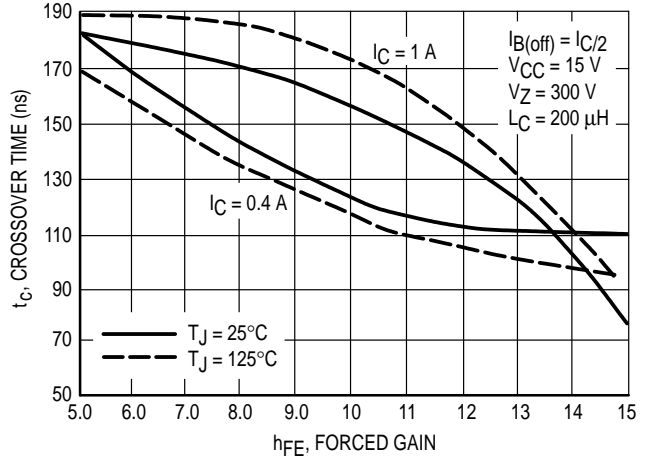


Figure 14. Inductive Crossover Time

**GUARANTEED SAFE OPERATING AREA INFORMATION**

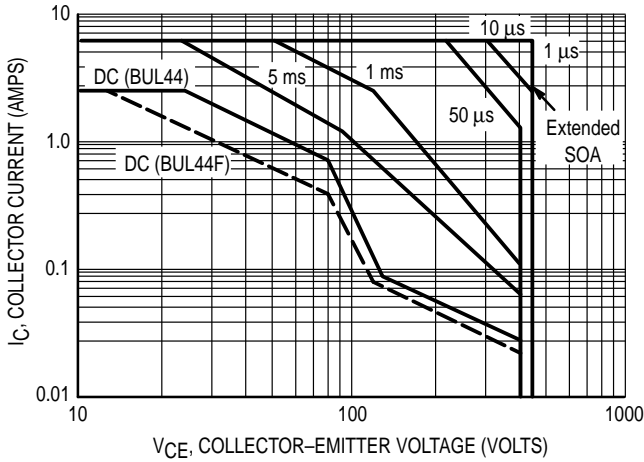


Figure 15. Forward Bias Safe Operating Area

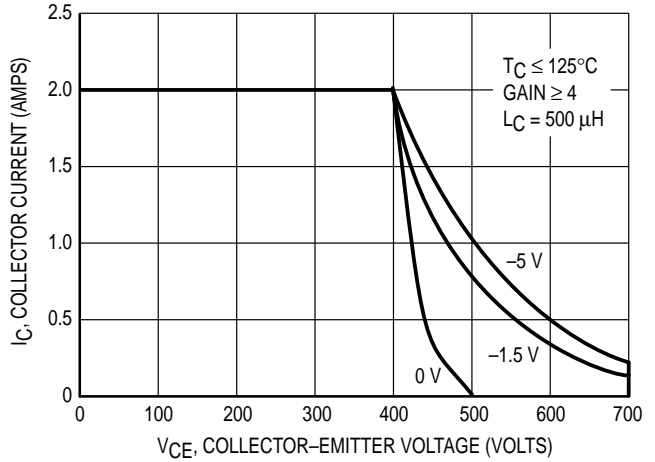


Figure 16. Reverse Bias Switching Safe Operating Area

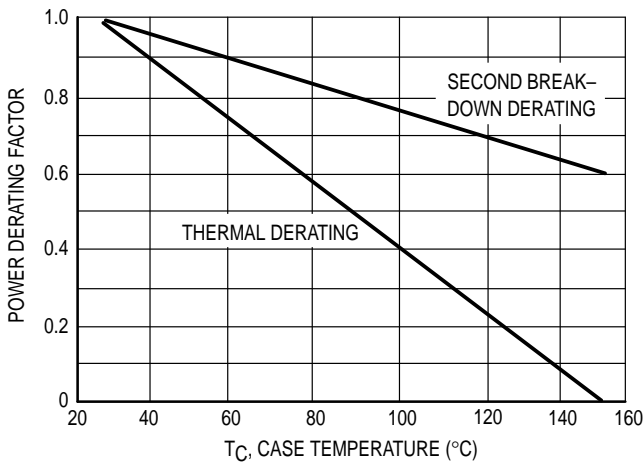
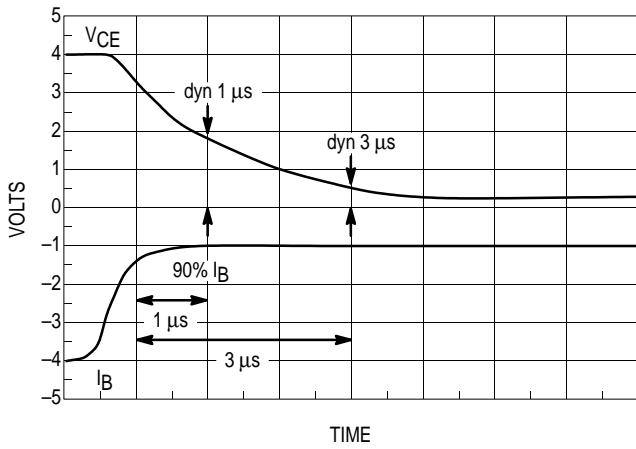
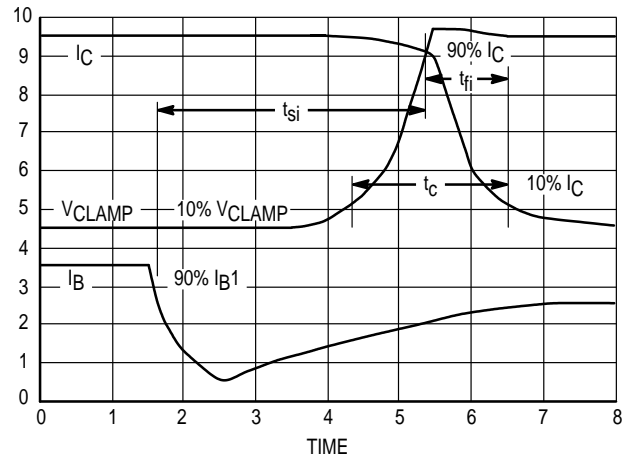


Figure 17. Forward Bias Power Derating

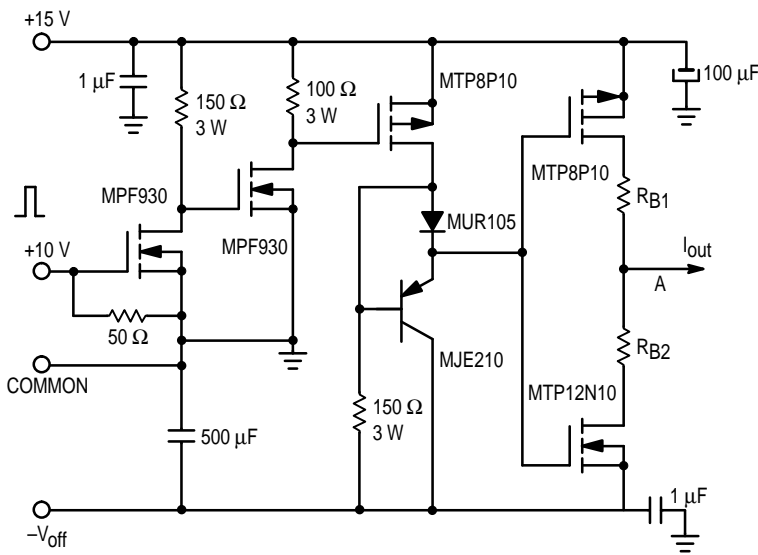
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on figure 15 may be found at any case temperature by using the appropriate curve on figure 17.  $T_{J(PK)}$  may be calculated from the data in figure 20 and 21. At any case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.



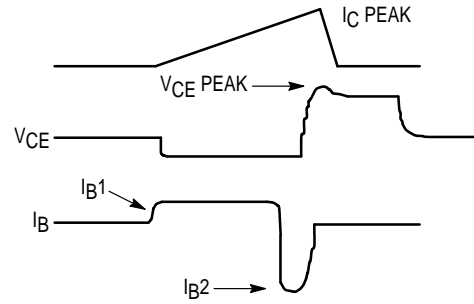
**Figure 18. Dynamic Saturation Voltage Measurements**



**Figure 19. Inductive Switching Measurements**



**Table 1. Inductive Load Switching Drive Circuit**



<b>V(BR)CEO(sus)</b>	<b>INDUCTIVE SWITCHING</b>	<b>RBSOA</b>
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

TYPICAL THERMAL RESPONSE

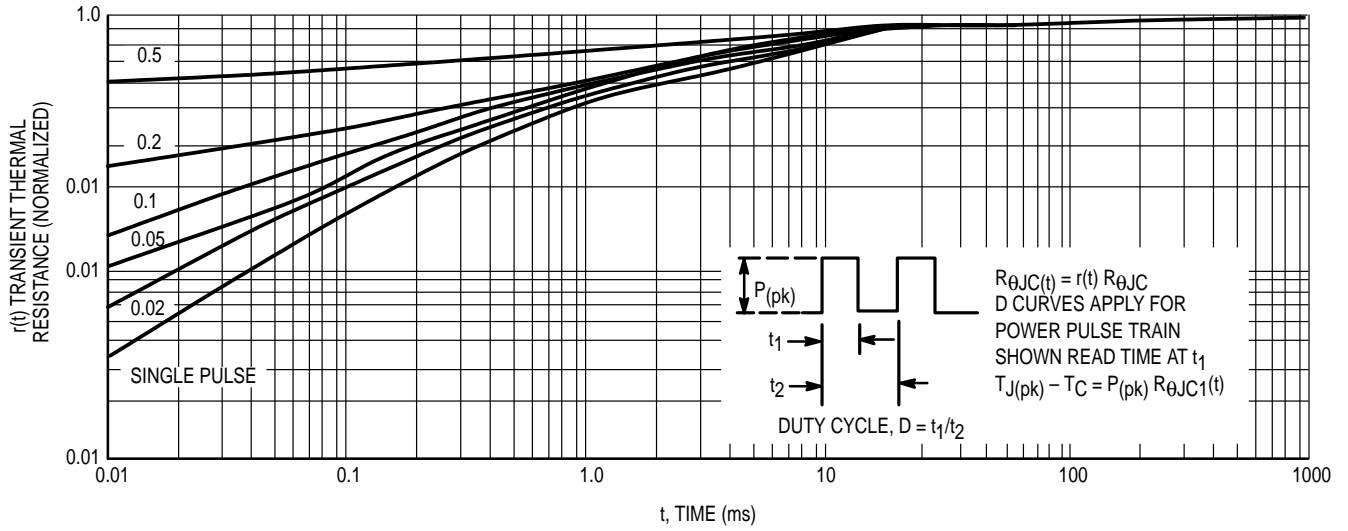


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL44

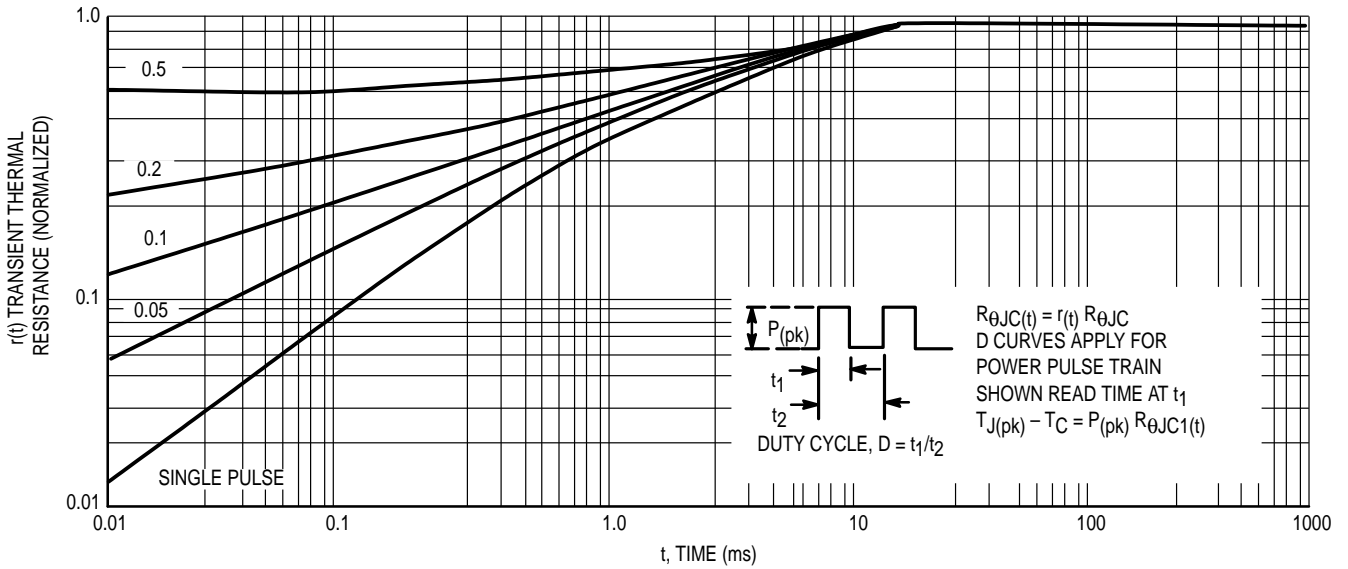
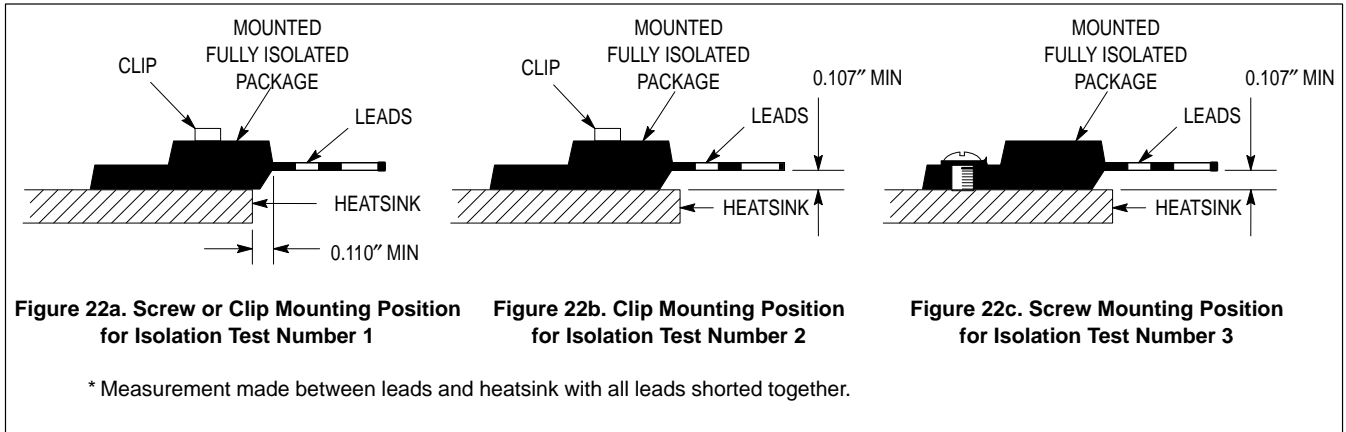
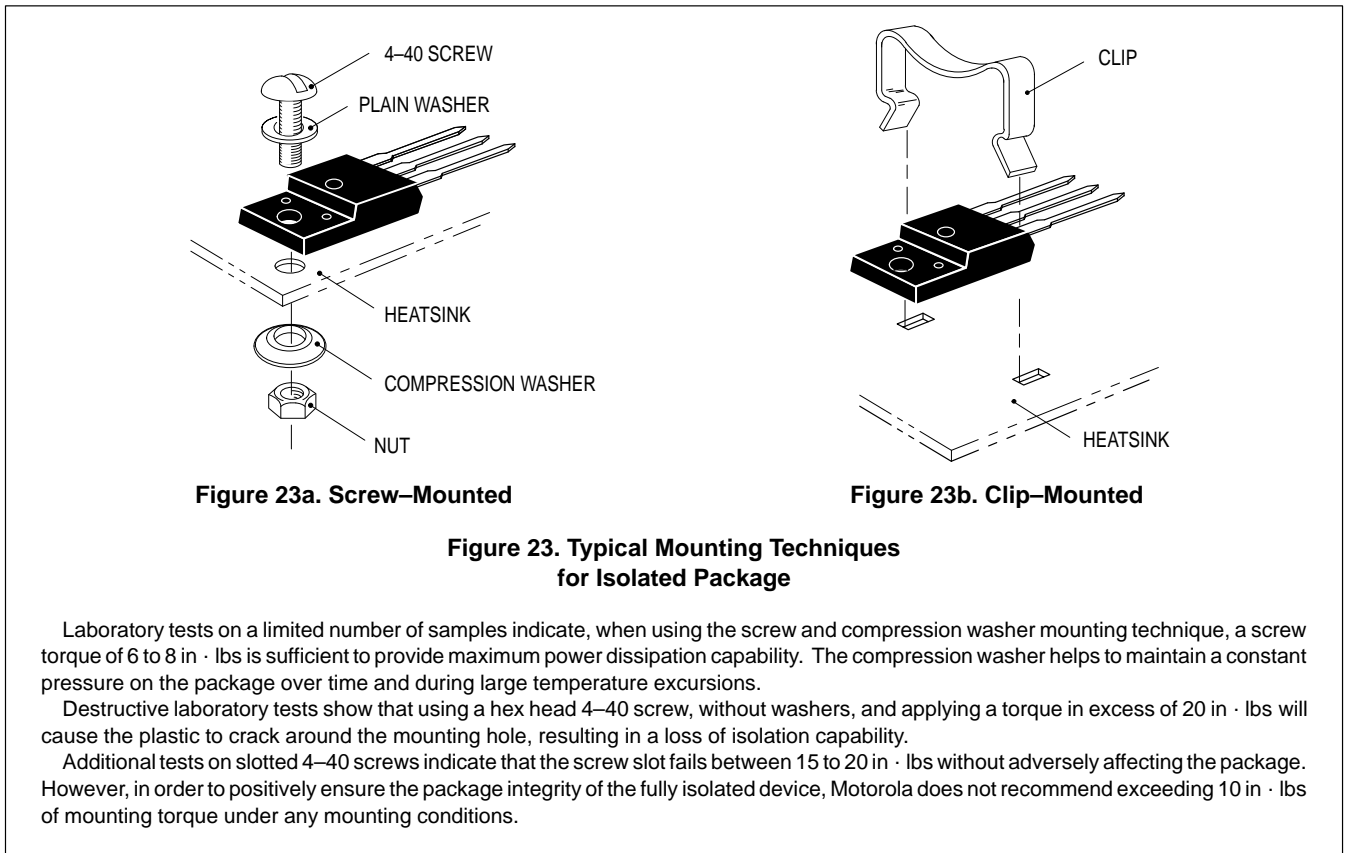


Figure 21. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL44F

TEST CONDITIONS FOR ISOLATION TESTS\*



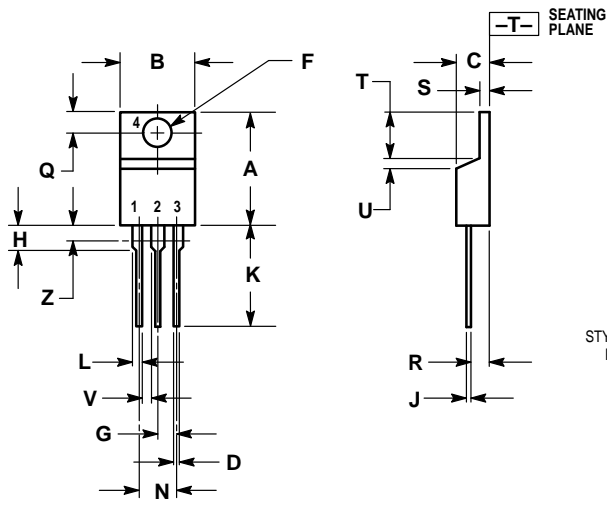
MOUNTING INFORMATION\*\*



\*\* For more information about mounting power semiconductors see Application Note AN1040.



PACKAGE DIMENSIONS

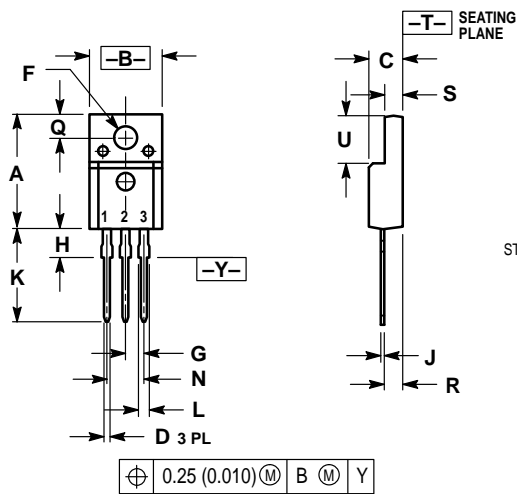


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

**BUL44**  
**CASE 221A-06**  
**TO-220AB**  
**ISSUE Y**




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC	—	2.54 BSC	—
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC	—	5.08 BSC	—
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

- STYLE 2:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER

**BUL44F**  
**CASE 221D-02**  
**(ISOLATED TO-220 TYPE)**  
**ISSUE D**

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