

Process C1210

CMOS 1.2 μ m

Zero Threshold Devices

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_N}	0.55	0.75	0.95	V	100x1.2 μ m
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2 μ m
Conduction Factor	β_N	64	75	86	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{eff_N}	0.8	1.0	1.2	μ m	100x1.2 μ m
Width Encroachment	ΔW_N		0.6		μ m	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

Zero Vt N-Channel Transis.	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	$V_{T_{ZLN}}$	0.00	0.15	0.30	V	100x100 μ m
Body Factor	γ_{ZLN}		0.348		$V^{1/2}$	100x100 μ m
Conduction Factor	β_{ZLN}	75	90	105	$\mu A/V^2$	100x100 μ m
Saturation Current	I_{DSATZN}	28	34	40	mA	100x1.5 μ m

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_P}	-0.7	-0.9	-1.1	V	100x1.2 μ m
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2 μ m
Conduction Factor	β_P	21	25	29	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{eff_P}	0.9	1.1	1.3	μ m	100x1.2 μ m
Width Encroachment	ΔW_P		0.8		μ m	Per side
Punch Through Voltage	$BVDSS_P$	-9.0			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-10.0			V	

Zero Vt P-Channel Transis.	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	$V_{T_{ZLP}}$	-0.3	-0.1	0.1	V	100x100 μ m
Body Factor	γ_{ZLP}		0.36		$V^{1/2}$	100x100 μ m
Conduction Factor	β_{ZLP}	21	26	31	$\mu A/V^2$	100x100 μ m
Saturation Current	I_{DSATZP}	-11	-15	-19	mA	100x1.5 μ m

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Electrical Characteristics

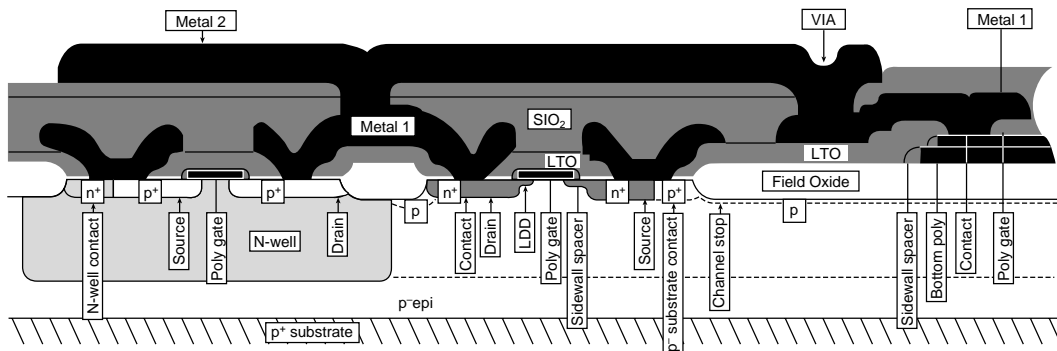
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well}(f)}$	0.6	1.0	1.3	$K\Omega/\square$	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/\square	
N+ Junction Depth	x_{jN+}		0.35		μm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/\square	
P+ Junction Depth	x_{jP+}		0.35		μm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	22	30	Ω/\square	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}		50		$m\Omega/\square$	
Metal-2 Sheet Resistance	ρ_{M2}		30		$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$\text{fF}/\mu\text{m}^2$	
Metal-1 to Poly-1	C_{M1P}		0.057		$\text{fF}/\mu\text{m}^2$	
Metal-1 to Silicon	C_{M1S}				$\text{fF}/\mu\text{m}^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$\text{fF}/\mu\text{m}^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$\text{fF}/\mu\text{m}^2$	

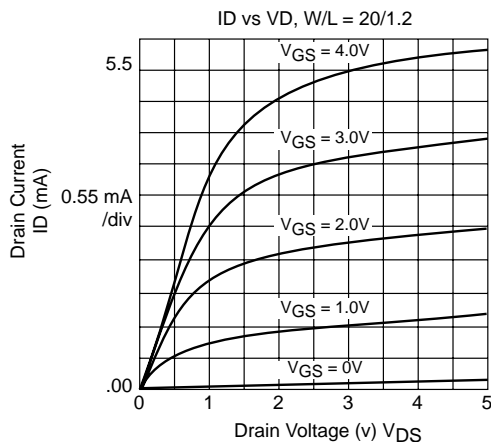
Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.5/ 2.0 μ m
Starting Mat. Resistivity	7 - 8.5 Ω -cm	N+ To P+ Space	9.0 μ m
Typ. Operating Voltage	5V	Contact To Poly Space	1.5 μ m
Well Type	N-well	Contact Overlap Of Diffusion	1.0 μ m
Metal Layers	2	Contact Overlap Of Poly	1.0 μ m
Poly Layers	2	Metal-1 Overlap Of Contact	1.0 μ m
Contact Size	1.5x1.5 μ m	Metal-1 Overlap Of Via	1.0 μ m
Via Size	1.5x1.5 μ m	Metal-2 Overlap Of Via	1.0 μ m
Metal-1 Width/Space	2.5 / 1.5 μ m	Minimum Pad Opening	65x65 μ m
Metal-2 Width/Space	2.5 / 1.5 μ m	Minimum Pad-to-Pad Spacing	5.0 μ m
Gate Poly Width/Space	1.5 / 2.0 μ m	Minimum Pad Pitch	80.0 μ m

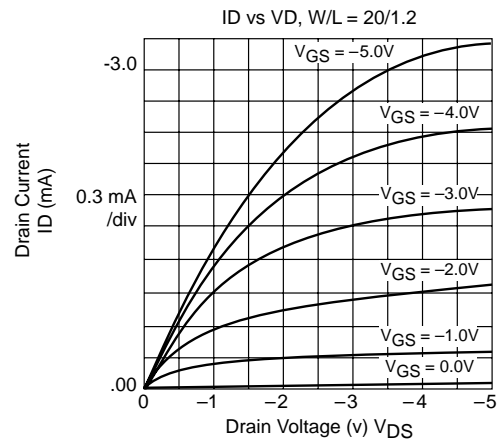
Special Feature of C1210 Process: This process offers zero threshold n- and p-channel transistors in addition to normal threshold transistors of CMOS 1.2 μ m technology.



Cross-Sectional view of the LVMOS process



n-ch Transistor IV characteristics of a 20/1.2 device



p-ch Transistor IV characteristics of a 20/1.2 device

