

**OBSOLETE PRODUCT  
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June 1999

## Speed Control System with Memory

### Features

- Low Power Dissipation
- I<sup>2</sup>L Control Logic
- Power-On Reset
- On-Chip Oscillator for System Time Reference
- Single Input Line for Operator Commands
- Amplitude Encoded Control Signals
- Transient Compensated Input Commands
- Controlled Acceleration Mode
- Internal Redundant Brake and Low-Speed Disable
- Braking Disable

### Applications

- Automotive Speed Control
- Residential and Industrial Heating and Cooling Controls
- Industrial AC and DC Motor Speed Control
- Applications Requiring Acceleration and Deceleration Control

### Description

The CA3228 is a monolithic integrated circuit designed as an automotive speed-control system.

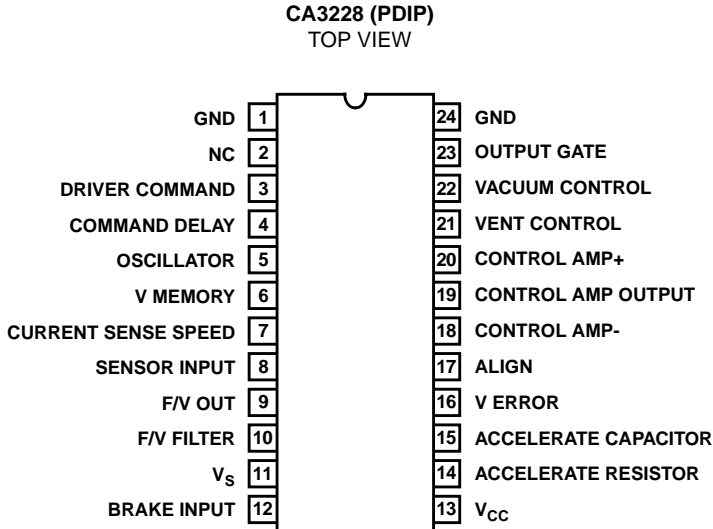
The system monitors vehicle speed and compares it to a stored reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed, set by the driver, is stored in a 9-bit counter.

The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate; the COAST command disables the servo, thereby forcing the vehicle to slowdown. Application of the brake disables the servo and places the system in the standby mode while the RESUME command returns the vehicle to the last stored speed.

Vehicle speed and driver commands are inputs to the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

The CA3228 is supplied in a 24 lead dual-in-line plastic package (E suffix). Refer to AN7326 for application information.

### Pinout



### Ordering Information

| PART NUMBER | TEMPERATURE    | PACKAGE             |
|-------------|----------------|---------------------|
| CA3228E     | -40°C to +85°C | 24 Lead Plastic DIP |

# Specifications CA3228

## Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| Supply Voltage, $V_{CC}$ .....                  | +9.0V           |
| Supply Current, $I_{CC}$ .....                  | 30mA            |
| Driver Command Input ( $I_{CMD}$ ), Pin 3 ..... | 2mA             |
| Brake Input ( $I_{BRAKE}$ ), Pin 12 .....       | 2mA             |
| Storage Temperature Range .....                 | -65°C to +150°C |
| Maximum Junction Temperature .....              | +150°C          |

## Thermal Information

|  |                              |
|--|------------------------------|
| Thermal Resistance   | $\theta_{JA}$                |
| Plastic DIP Package .....                                  | 65°C/W                       |
| Power Dissipation Per Package                              |                              |
| For $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$ ..... | 1.2mW                        |
| For $T_A$ Above $+70^\circ\text{C}$ .....                  | Derate Linearly at 15.4mW/°C |
| Lead Temperature (Soldering 10s) .....                     | +265°C                       |
| Operating Temperature Range .....                          | -40°C to +85°C               |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Typical Switching Characteristics

|   |  |       |
|---|--|-------|
| Driver Command Input Hold Times (Based on 0.68μF on Pin 4): | ON .....                                       | 50ms  |
| ACCEL .....   | OFF .....                                      | 50ms  |
| COAST .....   | Internal Oscillator Frequency, $F_{OSC}$ ..... | 10kHz |
| RESUME .....  | (Based on 0.001μF at Pin 5)                    |       |

## System Performance $F_{OSC} = 50\text{kHz}$ , $f_S/\text{Speed Ratio} = 2.22\text{Hz}/\text{mph}$

|   |               |                             |         |
|---|---------------|-----------------------------|---------|
| Speed Sensor Input Frequency Range, $f_S$ at Pin 8 .. | 62Hz to 222Hz | Maximum Stored Speed .....  | 100 mph |
| Speed Resolution .....                                | 0.45 mph      | Redundant Brake Speed ..... | 11 mph  |
| Minimum Operating Speed .....                         | 25 mph        |                             |         |

## Electrical Specifications $T_A = +25^\circ\text{C}$ , $V_{CC} = 8.20\text{V}$ , Unless Otherwise Specified (Refer to Figures 2 and 3)

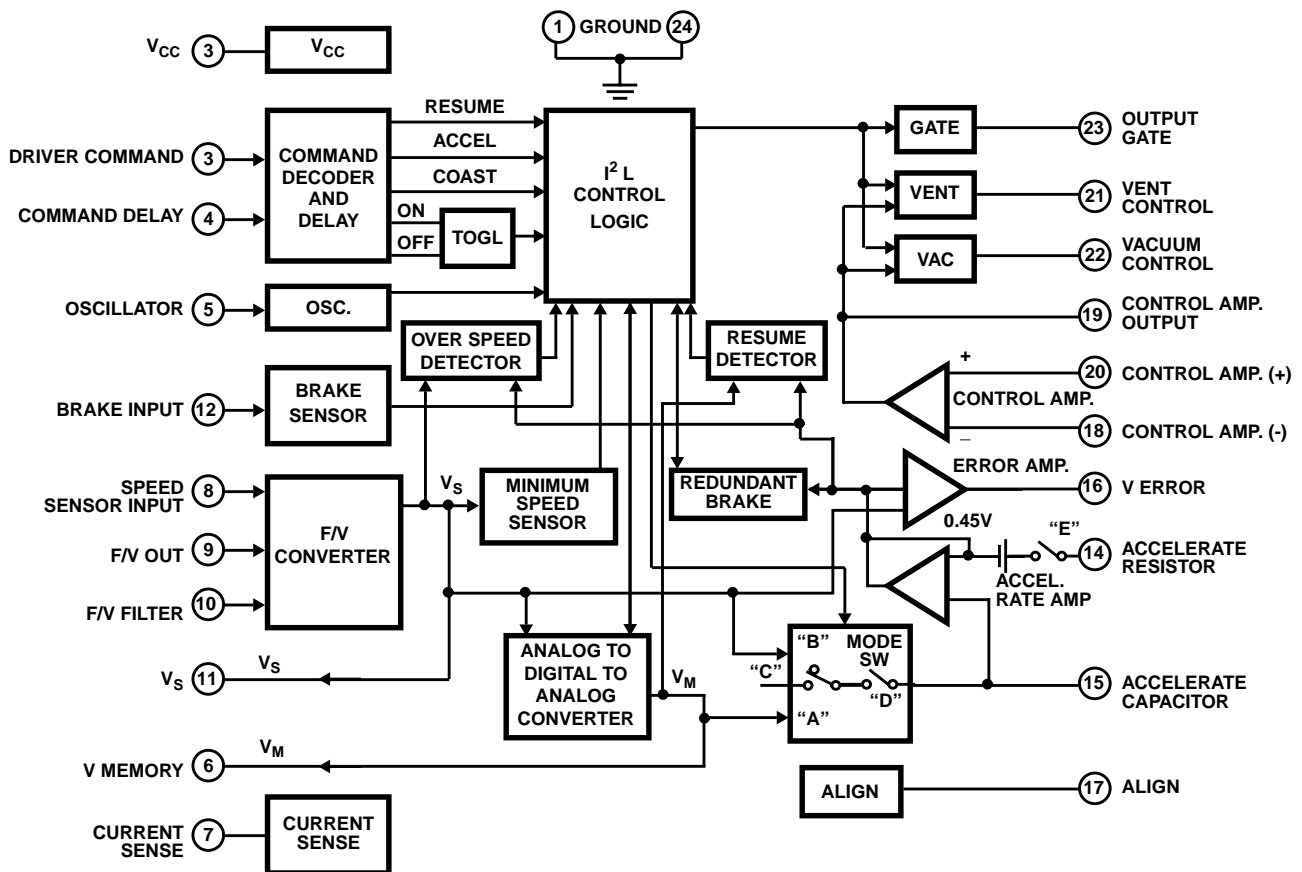
| PARAMETERS                           | SYMBOLS      | TEST PIN | TEST CONDITIONS                          | MIN  | MAX  | UNITS |
|--------------------------------------|--------------|----------|--|------|------|-------|
| Operating Voltage                    | $V_{CC}$     | 13       |  | 7.40 | 9.00 | V     |
| Speed Sensor Input Voltage Amplitude |              | T.P.B.   | $62\text{Hz} \leq f_S \leq 222\text{Hz}$ | 3.50 | 15.0 | Vpp   |
| $V_{CC}$ Supply Current              | $I_{CC}$     | 13       |  | 7.50 | 30.0 | mA    |
| Current Sense Voltage                | $V_7$        | 7        | 43kΩ to Ground                           | 4.85 | 5.95 | V     |
| Align Voltage                        | $V_{17}$     | 17       | 41kΩ to Ground                           | 4.00 | 4.20 | V     |
| Command Idle Voltage                 | $V_{3IDLE}$  | 3        | S1, S2, S3, S4, S5<br>Open               | 7.6  | 7.9  | V     |
| RESUME Command Voltage               | $V_{3RES}$   | 3        | S2 Closed                                | 5.95 | 6.56 | V     |
| ACCEL Command Voltage                | $V_{3ACCEL}$ | 3        | S3 Closed                                | 3.95 | 4.91 | V     |
| COAST Command Voltage                | $V_{3COAST}$ | 3        | S4 Closed                                | 1.22 | 2.23 | V     |
| OFF Voltage                          | $V_{3OFF}$   | 3        | S5 Closed                                | 0    | 0.77 | V     |
| ON Voltage                           | $V_{3ON}$    | T.P.A.   | S1 Closed                                | 9.2  | 28   | V     |
| Brake Input Voltage                  | $V_{BRAKE}$  | 12       | S6 Closed                                | 5.4  | 28   | V     |
| OUTPUT VOTLAGE                       |              |          |  |      |      |       |
| Gate                                 | $V_{OL}$     | 23       | 4.7kΩ to $V_{CC}$                        | -    | 300  | mV    |
|                                      | $V_{OH}$     |          |  | 8    | -    | V     |
| VAC                                  | $V_{OL}$     | 22       | 1.2kΩ to $V_{CC}$                        | -    | 400  | mV    |
|                                      | $V_{OH}$     |          |  | 8    | -    | V     |
| VENT                                 | $V_{OL}$     | 21       | 1.2kΩ to $V_{CC}$                        | -    | 400  | mV    |
|                                      | $V_{OH}$     |          |  | 8    | -    | V     |

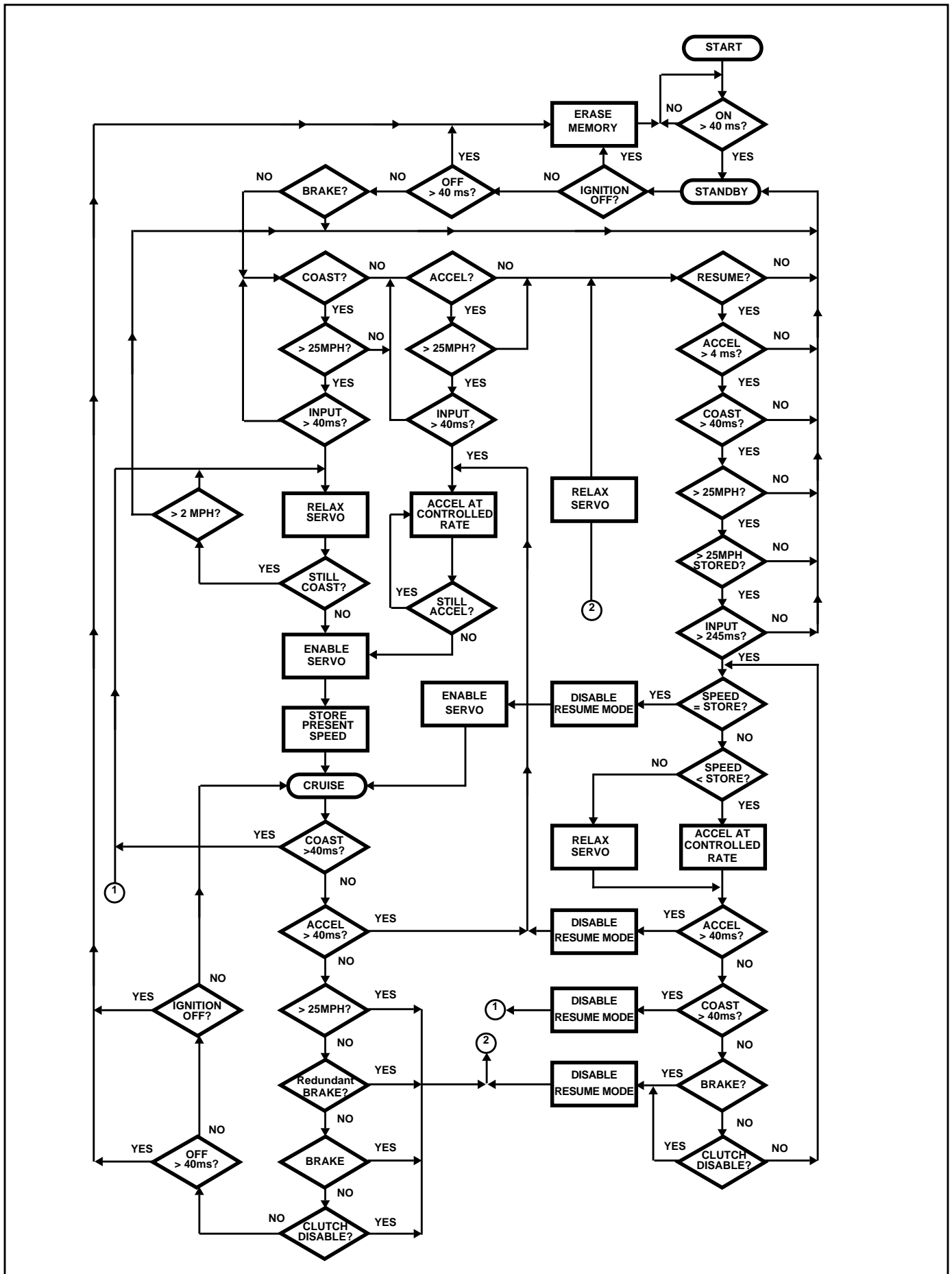
## Specifications CA3228

**Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 8.20\text{V}$ , Unless Otherwise Specified (Refer to Figures 2 and 3) **(Continued)**

| PARAMETERS                                | SYMBOLS        | TEST PIN | TEST CONDITIONS                 | MIN  | MAX  | UNITS |
|---|----------------|----------|---------------------------------|------|------|-------|
| Memory Set Error                          | $V_6 - V_{10}$ | 6, 10    |                                 | -77  | 67   | mV    |
| Deadband Range (VAC and VENT Outputs Off) | $V_{DB}$       | 21, 22   | Sweep Pin 19, Voltage at 1V/sec | 0.96 | 1.43 | V     |
| Control Amplifier Gain                    | $A_{CNTL}$     | 16, 19   | $A_{CNTL} = V_{19}/V_{16}$      | 74   | -    | Ratio |
| D/A Voltage Range                         | $V_M$          | 6        | Set Mode                        | 6    | 7.50 | V     |

### Functional Block Diagram





# CA3228

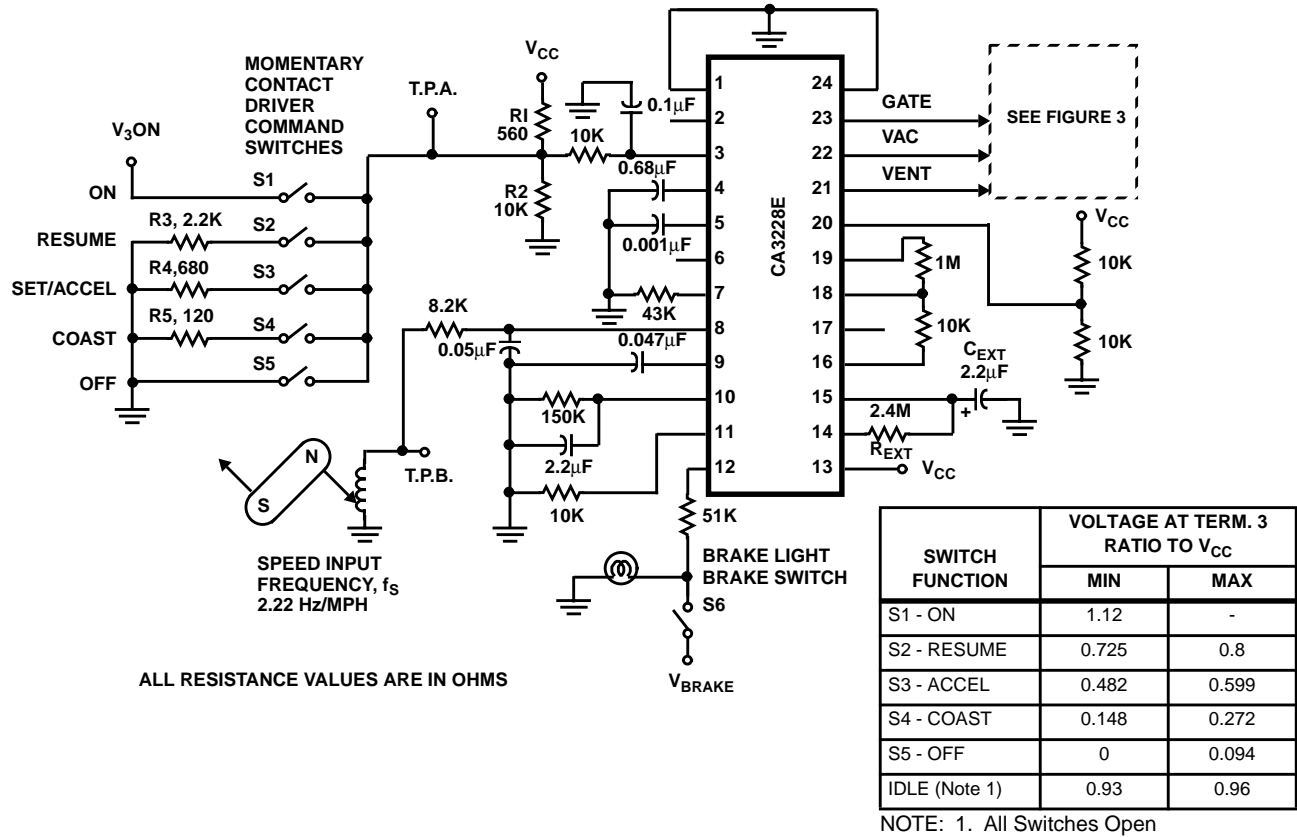


FIGURE 2. TYPICAL AUTOMOTIVE SPEED CONTROL APPLICATION

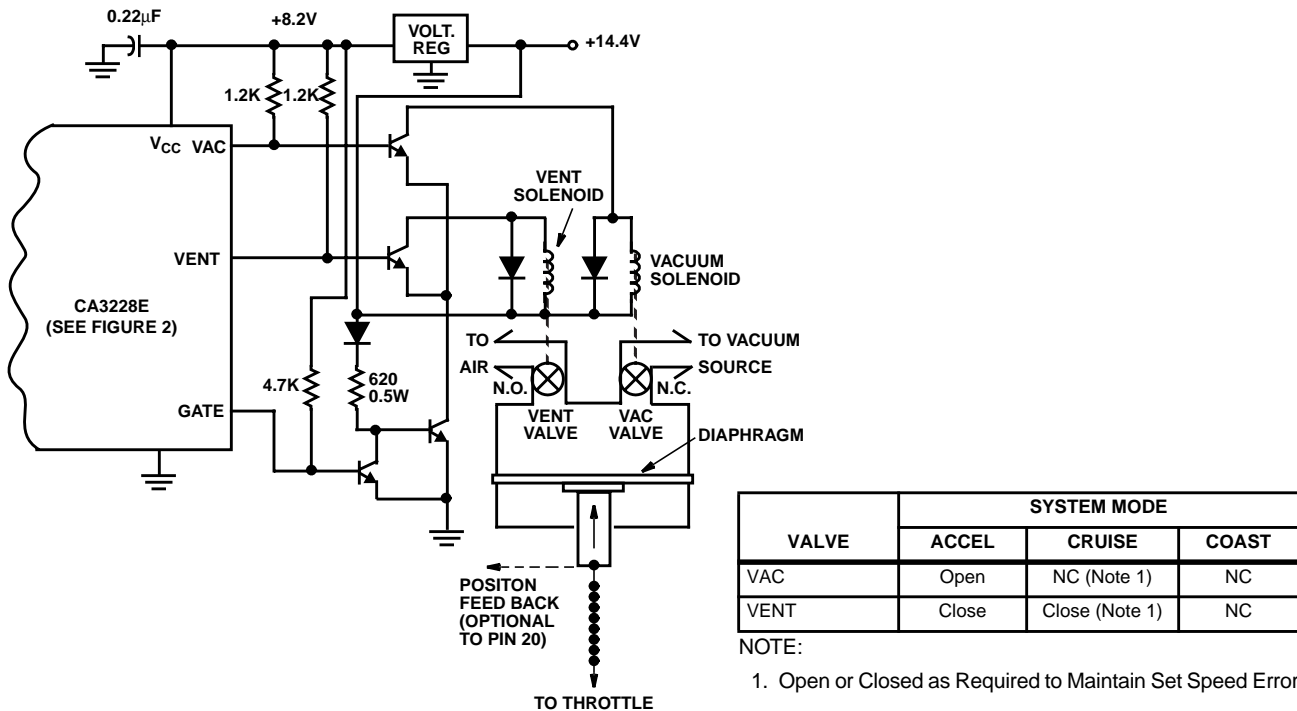


FIGURE 3. SOLENOID DRIVERS AND SERVO VACUUM CONTROL MECHANISM TYPICAL APPLICATION

|               | ACCEL | CRUISE | COAST | BRAKE | REDUNDANT BRAKE | HI-SPEED DROPOUT | LO-SPEED DROPOUT |
|---------------|-------|--------|-------|-------|-----------------|------------------|------------------|
| VAC (Pin 22)  | H     | L      | L     | L     | L               | L                | L                |
| VENT (Pin 21) | H     | H      | L     | L     | L               | L                | L                |
| GATE (pin 23) | L     | L      | L     | H     | H               | H                | H                |

## Device Description and Operation

The functional block diagram and Figures 1, 2 show the speed- control flow chart, and a typical automotive speed-control application, respectively.

### Command Decoder and Delay Logics (Pins 3,4)

Driver commands are input to pin 3 through the Driver Command Line. These signals are encoded on a single line as voltage levels selected by switches which adjust a resistor divider network.

The voltage level established is compared to a reference level which decodes the command. A command level greater than  $V_{CC} + 0.8V$  turns the system On, enabling dynamic control. Once the system is enabled, a voltage level of  $0.88V_{CC}$ ,  $0.66V_{CC}$ , and  $0.38V_{CC}$  decodes the RESUME, ACCEL, and COAST command, respectively. A driver command of  $0.12V_{CC}$  or less turns the system Off.

The Driver Command Delay established by the current sources and a capacitor at pin 4 assures that ON, OFF, ACCEL, and COAST commands are considered valid only if longer than 50ms. The time for RESUME is 330ms.

### Control Logic

The Control Logic accepts signals from the command decoder and other sensors. It causes the memory to be updated when operating in ACCEL and COAST modes. It will put the system in Standby mode if brakes are applied, if the speed error exceeds 11mph, or if the vehicle speed drops below the minimum Speed Lockout (25mph). It will return the vehicle to the previous set memory speed when a RESUME command is given.

### Frequency to Voltage Converter (Pins 8-11)

The speed sensor input  $f_S$  at pin 8 is an AC signal whose frequency is directly proportional to the vehicle speed at approximately 2.22Hz/mph. The current sources, capacitor and comparators at pin 9 cause equal rise and fall times to occur at pin 9 on the positive- and negative-going slopes of the sensor input. Pulse currents of time duration equal to the rise and fall times are used to charge the parallel resistor capacitor combination at pin 10 to give a voltage ( $V_S$ ) at pin 10 proportional to frequency at approximately 27mV/Hz. The  $f_S$  frequency range may be altered by changing the values of the filter capacitors at pins 8 and 9. However, the maximum-to-minimum frequency ratio will remain fixed.

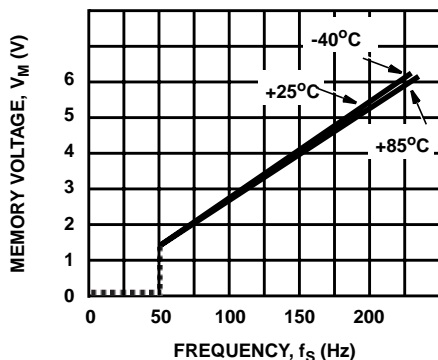


FIGURE 4. TYPICAL D/A MEMORY VOLTAGE,  $V_M$  vs

## FREQUENCY

### Memory Voltage, $V_M$ (Pin 6)

Upon release of the ACCEL or COAST switches the voltage, representing vehicle speed  $V_S$  determined by the output from the frequency-to-voltage converter, is stored as a binary number in a 9 bit counter. A memory update comparator allows clocking of the counter until memory voltage  $V_M$  equals  $V_S$ . The output of the counter controls a ladder network which provides memory voltage  $V_M$  at pin 6.

### Analog Accelerate and Resume Generator (Pins 14,15)

Numerous functions are combined in what is called the Analog Accelerate and Resume Generator. The circuit switches the signal output at pin 15 depending on the mode of operation. In the Accelerate and Resume mode the capacitor at pin 15 is charged at a fixed rate [ $450mV/(R_{EXT} \cdot C_{EXT})$ ]. In the Cruise mode pin 15 follows the memory voltage ( $V_M$ ) and in the On, Off, Brake, Redundant Brake, Minimum Speed Lockout, and Coast modes, pin 15 follows the voltage representing vehicle speed ( $V_S$ ).

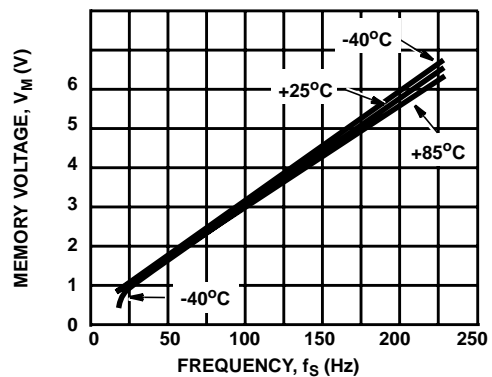


FIGURE 5. TYPICAL CHARACTERISTIC F/V CONVERTER OUTPUT,  $V_S$  vs FREQUENCY

### Error Amplifier (Pin 16)

In the Cruise mode the Error Amplifier determines the difference between the set memory speed ( $V_M$ ) and the actual speed ( $V_S$ ). This error signal is fed to the control amplifier where it defines whether VAC or VENT is required. The error signal represents deviation in vehicle speed from the memory or set speed condition. The Error signal is also used to control the Redundant Brake feature.

### Redundant Brake Comparator

When the error output drops below approximately  $0.42V_{CC}$ , the Redundant Brake output is activated. Redundant Brake causes the chip to go into the Standby mode.

### Control Amplifier (Pins 18, 20)

The Control Amplifier is an op amp using external components to set the gain. Inputs to the Control Amplifier are from the Error Amplifier output, servo position sensor and align output. The output of the Control Amplifier controls the VAC and VENT outputs.

### VAC, VENT and Gate-Driver Outputs (Pins 21, 22, 23)

The VAC, VENT and Gate Outputs are open collector devices used to control the throttle position. For the system

to be able to supply vacuum, the gate output must be low. If the output from the Control Amplifier exceeds  $0.573V_{CC}$ , vacuum is supplied to the servo unit. If the output of the Control Amplifier is between  $0.573V_{CC}$  and  $0.427V_{CC}$  the vacuum is held in the servo unit and vehicle speed is maintained. If the output from the Control Amplifier drops below  $0.427V_{CC}$  or if the gate output is high, the servo unit vacuum is vented.

#### **Overspeed Detector Comparator**

The Overspeed Detector circuit is used when the following sequence of events occur: A speed is set in memory, the vehicle is manually accelerated (foot pedal) to a higher speed and then the ACCEL switch is activated.

During vehicle acceleration  $V_S$  voltage is greater than the  $V_M$  voltage into the memory update comparator. When the ACCEL command is given, the capacitor at pin 15 rapidly charges to within 60mV of  $V_S$  before switching the comparator output low and starting the fixed acceleration rate from the present vehicle speed. The 60mV of offset is required to insure that the output of the overspeed detector is low under normal operating conditions. Hysteresis is also designed into the comparator to eliminate noise problems which may prevent the chip from going into the Acceleration mode.

#### **End of Resume Comparator**

The Resume Comparator is used when the following sequence of events occurs: A speed is set in memory, the brake applied, causing the vehicle to go to a lower speed, and the RESUME switch is activated.

Activation of the RESUME switch causes a fixed acceleration rate from the lower speed until the capacitor voltage at pin 15 is equal to the  $V_M$  voltage. A filter circuit contained in the output of the resume comparator insures that noise doesn't reset the comparator until  $V_{PIN}$  actually equals  $V_M$ .

#### **Align Voltage Source (Pin 17)**

The Align Voltage Source is a X1 buffer with an output of  $0.5V_{CC}$ .

#### **Brake Input Comparator (Pin 12)**

When the Brake Input exceeds  $0.55V_{CC}$ , the chip will go into the Standby mode from Cruise.

#### **Minimum Speed Lockout**

Assures that the system remains in a Standby mode if vehicle speed  $V_S$  is below  $0.183V_{CC}$ . It causes the system to revert to the Standby mode if  $V_S$  drops below  $0.183V_{CC}$  in the Cruise mode.

#### **Digital Filter for Redundant Brake and Minimum Speed Lockout**

A 4 bit shift register with an all '1's output decode is used to filter transients and electromagnetic interference. The filter prevents false signals from putting the system into Standby from Cruise.

#### **Ramp Oscillator (Pin 5)**

The Ramp Oscillator at pin 5 nominally varies between amplitudes of 4.1V and 6.1V. The discharge rate is approximately 4X the charge rate. With a capacitor of  $0.001\mu\text{F}$  on pin 5, the nominal oscillator frequency is 50kHz.

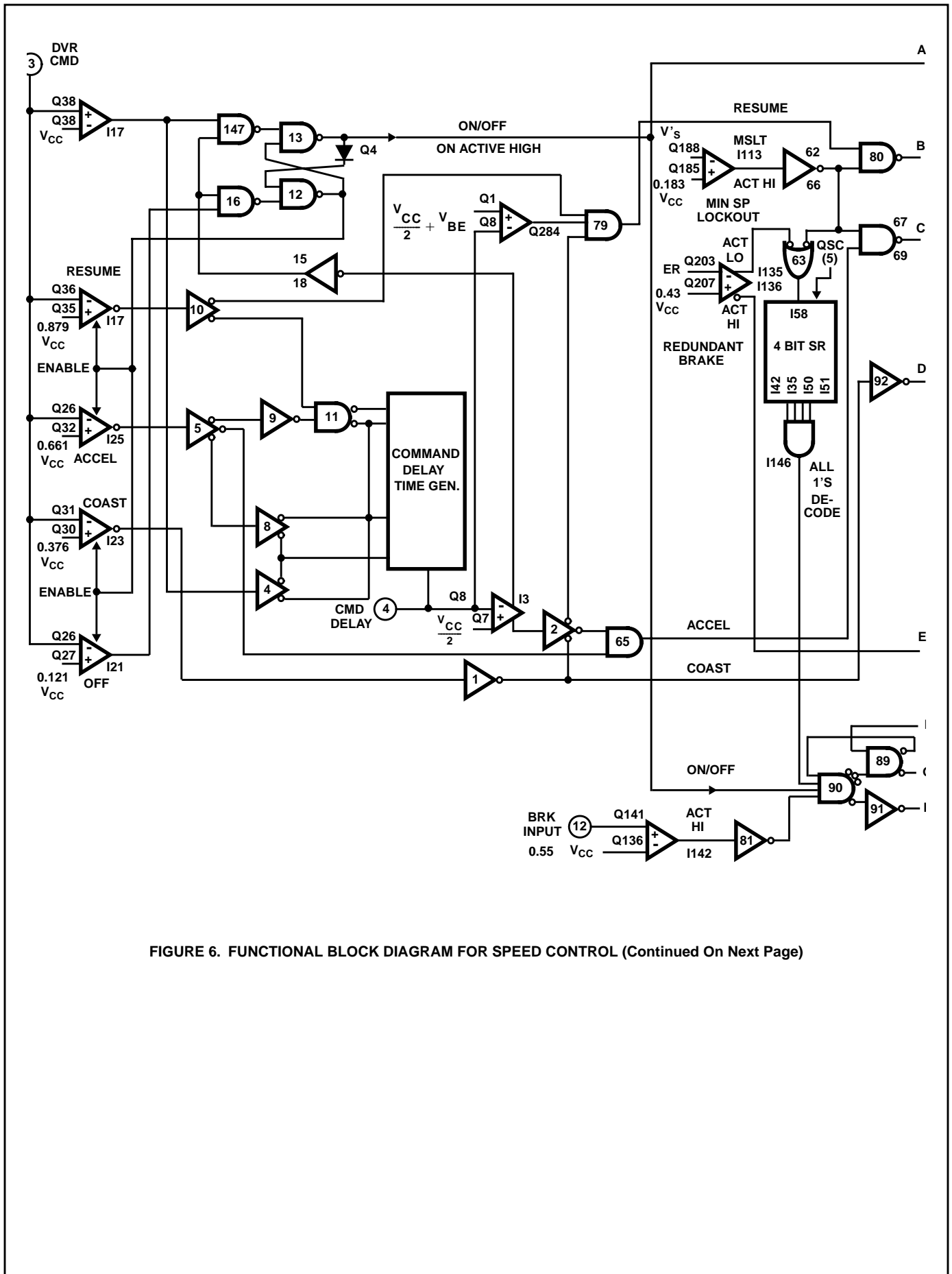


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued On Next Page)



CA3228

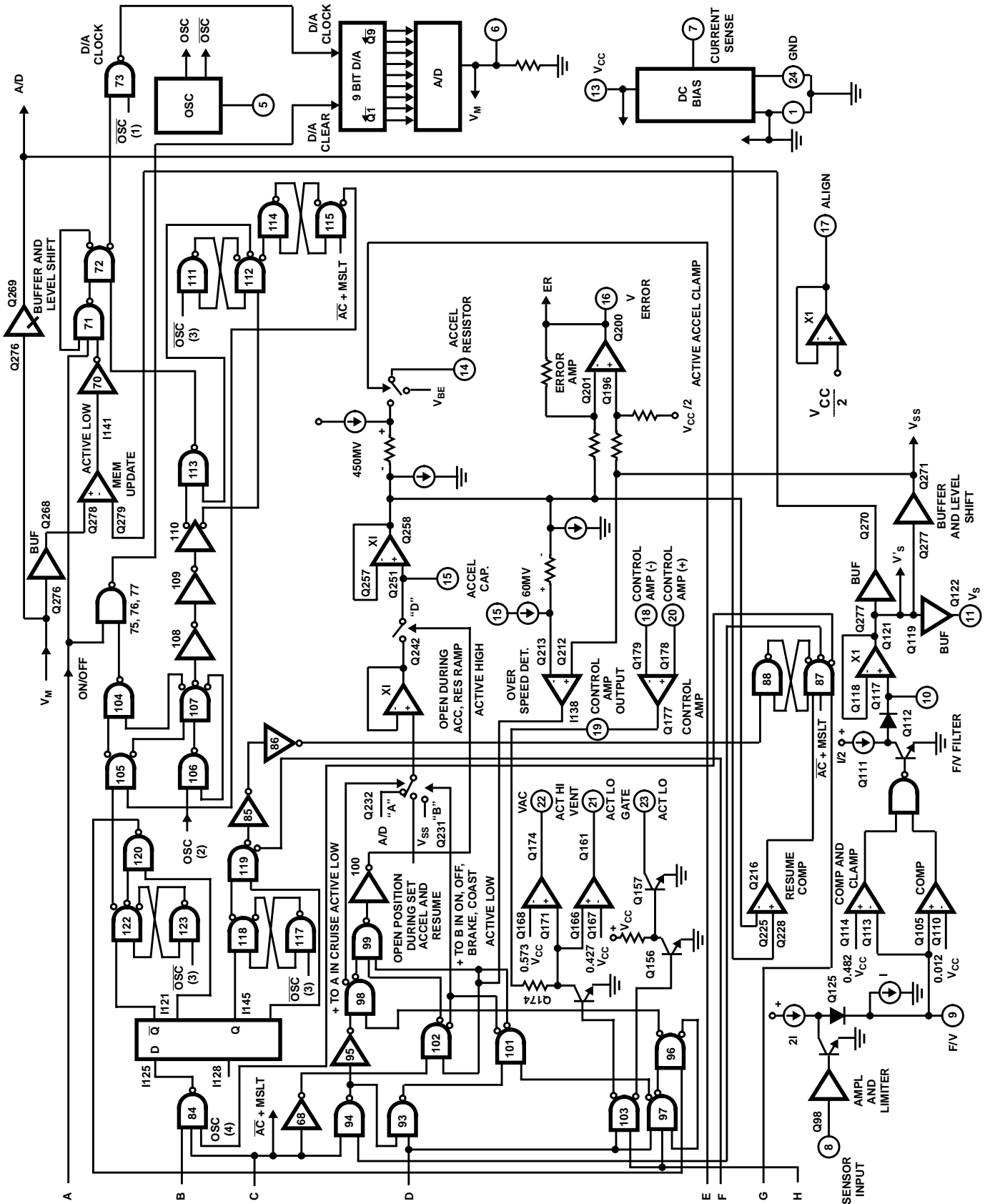


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued)