May 2001 File Number 3095.3

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

The Intersil CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Part Number Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3310E	±0.75 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310M	±0.75 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310AM	±0.5 LSB	-40 to 85	24 Ld SOIC	M24.3

Features

- CMOS Low Power (Typ) 15mW
- Single Supply Voltage . . . . . 3V to 6V
- Conversion Time 13µs
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Three-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

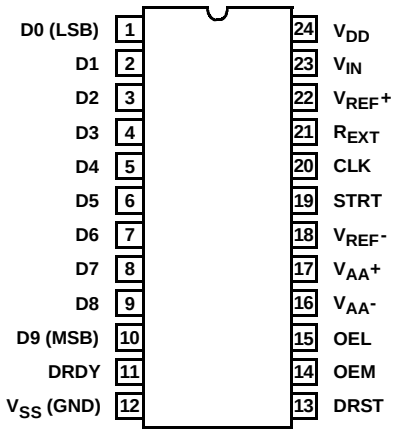
- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- µP Controlled Systems

Related Literature

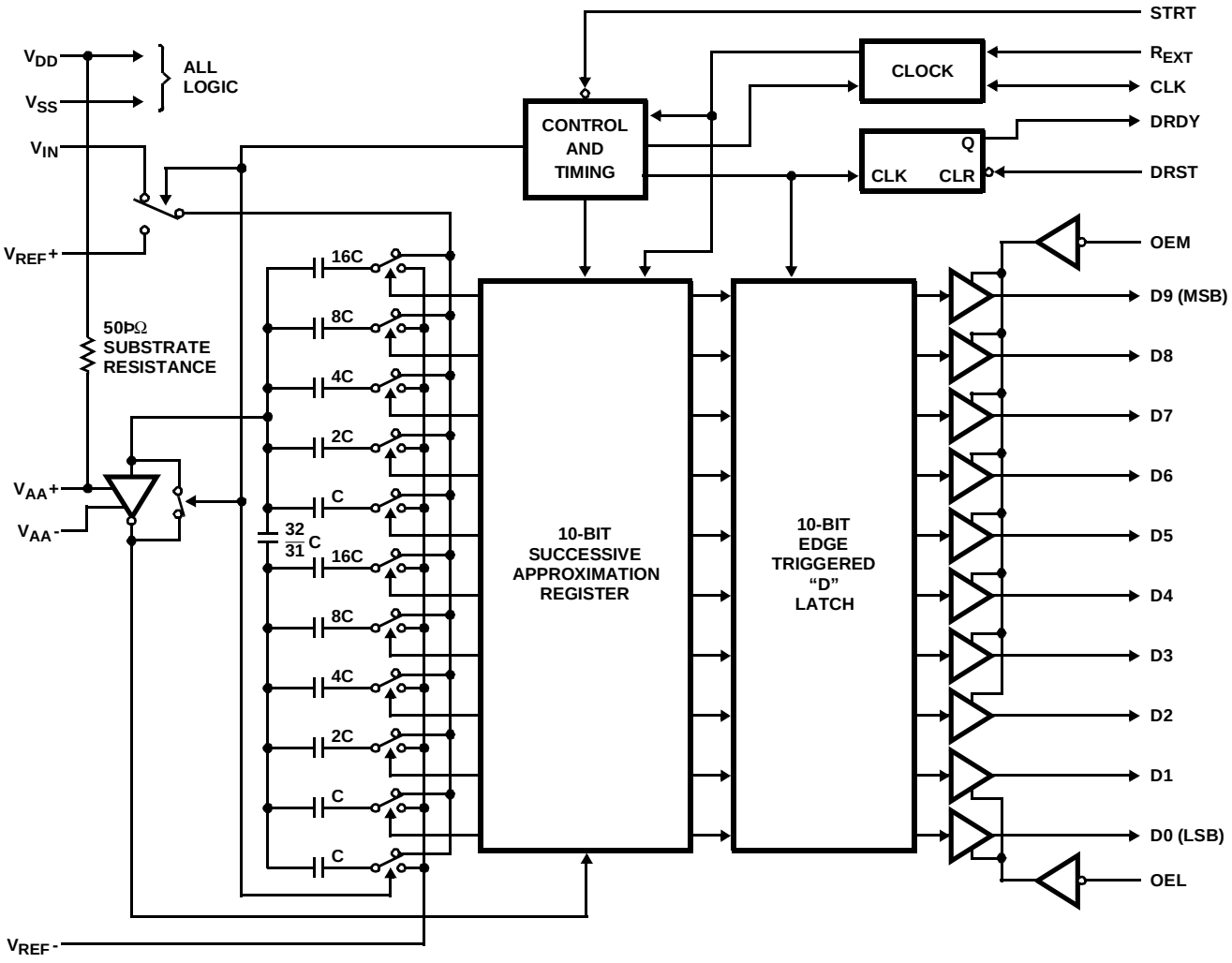
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

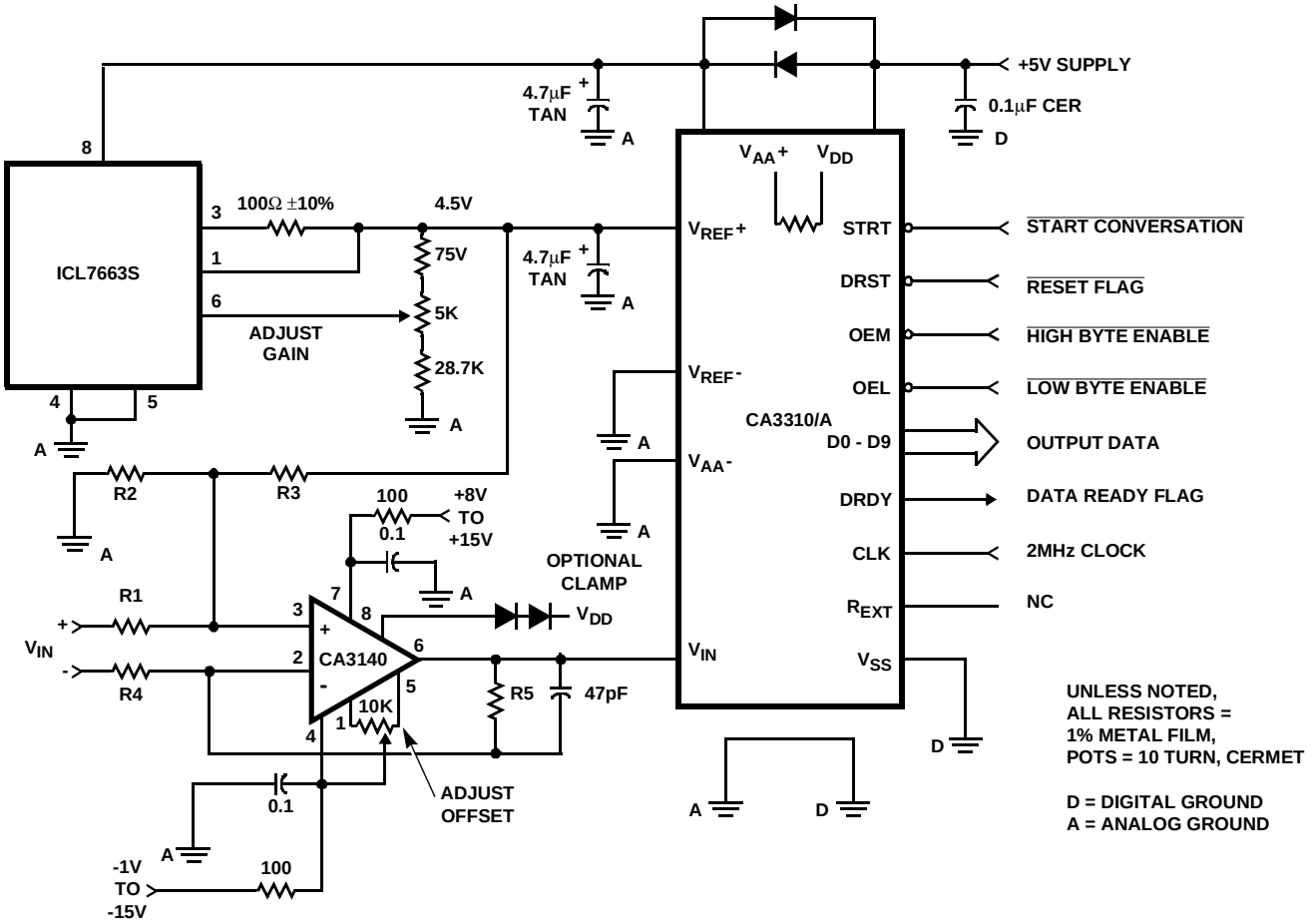
CA3310, CA3310A
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Typical Application Schematics



INPUT RANGE	R1	R2	R3	R4	R5
0V To 2.5V	4.99K	9.09K	OPEN	4.99K	9.09K
0V To 5V	4.99K	4.53K	OPEN	4.99K	4.53K
0V To 10V	10K	4.53K	OPEN	10K	4.53K
-2.5V To +2.5V	4.99K	9.09K	9.09K	4.99K	4.53K
-5V To +5V	10K	9.09K	9.09K	10K	4.53K

Absolute Maximum Ratings

Digital Supply Voltage V_{DD} . . . . . V_{SS} -0.5V to V_{SS} +7V
Analog Supply Voltage (V_{AA}+) . . . . . V_{DD} ±0.5V
Any Other Terminal . . . . . V_{SS} -0.5V to V_{DD} + 0.5V
DC Input Current or Output (Protection Diode) Current . . . . . ±20mA
DC Output Drain Current, per Output . . . . . ±35mA
Total DC Supply or Ground Current. . . . . ±70mA

Operating Conditions

Temperature Range (T_A) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	60
SOIC Package	75

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Maximum Storage Temperature (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

T_A = 25×°C, V_{DD} = V_{AA}+ = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1MHz, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Text For Definitions)						
Resolution			10	-	-	Bits
Differential Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Integral Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Gain Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
Offset Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
ANALOG INPUT						
Input Resistance		In Series with Input Sample Capacitors	-	330	-	Ω
Input Capacitance		During Sample State	-	300	-	pF
Input Capacitance		During Hold State	-	20	-	pF
Input Current		At V_{IN} = V_{REF}+ = 5V	-	-	+300	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-100	µA
Static Input Current		STRT = V+, CLK = V+ At V_{IN} = V_{REF}+ = 5V	-	-	1	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-1	µA
Input + Full-Scale Range		(Note 3)	V_{REF}- +1	-	V_{DD} +0.3	V
Input - Full-Scale Range		(Note 3)	V_{SS} -0.3	-	V_{REF}+ -1	V
Input Bandwidth		From Input RC Time Constant	-	1.5	-	MHz
DIGITAL INPUTS DRST, OEL, OEM, STRT, CLK						
High-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 3)	70	-	-	% of V_{DD}
Low-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 3)	-	-	30	% of V_{DD}
Input Leakage Current		Except CLK	-	-	±1	µA
Input Capacitance		(Note 3)	-	-	10	pF
Input Current		CLK Only (Note 3)	-	-	±400	µA
DIGITAL OUTPUTS D0 - D9, DRDY						
High-Level Output Voltage		I_{SOURCE} = -4mA	4.6	-	-	V
Low-Level Output Voltage		I_{SINK} = 6mA	-	-	0.4	V
Three-State Leakage		Except DRDY	-	-	±1	µA
Output Capacitance		Except DRDY (Note 3)	-	-	20	pF

Electrical Specifications $T_A = 25^{\times o}C$, $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = 4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 1MHz, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
CLK OUTPUT						
High-Level Output Voltage	I_{SOURCE} = 100µA (Note 3)		4	-	-	V
Low-Level Output Voltage	I_{SINK} = 100µA (Note 3)		-	-	1	V
TIMING						
Clock Frequency	Internal, CLK and R_{EXT} Open		200	300	400	kHz
	Internal, CLK Shorted to R_{EXT}		600	800	1000	kHz
	External, Applied to CLK (Note 3)	(Max)	-	4	2	MHz
		(Min)	100	10	-	kHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External, Applied to CLK: See Figure 1 (Note 3)		100	-	-	ns
Conversion Time	Internal, CLK Shorted to R_{EXT}		13	-	-	µs
Aperture Delay, t_D APR	See Figure 1		-	100	-	ns
Clock to Data Ready Delay, t_{D1} DRDY	See Figure 1		-	150	-	ns
Clock to Data Ready Delay, t_{D2} DRDY	See Figure 1		-	250	-	ns
Clock to Data Delay, t_D Data	See Figure 1		-	200	-	ns
Start Removal Time, t_R STRT	See Figures 3 and 4 (Note 2)		-	-120	-	ns
Start Setup Time, t_{SU} STRT	See Figure 4		-	160	-	ns
Start Pulse Width, t_W STRT	See Figures 3 and 4		-	10	-	ns
Start to Data Ready Delay, t_{D3} DRDY	See Figures 3 and 4		-	170	-	ns
Clock Delay from Start, t_D CLK	See Figure 3		-	200	-	ns
Ready Reset Removal Time, t_R DRST	See Figure 5 (Note 2)		-	-80	-	ns
Ready Reset Pulse Width, t_W DRST	See Figure 5		-	10	-	ns
Ready Reset to Data Ready Delay, t_{D4} DRDY	See Figure 5		-	35	-	ns
Output Enable Delay, t_{EN}	See Figure 2		-	40	-	ns
Output Disable Delay, t_{DIS}	See Figure 2		-	50	-	ns
SUPPLIES						
Supply Operating Range, V_{DD} or V_{AA}	(Note 3)		3	-	6	V
Supply Current, $I_{DD} + I_{AA}$	See Figures 14, 15		-	3	8	mA
Supply Standby Current	Clock Stopped During Cycle 1		-	3.5	-	mA
Analog Supply Rejection	At 120Hz, See Figure 13		-	25	-	mV/V
Reference Input Current	See Figure 10		-	160	-	µA
TEMPERATURE DEPENDENCY						
Offset Drift	At 0 to 1 Code Transition		-	-4	-	$\mu V/^oC$
Gain Drift	At 1022 to 1023 Code Transition		-	-6	-	$\mu V/^oC$
Internal Clock Speed	See Figure 7		-	-0.5	-	$\%/^oC$

NOTES:

2. A (-) removal time means the signal can be removed after the reference signal.
3. Parameter not tested, but guaranteed by design or characterization.

Timing Diagrams

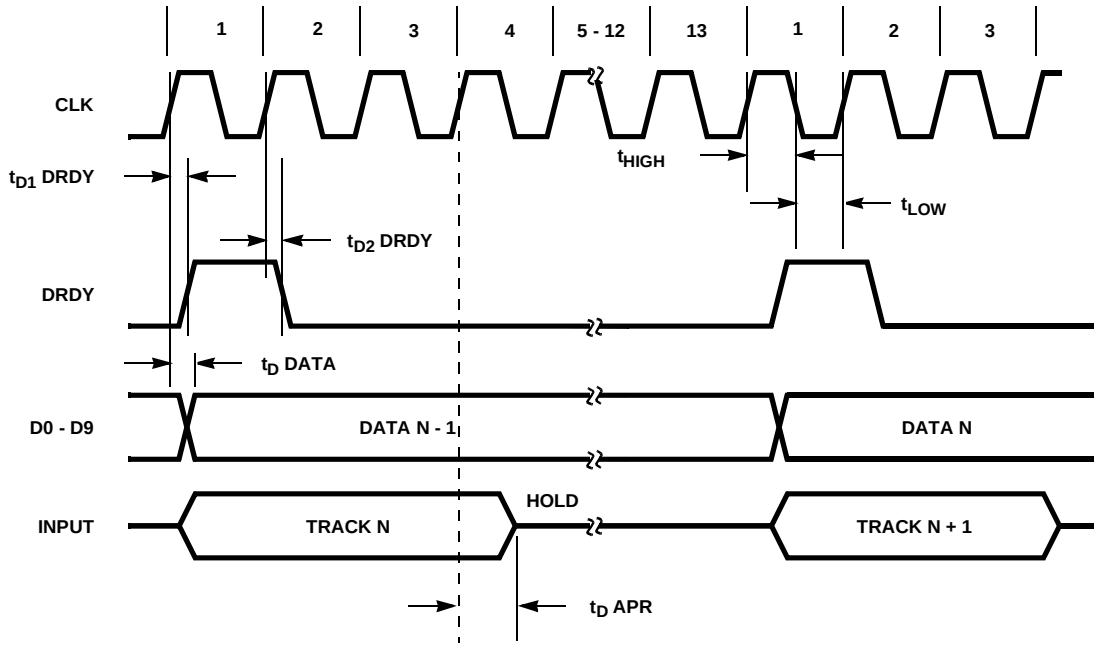


FIGURE 1. FREE RUNNING, STRT TIED LOW, DRST TIED HIGH

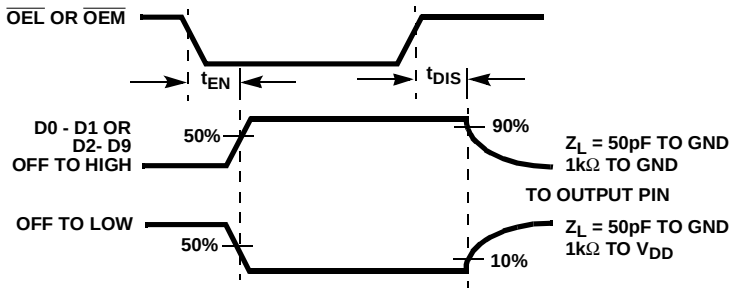


FIGURE 2. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

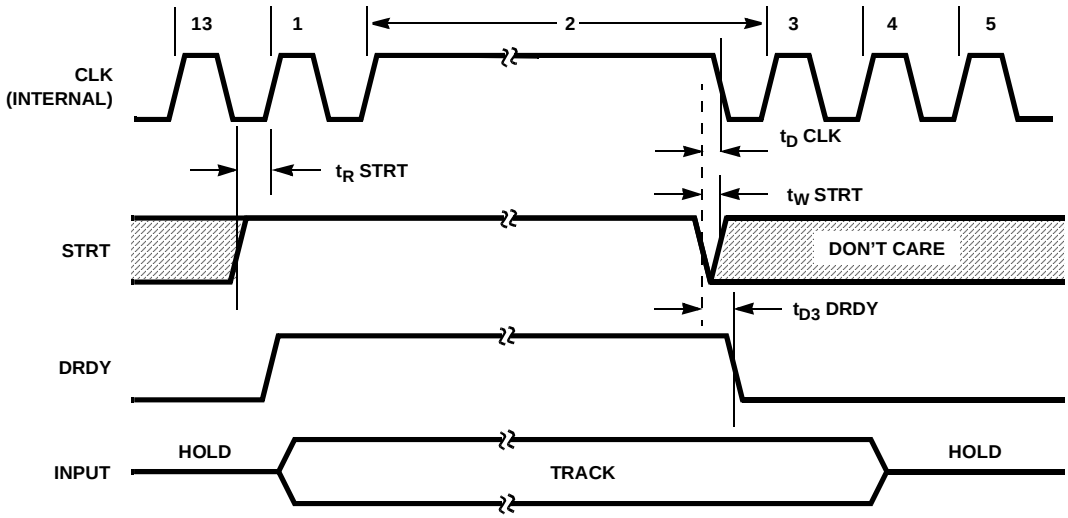


FIGURE 3. STRT PULSED LOW, DRST TIED HIGH, INTERNAL CLOCK

Timing Diagrams (Continued)

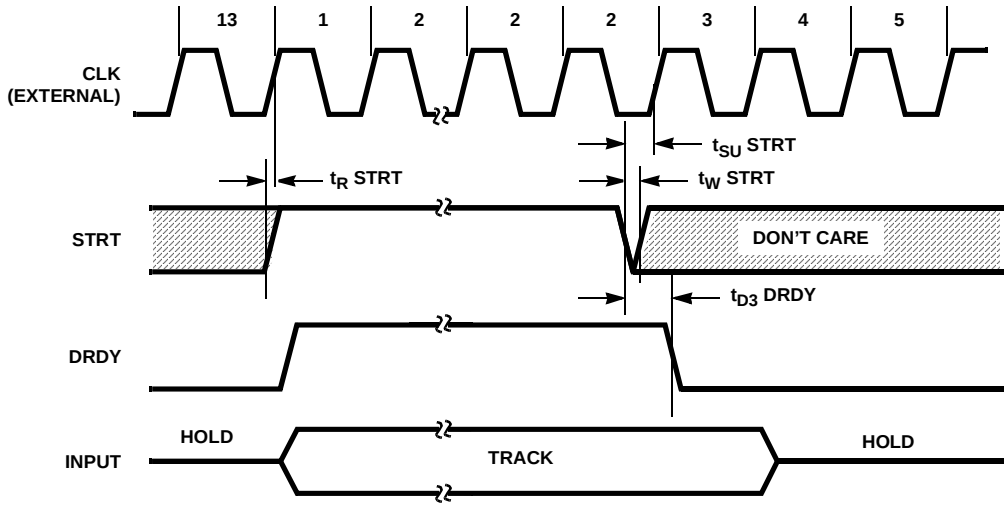


FIGURE 4. STRT PULSED LOW, DRST TIED HIGH, EXTERNAL CLOCK

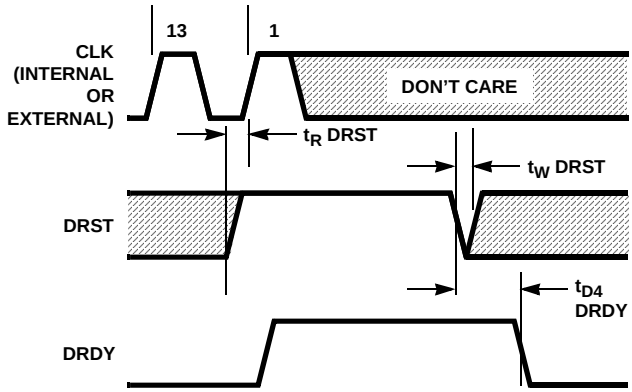


FIGURE 5. DRST PULSED LOW, STRT TIED HIGH

Typical Performances Curves

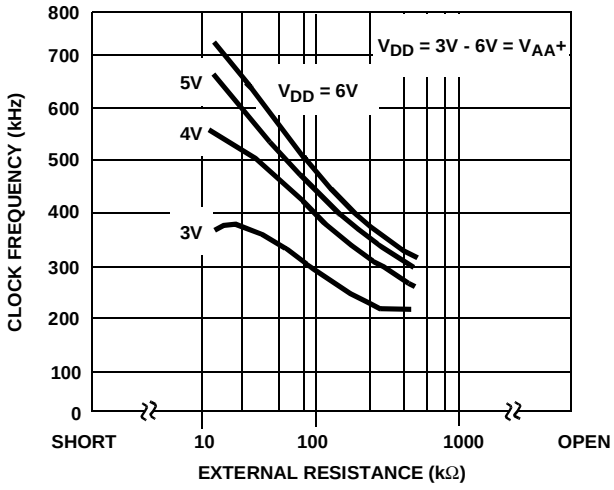


FIGURE 6. INTERNAL CLOCK FREQUENCY vs EXTERNAL RESISTANCE

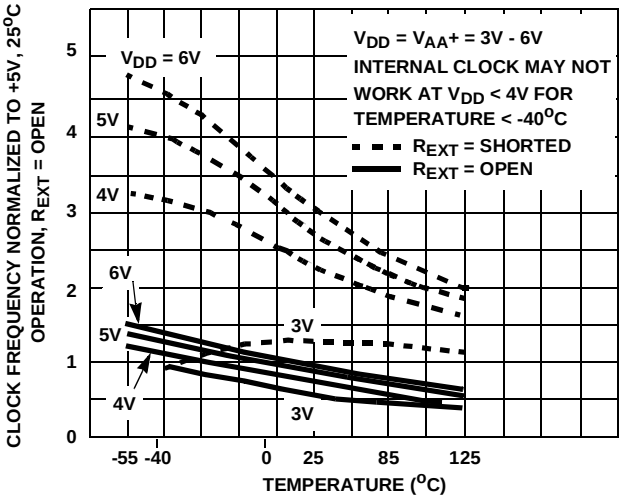


FIGURE 7. INTERNAL CLOCK FREQUENCY vs TEMPERATURE AND SUPPLY VOLTAGE

Typical Performances Curves (Continued)

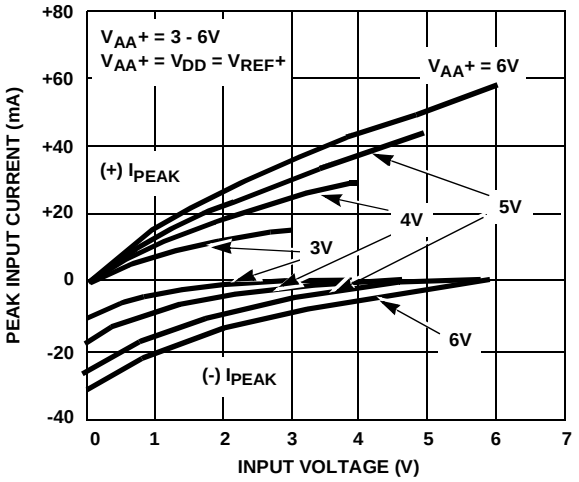


FIGURE 8. PEAK INPUT CURRENT vs INPUT VOLTAGE

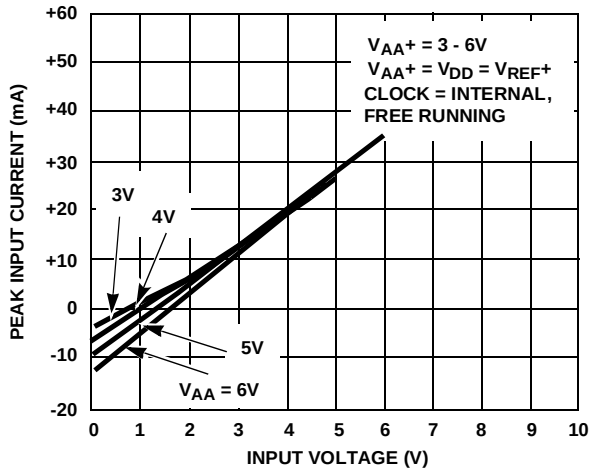


FIGURE 9. AVERAGE INPUT CURRENT vs INPUT VOLTAGE

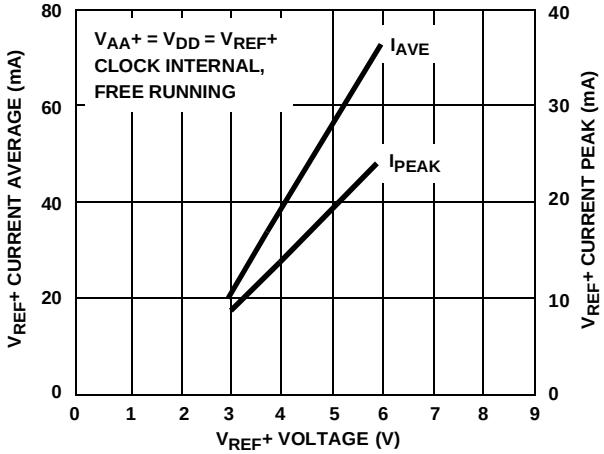


FIGURE 10. V_{REF}+ CURRENT vs V_{REF}+ VOLTAGE

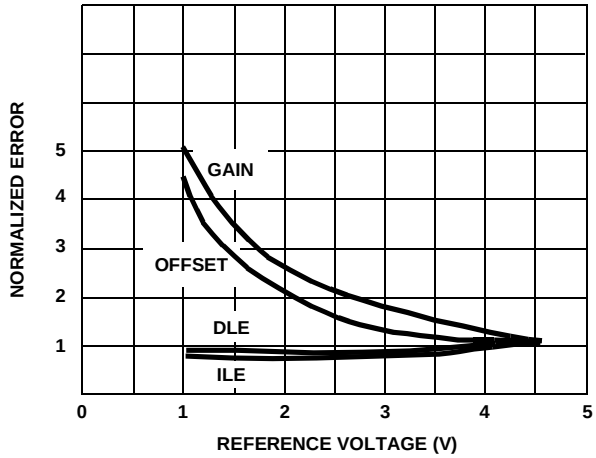


FIGURE 11. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs REFERENCE VOLTAGE

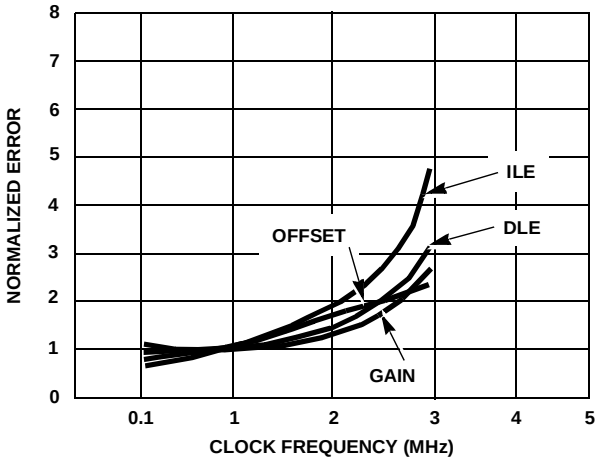


FIGURE 12. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs CLOCK SPEED

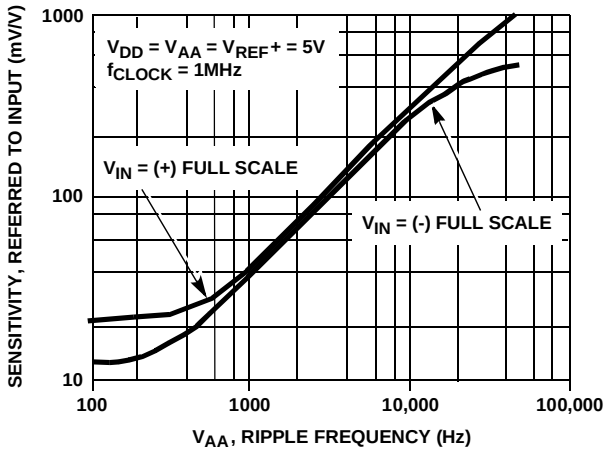


FIGURE 13. V_{AA} SUPPLY SENSITIVITY

Typical Performances Curves (Continued)

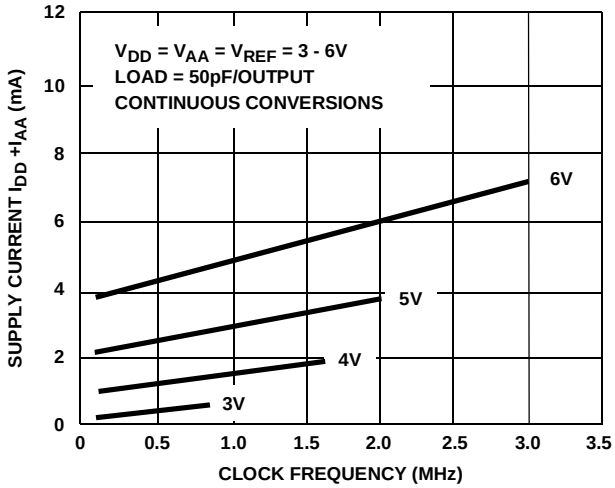


FIGURE 14. SUPPLY CURRENT vs CLOCK FREQUENCY

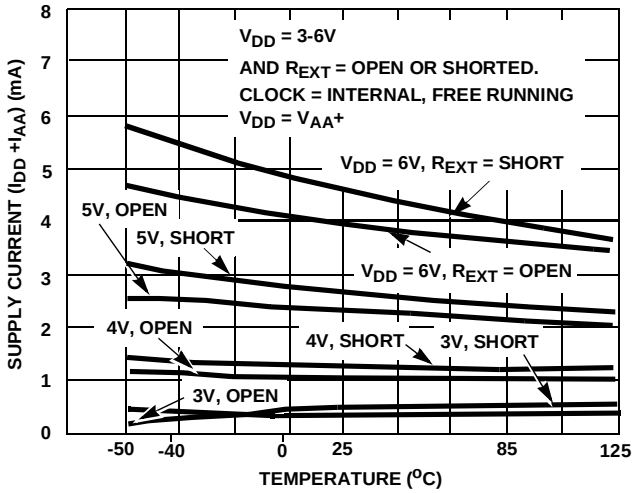


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

TABLE 1. PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION
1-10	D0 - D9	Three-State outputs for data bits representing 2^0 (LSB) through 2^9 (MSB).
11	DRDY	Output flag signifying new data is available. Goes high at end of clock period 13, goes low when new conversion started. Also reset asynchronously by DRST.
12	V_{SS}	Digital Ground.
13	DRST	Active low input, resets DRDY.
14	OEM	Active low input, three-state enable of D2 - D9.
15	OEL	Active low input, three-state enable of D0, D1.
16	V_{AA}-	Analog Ground.
17	V_{AA}+	Analog + Supply.
18	V_{REF}-	Reference input voltage, sets 0 code (-) end of input range.
19	STRT	Active Low Start Conversion Input. Recognized after end of clock period 13.
20	CLK	Clock input or output. Conversion functions are synchronous to high-going edge.
21	R_{EXT}	Clock adjust input when using internal clock.
22	V_{REF}+	Reference input voltage, set 1023 code (+) end of input range.
23	V_{IN}	Analog Input.
24	V_{DD}	Digital + Supply.

TABLE 2. OUTPUT CODES

CODE DESCRIPTION $LSB = \frac{(V_{REF+} - V_{REF-})}{1024}$	INPUT VOLTAGE (NOTE 4) $(V_{REF+} - V_{REF-}) = 4.608V$ (V)	BINARY OUTPUT CODE MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	DECIMAL COUNT
Zero	0.000	0	0	0	0	0	0	0	0	0	0	0
1 LSB	0.0045	0	0	0	0	0	0	0	0	0	1	1
$^1/_4$ (V_{REF}+ - V_{REF}-)	1.152	0	1	0	0	0	0	0	0	0	0	256
$^1/_2$ (V_{REF}+ - V_{REF}-)	2.304	1	0	0	0	0	0	0	0	0	0	512
$^3/_4$ (V_{REF}+ - V_{REF}-)	3.456	1	1	0	0	0	0	0	0	0	0	768
(V_{REF}+ - V_{REF}-) - 1 LSB	4.6035	1	1	1	1	1	1	1	1	1	1	1023

NOTE:

4. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Device Operation

The CA3310 is a CMOS 10-bit, analog-to-digital converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the D-to-A "Heart" of the device. See the Functional Diagram of the CA3310.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF}+$ or $V_{REF}-$.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input. The comparator is being auto-balanced at its trip point, thus setting the voltage at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input, the one representing the MSB (D9) is connected to the $V_{REF}+$ terminal, and the remaining capacitors to $V_{REF}-$. The capacitor-common node, after the charges balance out, will represent whether the input was above or below $^1/_2$ of ($V_{REF}+ - V_{REF}-$).

At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF}+$ (if the comparator was high) or returned to $V_{REF}-$. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of ($V_{REF}+ - V_{REF}-$).

At the end of periods 5 through 12, capacitors representing the next to MSB (D8) through the next to LSB (D1) are tested, the result stored, and each capacitor either left at $V_{REF}+$ or at $V_{REF}-$.

At the end of the 13th period, when the LSB (D0) capacitor is tested, D0 and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Clock

The CA3310 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronous with the rising edge of the clock signal.

Figure 16 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and wiring capacitance should be kept to a minimum.

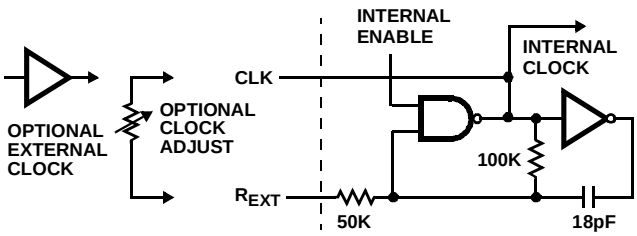


FIGURE 16. CLOCK CIRCUITRY

The R_{EXT} pin allows adjusting of the internal clock frequency by connecting a resistor between R_{EXT} and CLK. Figure 6 shows the typical relationship between the resistor and clock speed, while Figure 7 shows clock speed versus temperature and supply voltage.

The internal clock will shut down if the A/D is not restarted after a conversion. This is described under Control Timing. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold: this is described further under Applications.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 13) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Control Signals

The CA3310 may be synchronized from an external source by using the STRT (Start Conversion) input to initiate conversions, or if STRT is tied low, may be allowed to free-run. In the free-running mode, illustrated in Figure 1, each conversion takes 13 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1} DRDY) after the start of clock period 1, and returns low (specified by t_{D2} DRDY) after the start of clock period 2. DRDY may also be asynchronously reset by a low on DRST (to be discussed later).

If the output data is to be latched externally by the DRDY signal, the trailing edge of DRDY should be used: there is no guaranteed set-up time to the leading edge.

The 10 output data bits are available in parallel on three- state bus driver outputs. When low, the OEM input enables the most significant byte (D2 through D9) while the OEL input enables the two least significant bits (D0, D1). t_{EN} and t_{DIS} specify the output enable and disable times, respectively. See Figure 2.

When the STRT input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the STRT signal is removed (at least t_R STRT) before clock

period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track the DRDY output will remain high during this time.

A low signal applied to STRT (at least t_W STRT wide) can now initiate a new conversion. The STRT signal (after a delay of t_{D3} DRDY) will cause the DRDY flag to drop, and (after a delay of t_D CLK) cause the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free-running.

Figure 4 illustrates the same operation as above, but with an external clock. If STRT is removed (at least t_R STRT) before clock period 1, and not reapplied during that period, the clock will continue to cycle in period 2. A low signal applied to STRT will drop the DRDY flag as before, and with the first positive-going clock edge that meets the t_{SU} STRT set-up time, the converter will continue with clock period 3.

The DRDY flag output, as described previously, goes active at the start of period 1, and drops at the start of period 2 or upon a new STRT command, whichever is later. It may also be controlled with the DRST (Data Ready Reset) input. Figure 5 depicts this operation.

DRST must be removed (at least t_R DRST) before the start of period 1 to allow DRDY to go high. A low level on DRST (at least t_W DRST wide) will (after a delay of t_{D4} DRDY) drop DRDY.

Analog Input

The analog input pin is a predominantly capacitive load that changes between the track and hold periods of a conversion cycle. During hold, clock period 4 through 13, the input loading is leakage and stray capacitance, typically less than 0.1µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the charge by the end of the tracking period. The amount of charge is dependent on supply and input voltages. Figure 8 shows typical peak input currents for various supply and input voltages, while Figure 9 shows typical average input currents. The average current is also proportional to clock frequency, and should be scaled accordingly.

During tracking, the input appears as approximately a 300pF capacitor in series with 330Ω, for a 100ns time constant. A full-scale input swing would settle to $^1/_2$ LSB ($^1/_{2048}$) in 7RC time constants. Doing continuous conversions with a 1MHz clock provides 3µs of tracking time, so up to 1kΩ of external source impedance (400ns time constant) would allow proper settling of a step input.

If the clock was slower, or the converter was not restarted immediately (causing a longer sample lime), a higher source impedance could be used.

The CA3310s low-input time constant also allows good tracking of dynamic input waveforms. The sampling rate with a 1MHz clock is approximately 80kHz. A Nyquist rate ($f_{SAMPLE}/2$) input sine wave of 40kHz would have negligible attenuation and a phase lag of only 1.5 degrees.

Accuracy Specifications

The CA3310 accepts an analog input between the values of V_{REF}- and V_{REF}+, and quantizes it into one of 2^{10} or 1024 output codes. Each code should exist as the input is varied through a range of $^1/_{1024}$ x (V_{REF}+ - V_{REF}-), referred to as 1 LSB of input voltage. A differential linearity error, illustrated in Figure 17, occurs if an output code occurs over other than the ideal (1 LSB) input range. Note that as long as the error does not reach -1 LSB, the converter will not miss any codes.

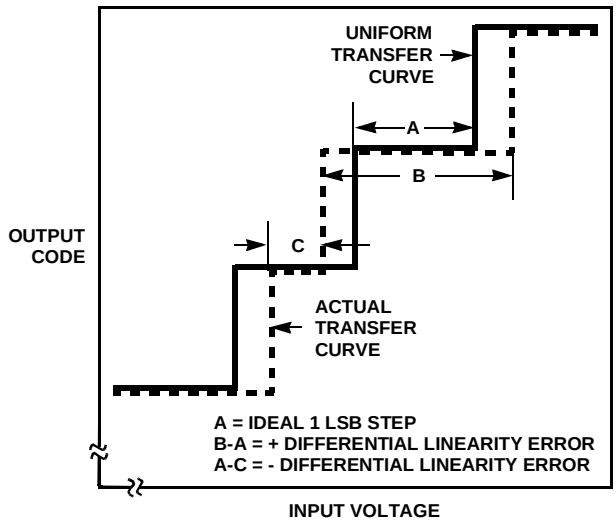


FIGURE 17. DIFFERENTIAL LINEARITY ERROR

The CA3310 output should change from a code of 000_{16} to 001_{16} at an input voltage of (V_{REF}- +1 LSB). It should also change from a code of $3FE_{16}$ to $3FF_{16}$ at an input of (V_{REF}+ -1 LSB). Any differences between the actual and expected input voltages that cause these transitions are the offset and gain errors, respectively. Figure 18 illustrates these errors.

As the input voltage is increased linearly from the point that causes the 00016 to 00116 transition to the point that causes the $3FE_{16}$ to $3FF_{16}$ transition, the output code should also increase linearly. Any deviation from this input-to-output correspondence is integral linearity error, illustrated in Figure 19.

Note that the integral linearity is referenced to a straight line drawn through the actual end points, not the ideal end points. For absolute accuracy to be equal to the integral linearity, the gain and offset would have to be adjusted to ideal.

Offset and Gain Adjustments

The V_{REF}+ and V_{REF}- pins, references for the two ends of the analog input range, are the only means of doing offset or

gain adjustments. In a typical system, the V_{REF}- might be returned to a clean ground, and offset adjustment done on an input amplifier. V_{REF}+ would then be adjusted for gain.

V_{REF}- could be raised from ground to adjust offset or to accommodate an input source that can't drive down to ground.

There are current pulses that occur, however, during the successive approximation part of a conversion cycle, as the charge-balancing capacitors are switched between V_{REF}- and V_{REF}+. For that reason, V_{REF}- and V_{REF}+ should be well bypassed. Figure 10 shows peak and average V_{REF}+ current.

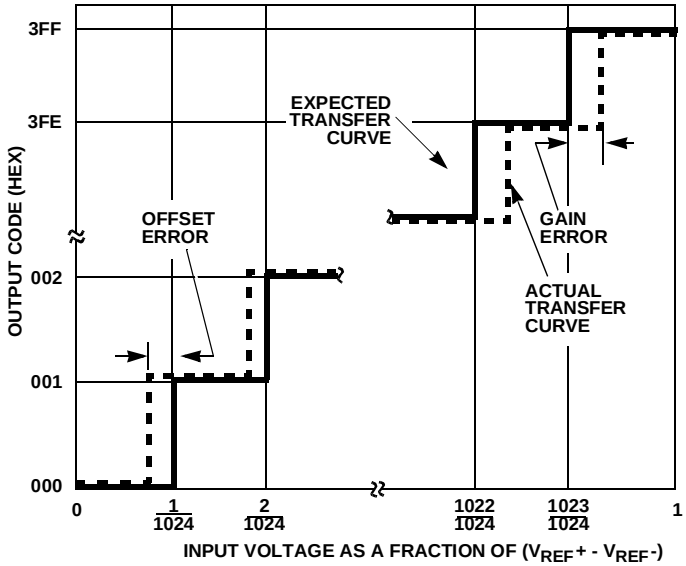


FIGURE 18. GAIN AND OFFSET ERROR

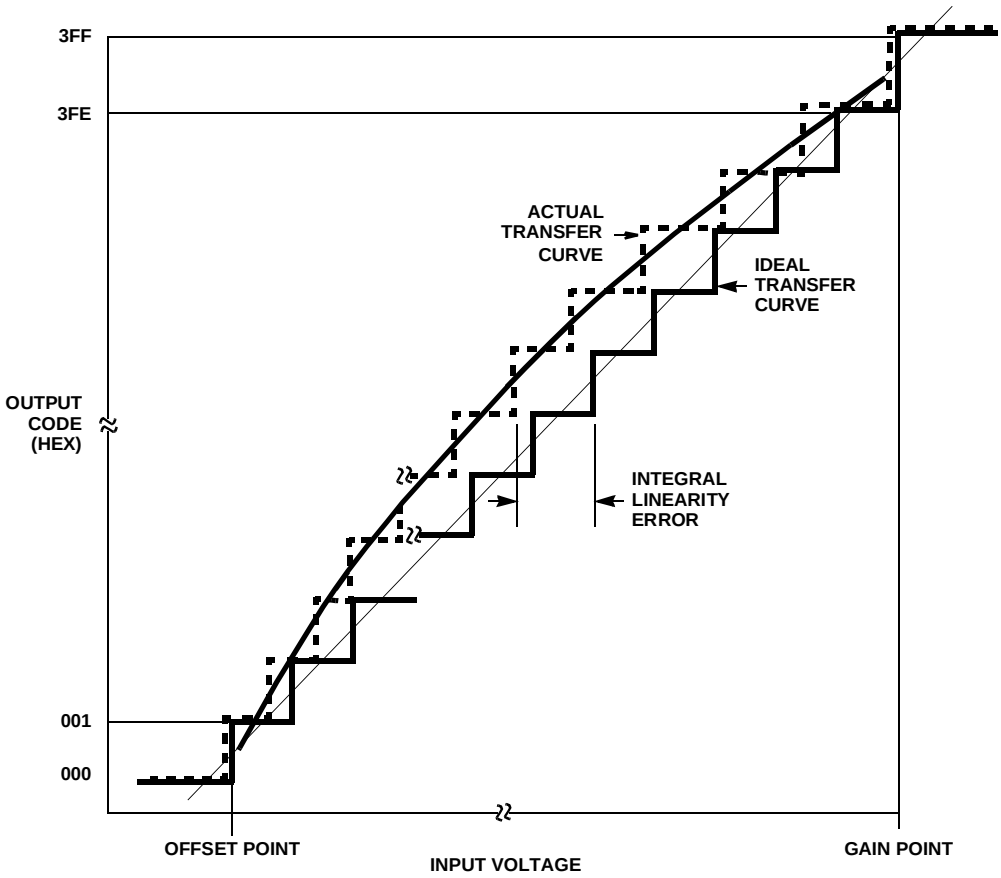


FIGURE 19. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs REFERENCE VOLTAGE

Other Accuracy Effects

Linearity, offset, and gain errors are dependent on the magnitude of the full-scale input range, $V_{REF}+ - V_{REF}-$. Figure 11 shows how these errors vary with full-scale range.

The clocking speed is a second factor that affects conversion accuracy. Figure 12 shows the typical variation of linearity, offset, and gain errors versus clocking speed.

Gain and offset drift due to temperature are kept very low by means of auto-balancing the comparator. The specifications show typical offset and gain dependency on temperature.

There is also very little linearity change with temperature, only that caused by the slight slowing of CMOS with increasing temperature. At 85^oC, for instance, the lLE and DLE would be typically those for a 20% faster clock than at 25^oC.

Power Supplies and Grounding

V_{DD}(+) and V_{SS}(GND) are the digital supply pins: they operate all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for $V_{DD}+$, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}: input transients above V_{DD} or below V_{SS} will get steered to the digital supplies. Current on these pins must be limited by external means to the values specified under maximum ratings.

The $V_{AA}+$ and $V_{AA}-$ terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies, however: $V_{AA}-$ should be returned to a clean analog ground, and $V_{AA}+$ should be RC decoupled from the digital supply.

There is approximately 50ÞΩ of substrate impedance between V_{DD} and $V_{AA}+$. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10pF capacitor from $V_{AA}+$ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to $V_{AA}+$ to handle supply to capacitor turn-on or turn-off current spikes.

Figure 16 shows $V_{AA}+$ supply rejection versus frequency. Note that the frequency to be rejected scales with the clock: the 100Hz rejection with a 100kHz clock would be roughly equivalent to the 1kHz rejection with a 1MHz clock.

The supply current for the CA3310 is dependent on clock frequency, supply voltage, and temperature. Figure 14 shows the typical current versus frequency and voltage, while Figure 15 shows it versus temperature and voltage. Note that if stopped in auto-balance, the supply current is typically somewhat higher than if free-running. See Specifications.

Application Circuits

Differential Input A/D System

As the CA3310 accepts a unipolar positive-analog input, the accommodation of other ranges requires additional circuitry. The input capacitance and the input energy also force using a low-impedance source for all but slow speed use. Figure 20 shows the CA3310 with a reference, input amplifier, and input-scaling resistors for several input ranges.

The ICL7663S regulator was chosen as the reference, as it can deliver less than 0.25V input-to-output (dropout) voltage and uses very little power. As high a reference as possible is generally desirable, resulting in the best linearity and rejection of noise at the CA3310.

The tantalum capacitor sources the V_{REF} current spikes during a conversion cycle. This relieves the response and peak current requirements of the reference.

The CA3140 operational amplifier provides good slewing capability for high bandwidth input signals and can quickly settle the energy that the CA3310 outputs at its V_{IN} terminal. It can also drive close to the negative supply rail.

If system supply sequencing or an unknown input voltage is likely to cause the operational amplifier to drive above the V_{DD} supply, a diode clamp can be added from pin 8 of the operational amplifier to the V_{DD} supply. The minus drive current is low enough not to require protection.

With a 2MHz clock (~150kHz sampling), Nyquist criteria would give a maximum input bandwidth of 75kHz. The resistor values chosen are low enough to not seriously degrade system bandwidth (an operational amplifier settling) at that clock frequency. If A/D clock frequency and bandwidth requirements are lower, the resistor values (and input impedance) can be made correspondingly higher.

The A/D system would generally be calibrated by tying $V_{IN}-$ to ground and applying a voltage to $V_{IN}+$ that is 0.5 LSB ($^1/_{2048}$ of full-scale range) above ground. The operational amplifier offset should be adjusted for an output code dithering between 000_{16} and 001_{16} for unipolar use, or 100_{16} and 101_{16} for bipolar use. The gain would then be adjusted by applying a voltage that is 1.5 LSB below the positive full scale input, and adjusting the reference for an output dithering between $3FE_{16}$ and $3FF_{16}$.

Note that R1 through R5 should be very well matched, as they affect the common-mode rejection of the A/D system. Also, if R2 and R3 are not matched, the offset adjust of the operational amplifier may not have enough adjustment range in bipolar systems.

The common-mode input range of the system is set by the supply voltage available to the operational amplifier. The range that can be applied to the $V_{IN}-$ terminal can be calculated by:

$\left(\frac{R4}{R5}+1\right)$ $V_{IN}-$ for the most negative,

$\left(\frac{R4}{R5}+1\right)$ $(V_{IN}+ -2.5V) - (\frac{R4}{R5})V_{REF}+$ for the most positive.

Single +5V Supply

If only a single +5V supply is available, an ICL7660 can be used to provide approximately +8V and -4V to the operational amplifier. Figure 20 shows this approach. Note that the converter and associated capacitors should be grounded to the digital supply. The 1kΩ in series with each supply at the operational amplifier isolates digital and analog grounds.

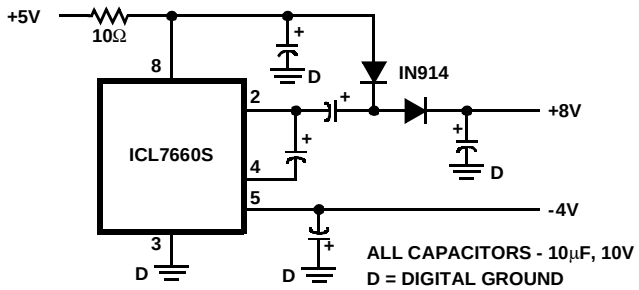


FIGURE 20. USING ICL7660 TO GENERATE SUPPLIES

Digital Sample and Hold

With a minimum of external logic, the CA3310 can be made to wait at the verge of ending a sample. A start pulse will then, after the internal aperture delay, capture the input and finish the conversion cycle. Figure 21 illustrates this application.

The CA3310 is connected as if to free run. The Data Ready signal is shifted through a CD74HC175, and at the low-going clock edge just before the sample would end, is used to hold the clock low.

The same signal, active high, is available to indicate the CA3310 is ready to convert. A low pulse to reset the CD74HC175 will now release the clock, and the sample will end as it goes positive. Ten cycles later, the conversion will be complete, and DRDY will go active.

Operating and Handling Considerations

Handling

All inputs and outputs of Intersil CMOS devices have a network for electrostatic protection during handling.

Operating

OPERATING VOLTAGE

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

INPUT SIGNALS

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} +0.3V nor less than V_{SS} -0.3V. Input currents must not exceed 20mA even when the power supply is off.

UNUSED INPUTS

A connection must be provided at every input terminal. All unused Input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

OUTPUT SHORT CIRCUITS

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

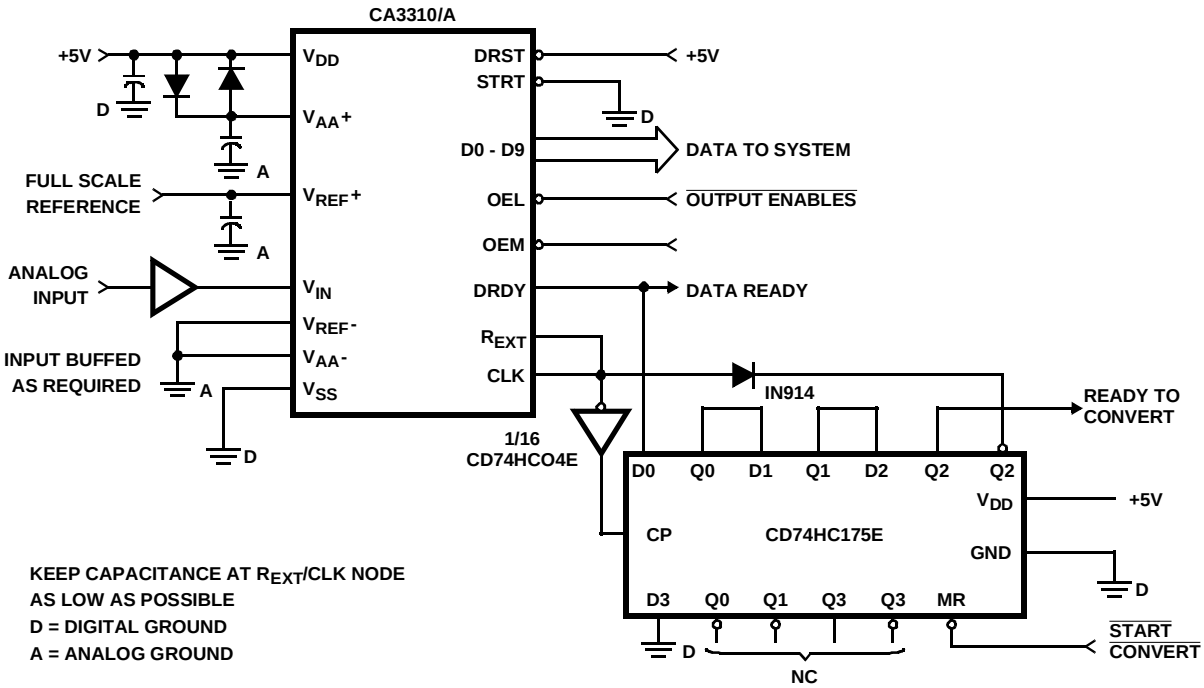
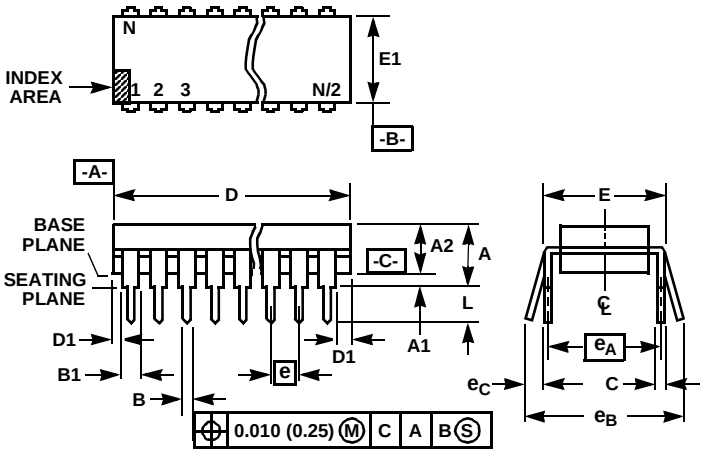


FIGURE 21. DIGITAL TRACK-AND-HOLD BLOCK DIAGRAM

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

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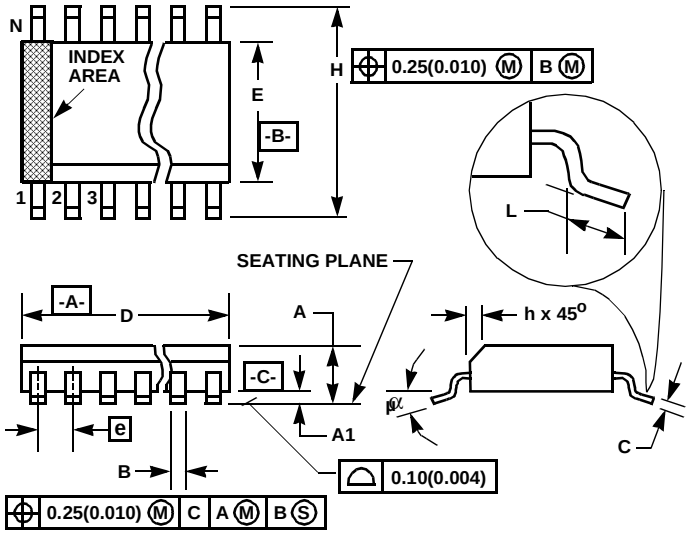
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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