CATALYST

Preliminary Information

CAT1024, CAT1025

Supervisory Circuits with I²C Serial 2k-bit CMOS EEPROM and Manual Reset

FEATURES

- Precision power supply voltage monitor
  - — 5V, 3.3V and 3V systems
  - — Five threshold voltage options
- Active high or low reset
  - — Valid reset guaranteed at V_{CC} = 1V
- 400kHz I²C bus
- 3.0V to 5.5V operation
- Low power CMOS technology
- 16-Byte page write buffer
- Built-in inadvertent write protection
  - — WP pin (CAT1025)
- 1,000,000 Program/Erase cycles
- Manual reset input
- 100 year data retention
- 8-pin DIP, SOIC, TSSOP, MSOP & TDFN (3x3mm foot print) packages
- Industrial and extended temperature ranges

DESCRIPTION

The CAT1024 and CAT1025 are complete memory and supervisory solutions for microcontroller-based systems. A 2k-bit serial EEPROM memory and a system power supervisor with brown-out protection are integrated together in low power CMOS technology. Memory interface is via a 400kHz I²C bus.

The CAT1025 provides a precision V_{CC} sense circuit and two open drain outputs: one (RESET) drives high and the other ($\overline{\text{RESET}}$) drives low whenever V_{CC} falls below the reset threshold voltage. The CAT1025 also has a Write Protect input (WP). Write operations are disabled if WP is connected to a logic high.

The CAT1024 also provides a precision V_{CC} sense circuit, but has only a $\overline{\text{RESET}}$ output and does not have a Write Protect input.

The power supply monitor and reset circuit protect memory and system controllers during power up/down and against brownout conditions. Five reset threshold voltages support 5V, 3.3V and 3V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 200 ms after the supply voltage exceeds the reset threshold level. With both active high and low reset signals, interface to microcontrollers and other ICs is simple. In addition, the $\overline{\text{RESET}}$ pin or a separate input, $\overline{\text{MR}}$, can be used as an input for push-button manual reset capability.

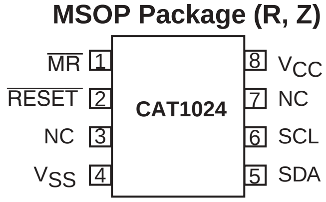
The CAT1024/25 memory features a 16-byte page. In addition, hardware data protection is provided by a V_{CC} sense circuit that prevents writes to memory whenever V_{CC} falls below the reset threshold or until V_{CC} reaches the reset threshold during power up.

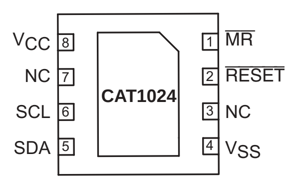
Available packages include an 8-pin DIP, 8-pin SOIC, 8-pin TSSOP, 8-pin TDFN and 8-pin MSOP. The TDFN package thickness is 0.8mm maximum. TDFN footprint is 3x3mm.

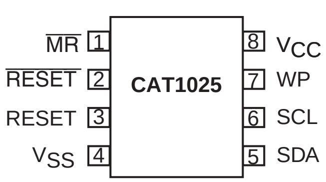
PIN CONFIGURATION

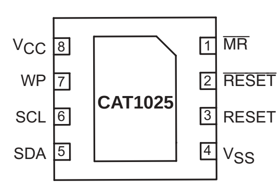
DIP Package (P, L)
SOIC Package (J, W)
TSSOP Package (U, Y)
MSOP Package (R, Z)

(Bottom View)
TDFN Package: 3mm x 3mm
0.8mm maximum height - (RD4, ZD4)

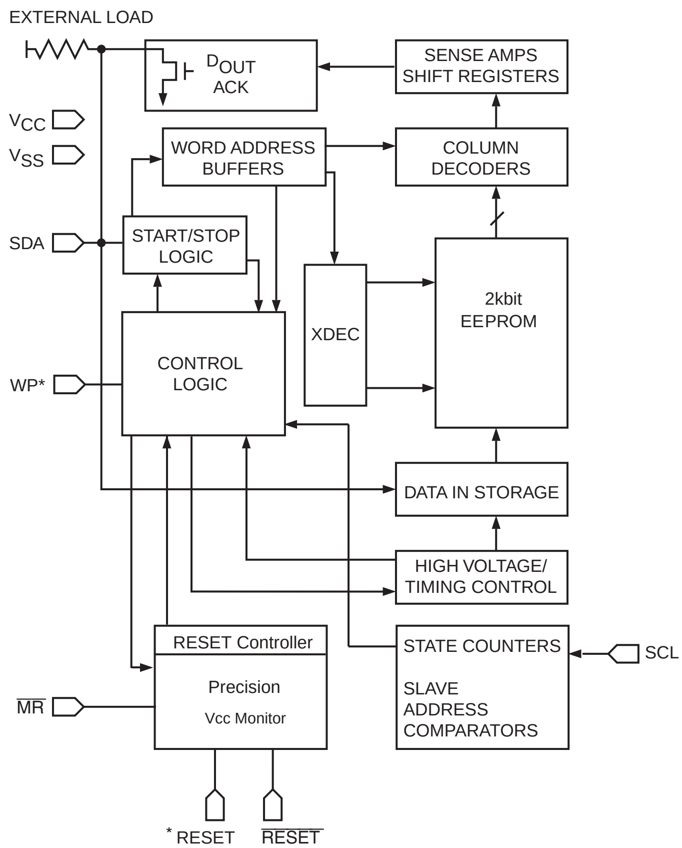








BLOCK DIAGRAM — CAT1024, CAT1025



*CAT1025 Only

Threshold Voltage Options

Part Dash Number	Minimum Threshold	Maximum Threshold
-45	4.50	4.75
-42	4.25	4.50
-30	3.00	3.15
-28	2.85	3.00
-25	2.55	2.70

PIN FUNCTIONS

Pin Name	Function
NC	No Connect
$\overline{\text{RESET}}$	Active Low Reset Input/Output
V_{SS}	Ground
SDA	Serial Data/Address
SCL	Clock Input
RESET	Active High Reset Output (CAT1025 only)
V_{CC}	Power Supply
WP	Write Protect (CAT1025 only)
$\overline{\text{MR}}$	Manual Reset Input

OPERATING TEMPERATURE RANGE

Industrial	-40˚C to 85˚C
Extended	-40˚C to 125˚C

PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: RESET OUTPUTS
(RESET CAT1025 Only)
These are open drain pins and $\overline{\text{RESET}}$ can be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull-down resistor, and the $\overline{\text{RESET}}$ pin must be connected through a pull-up resistor.

SDA: SERIAL DATA ADDRESS
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

SCL: SERIAL CLOCK
Serial clock input.

$\overline{\text{MR}}$: MANUAL RESET INPUT
Manual Reset input is a debounced input that can be connected to an external source for Manual Reset. Pulling the MR input low will generate a Reset condition. Reset outputs are active while $\overline{\text{MR}}$ input is low and for the reset timeout period after $\overline{\text{MR}}$ returns to high. The input has an internal pull-up resistor.

WP (CAT1025 Only): WRITE PROTECT INPUT
When tied to V_{SS} or left unconnected write operations to the entire array are allowed. When tied to V_{CC}, the entire array is protected. This input has an internal pull down resistor.

CAT10XX FAMILY OVERVIEW

Device	Manual Reset Input Pin	Watchdog	Watchdog Monitor Pin	Write Protection Pin	Independent Auxiliary Voltage Sense	RESET: Active High and LOW	EEPROM
CAT1021	●	●	SDA	●		●	2k
CAT1022	●	●	SDA				2k
CAT1023	●	●	WDI			●	2k
CAT1024	●						2k
CAT1025	●			●		●	2k
CAT1026					●	●	2k
CAT1027		●	WDI		●		2k

For supervisory circuits with embedded 16k EEPROM, please refer to the CAT1161, CAT1162 and CAT1163 data sheets.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... –55°C to +125°C

Storage Temperature....................... –65°C to +150°C

Voltage on any Pin with
Respect to Ground[1] .... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current[2] .... 100 mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +3.0V to +5.5V and over the recommended temperature conditions unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc	-2		10	µA
I_{LO}	Output Leakage Current	V_{IN} = GND to Vcc	-10		10	µA
I_{CC1}	Power Supply Current (Write)	f_{SCL} = 400kHz V_{CC} = 5.5V			3	mA
I_{CC2}	Power Supply Current (Read)	f_{SCL} = 400kHz V_{CC} = 5.5V			1	mA
I_{SB}	Standby Current	Vcc = 5.5V, V_{IN} = GND or Vcc			40	µA
V_{IL}[1]	Input Low Voltage		-0.5		0.3 x Vcc	V
V_{IH}[1]	Input High Voltage		0.7 x Vcc		Vcc + 0.5	V
V_{OL}	Output Low Voltage (SDA, $\overline{\text{RESET}}$)	I_{OL} = 3mA V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage (RESET)	I_{OH} = -0.4mA V_{CC} = 2.7V	Vcc - 0.75			V
V_{TH}	Reset Threshold	CAT102x-45 (V_{CC} = 5V)	4.50		4.75	V
		CAT102x-42 (V_{CC} = 5V)	4.25		4.50	
		CAT102x-30 (V_{CC} = 3.3V)	3.00		3.15	
		CAT102x-28 (V_{CC} = 3.3V)	2.85		3.00	
		CAT102x-25 (V_{CC} = 3V)	2.55		2.70	
V_{RVALID}	Reset Output Valid V_{CC} Voltage		1.00			V
V_{RT}[2]	Reset Threshold Hysteresis		15			mV

Notes:
1. V_{IL} min and V_{IH} max are reference values only and are not tested.
2. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Test Conditions	Max	Units
$C_{OUT}^{(1)}$	Output Capacitance	V_{OUT} = 0V	8	pF
$C_{IN}^{(1)}$	Input Capacitance	V_{IN} = 0V	6	pF

AC CHARACTERISTICS

V_{CC} = 3.0V to 5.5V and over the recommended temperature conditions, unless otherwise specified.

Memory Read & Write Cycle[2]

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency		400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)		100	ns
t_{LOW}	Clock Low Period	1.3		µs
t_{HIGH}	Clock High Period	0.6		µs
$t_R^{(1)}$	SDA and SCL Rise Time		300	ns
$t_F^{(1)}$	SDA and SCL Fall Time		300	ns
$t_{HD;STA}$	Start Condition Hold Time	0.6		µs
$t_{SU;STA}$	Start Condition Setup Time (for a Repeated Start)	0.6		µs
$t_{HD;DAT}$	Data Input Hold Time	0		ns
$t_{SU;DAT}$	Data Input Setup Time	100		ns
$t_{SU;STO}$	Stop Condition Setup Time	0.6		µs
t_{AA}	SCL Low to Data Out Valid		900	ns
t_{DH}	Data Out Hold Time	50		ns
$t_{BUF}^{(1)}$	Time the Bus must be Free Before a New Transmission Can Start	1.3		µs
$t_{WC}^{(3)}$	Write Cycle Time (Byte or Page)		5	ms

Notes:
1. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
2. Test Conditions according to “AC Test Conditions” table.
3. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PURST}	Reset Timeout	Note 2	130	200	270	ms
t_{RPD}	V_{TH} to RESET Output Delay	Note 3			5	µs
t_{GLITCH}	V_{CC} Glitch Reject Pulse Width	Note 4, 5			30	ns
MR Glitch	Manual Reset Glitch Immunity	Note 1			100	ns
t_{MRW}	MR Pulse Width	Note 1	5			µs
t_{MRD}	MR Input to RESET Output Delay	Note 1			1	µs

POWER-UP TIMING[5,6]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PUR}	Power-Up to Read Operation				270	ms
t_{PUW}	Power-Up to Write Operation				270	ms

AC TEST CONDITIONS

Parameter	Test Conditions
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Times	10 ns
Input Reference Voltages	$0.3V_{CC}$, $0.7V_{CC}$
Output Reference Voltages	$0.5V_{CC}$
Output Load	Current Source: I_{OL} = 3mA; C_L = 100pF

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END}(5)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR}(5)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP}(5)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH}(5)(7)	Latch-Up	JEDEC Standard 17	100		mA

Notes:
1. Test Conditions according to “AC Test Conditions” table.
2. Power-up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
3. Power-Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
4. V_{CC} Glitch Reference Voltage = V_{THmin}; Based on characterization data
5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified memory operation can be initiated.
7. Latch-up protection is provided for stresses up to 100mA on input and output pins from -1V to V_{CC} + 1V.

DEVICE OPERATION

Reset Controller Description

The CAT1024/25 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TH} threshold and will continue driving the outputs for approximately 200ms (t_{PURST}) after reaching V_{TH}. After the t_{PURST} timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors.

During power-down, the RESET outputs will be active when V_{CC} falls below V_{TH}. The $\overline{\text{RESET}}$ output will be valid so long as V_{CC} is >1.0V (V_{RVALID}). The device is designed to ignore the fast negative going V_{CC} transient pulses (glitches).

Reset output timing is shown in Figure 1.

Manual Reset Operation

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 msec timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

CAT1024/25 also have a separate manual reset input. Driving the $\overline{\text{MR}}$ input low by connecting a pushbutton (normally open) from $\overline{\text{MR}}$ pin to GND will generate a reset condition. The input has a internal pull up resistor.

Reset remains asserted while $\overline{\text{MR}}$ is low and for the Reset Timeout period after $\overline{\text{MR}}$ input has gone high.

Glitches shorter than 100 ns on $\overline{\text{MR}}$ input will not generate a reset pulse. No external debouncing circuits are required. Manual reset operation using $\overline{\text{MR}}$ input is shown in Figure 2.

Hardware Data Protection

The CAT1024/25 family has been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when incorrect data is stored in a memory location which is assumed to hold correct data.

Whenever the device is in a Reset condition, the embedded EEPROM is disabled for all operations, including write operations. If the Reset output(s) are active, in progress communications to the EEPROM are aborted and no new communications are allowed. In this condition an internal write cycle to the memory can not be started, but an in progress internal non-volatile memory write cycle can not be aborted. An internal write cycle initiated before the Reset condition can be successfully finished if there is enough time (5ms) before VCC reaches the minimum value of 2V.

In addition, the CAT1025 includes a Write Protection Input which when tied to V_{CC} will disable any write operations to the device.

Figure 1. RESET Output Timing

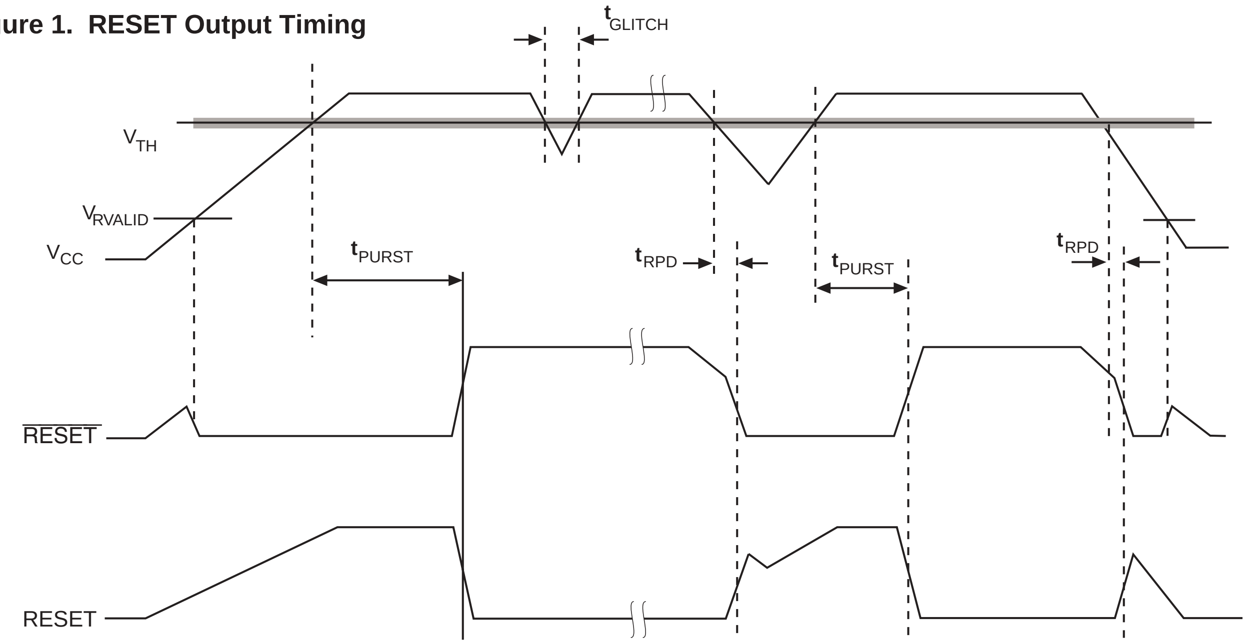
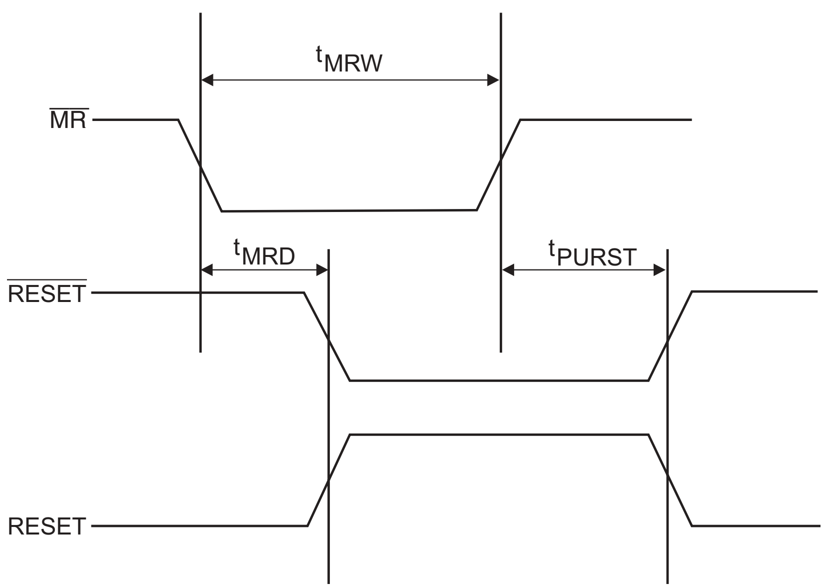


Figure 2. $\overline{MR}$ Operation and Timing



EMBEDDED EEPROM OPERATION

The CAT1024 and CAT1025 feature a 2kbit embedded serial EEPROM that supports the I^{2}C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^{2}C Bus Protocol

The features of the I^{2}C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1024/25 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1024/25 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1024/25 then performs a Read or Write operation depending on the R/$\overline{W}$ bit.

Figure 3. Bus Timing

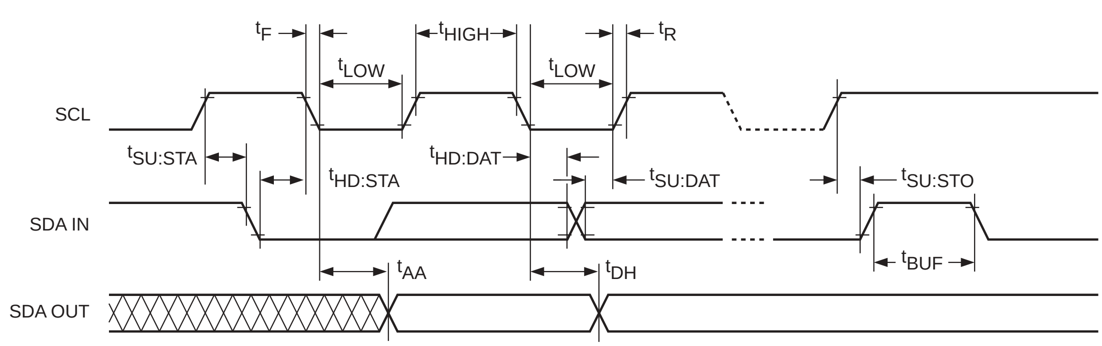
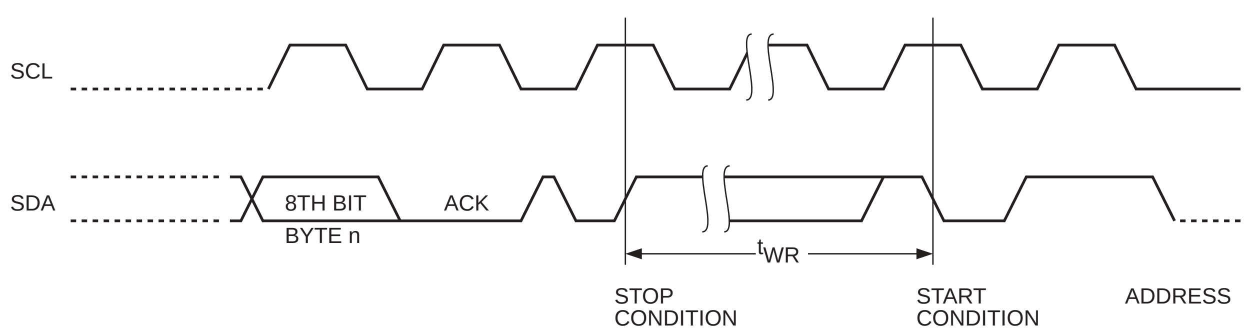


Figure 4. Write Cycle Timing



ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1024/25 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT1024/25 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1024/25 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8-bit address that is to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1024/25 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non-volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Figure 5. Start/Stop Timing

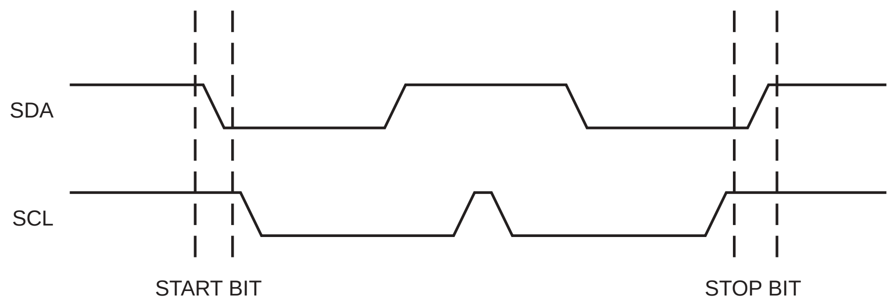


Figure 6. Acknowledge Timing

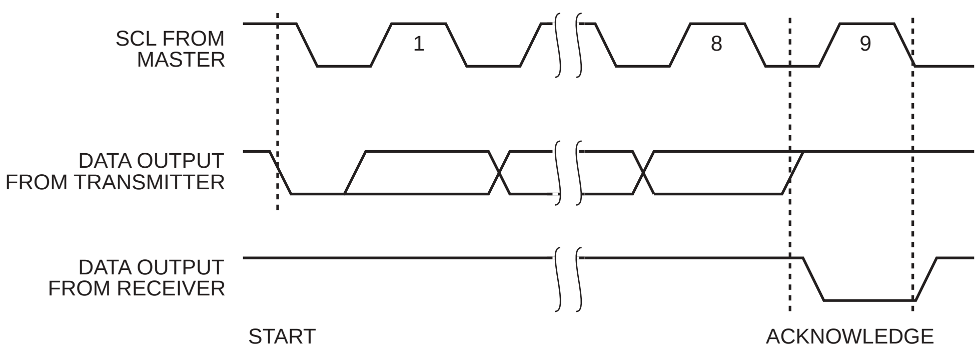


Figure 7. Slave Address Bits

Default Configuration								
	1	0	1	0	0	0	0	R/$\overline{W}$

Page Write

The CAT1024/25 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted, the CAT1024/25 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes before sending the STOP condition, the address counter 'wraps around,' and previously transmitted data will be overwritten.

When all 16 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1024/25 in a single write cycle.

Figure 8. Byte Write Timing

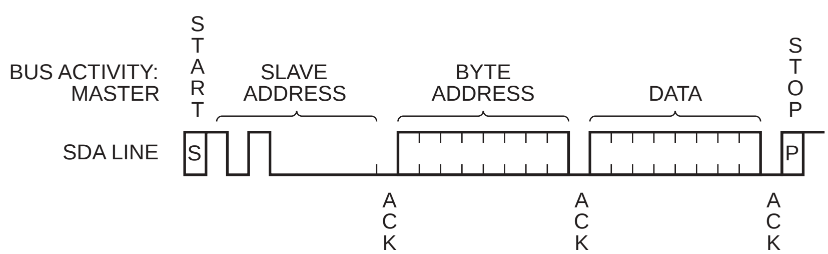
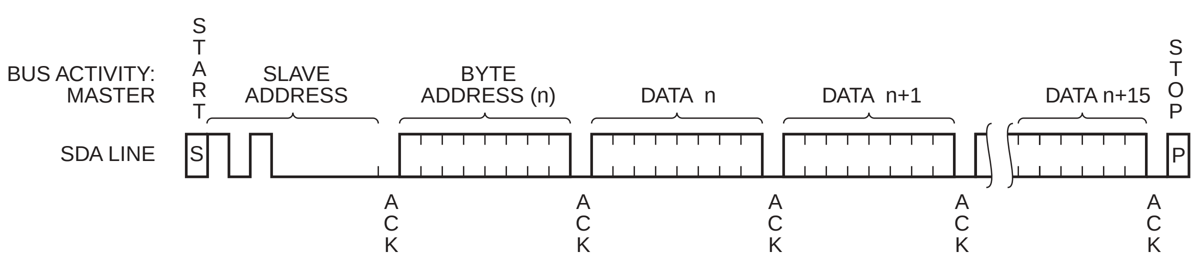


Figure 9. Page Write Timing



Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write opration, the CAT1024/25 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

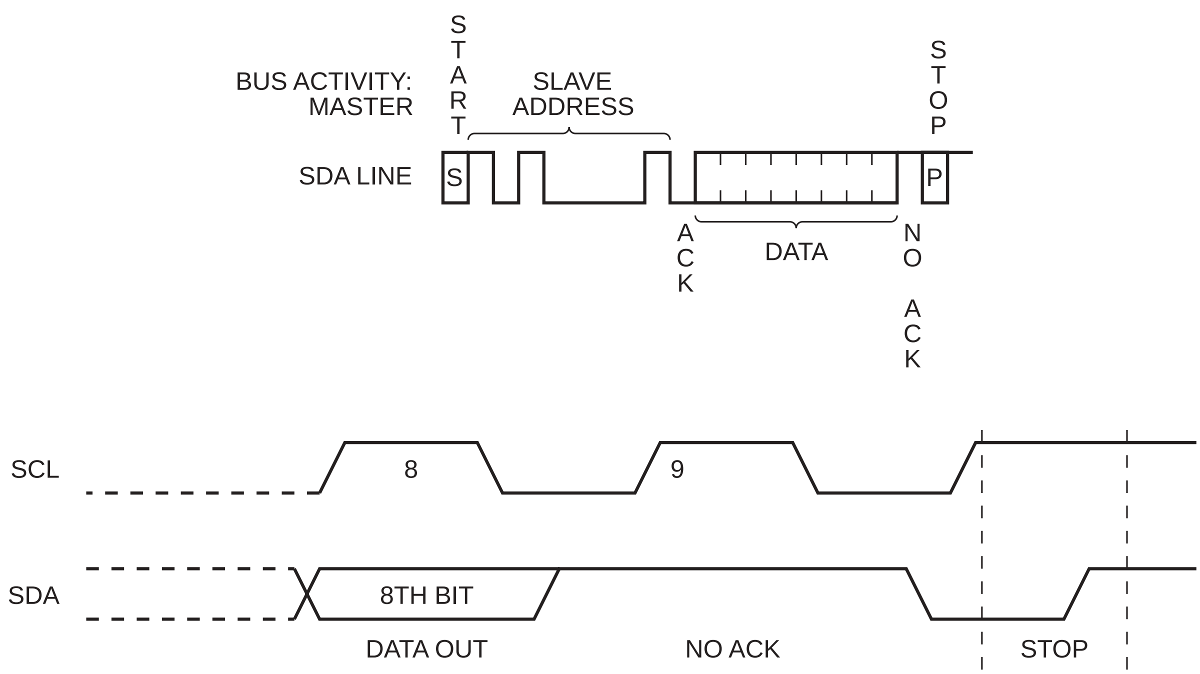
WRITE PROTECTION

The Write Protection feature (CAT1025 only) allows the user to protect against inadvertent memory array programming. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT1025 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

Read Operations

The READ operation for the CAT1024/25 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Figure 10. Immediate Address Read Timing



Immediate/Current Address Read

The CAT1024 and CAT1025 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. For N=E=255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1024 and CAT1025 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1024 and CAT1025 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1024 and CAT1025 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1024 and CAT1025 sends the inital 8-bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1024 and CAT1025 will continue to output an 8-bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1024 and CAT1025 is sent sequentially with the data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT1024 and CAT1025 address bits so that the entire memory array can be read during one operation.

Figure 11. Selective Read Timing

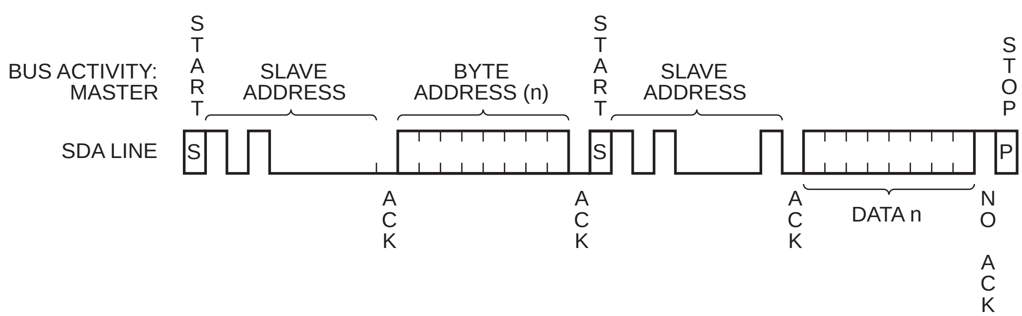
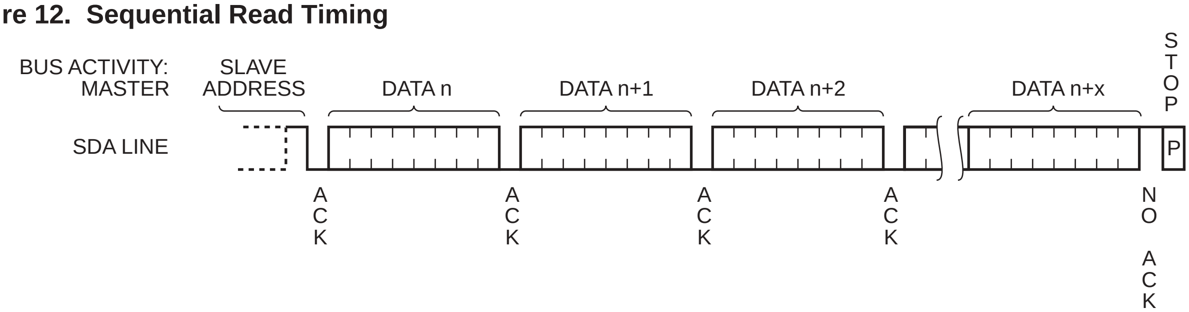
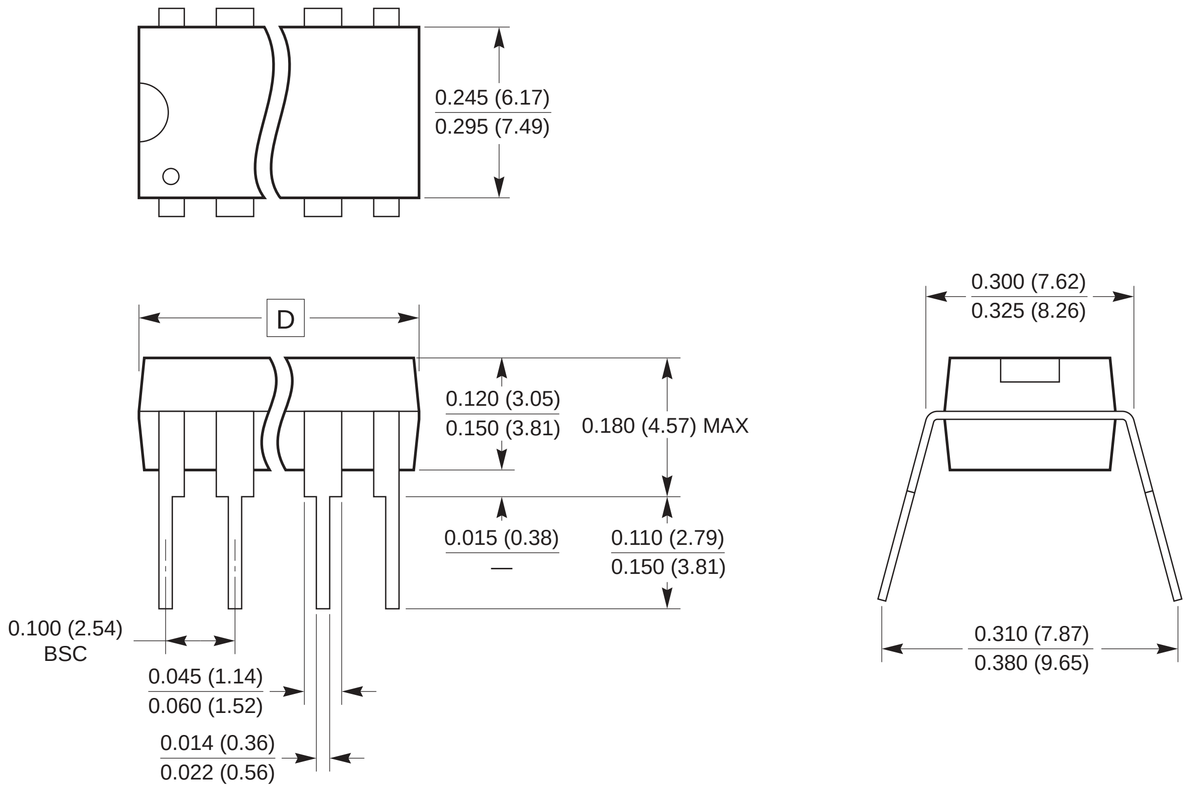


Figure 12. Sequential Read Timing



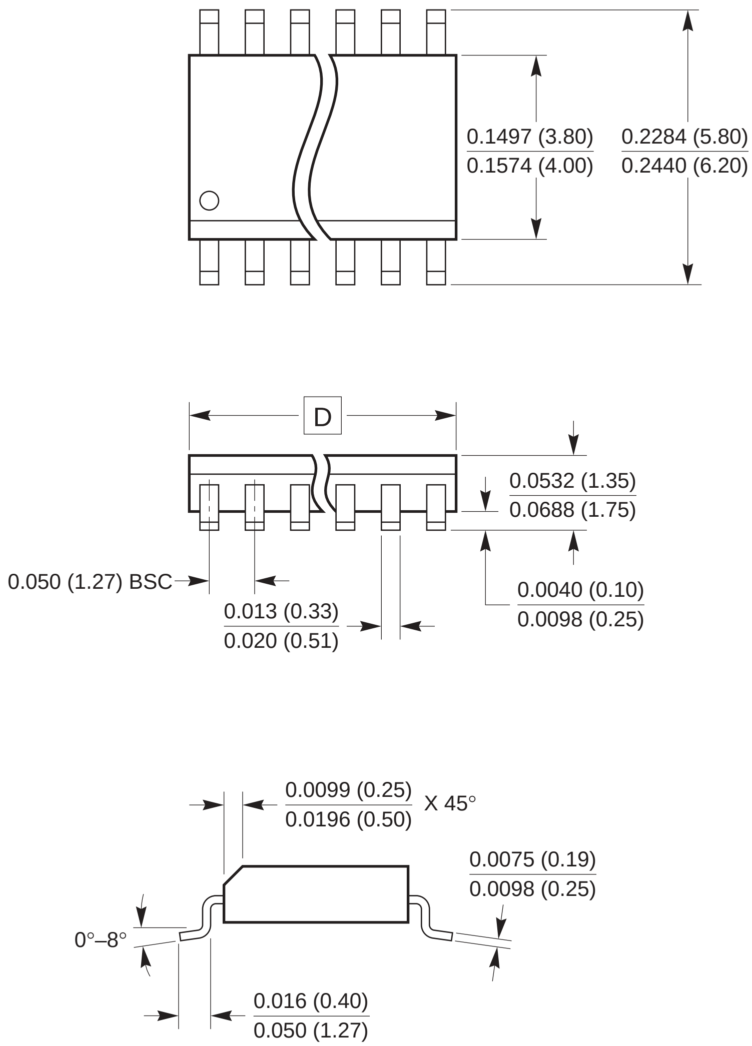
PACKAGE OUTLINES
8-LEAD 300 MIL WIDE PLASTIC DIP (P, L)



Dimension D		
Pkg	**Min**	**Max**
8L	0.355 (9.02)	0.400 (10.16)

Notes:
1. Complies with JEDEC Publication 95 MS001 dimensions; however, some of the dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

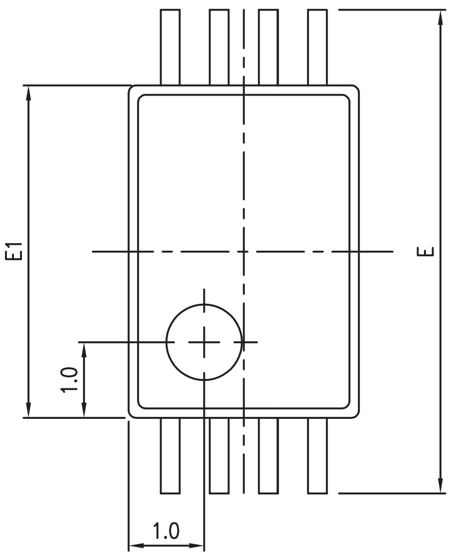
8-LEAD 150 MIL WIDE SOIC (J, W)

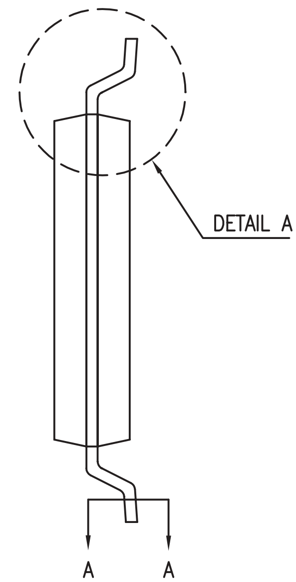


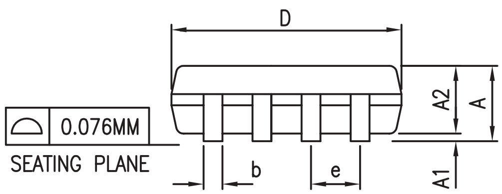
Dimension D		
Pkg	**Min**	**Max**
8L	0.1890(4.80)	0.1968(5.00)

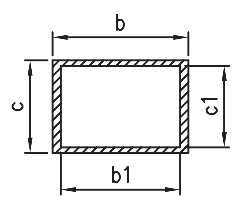
Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.
3. Lead coplanarity is 0.004" (0.102mm) maximum.

8-LEAD TSSOP (U, Y)

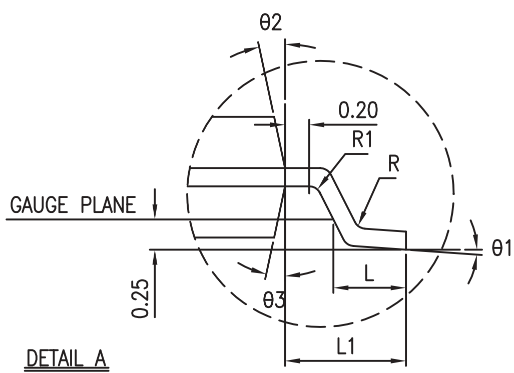








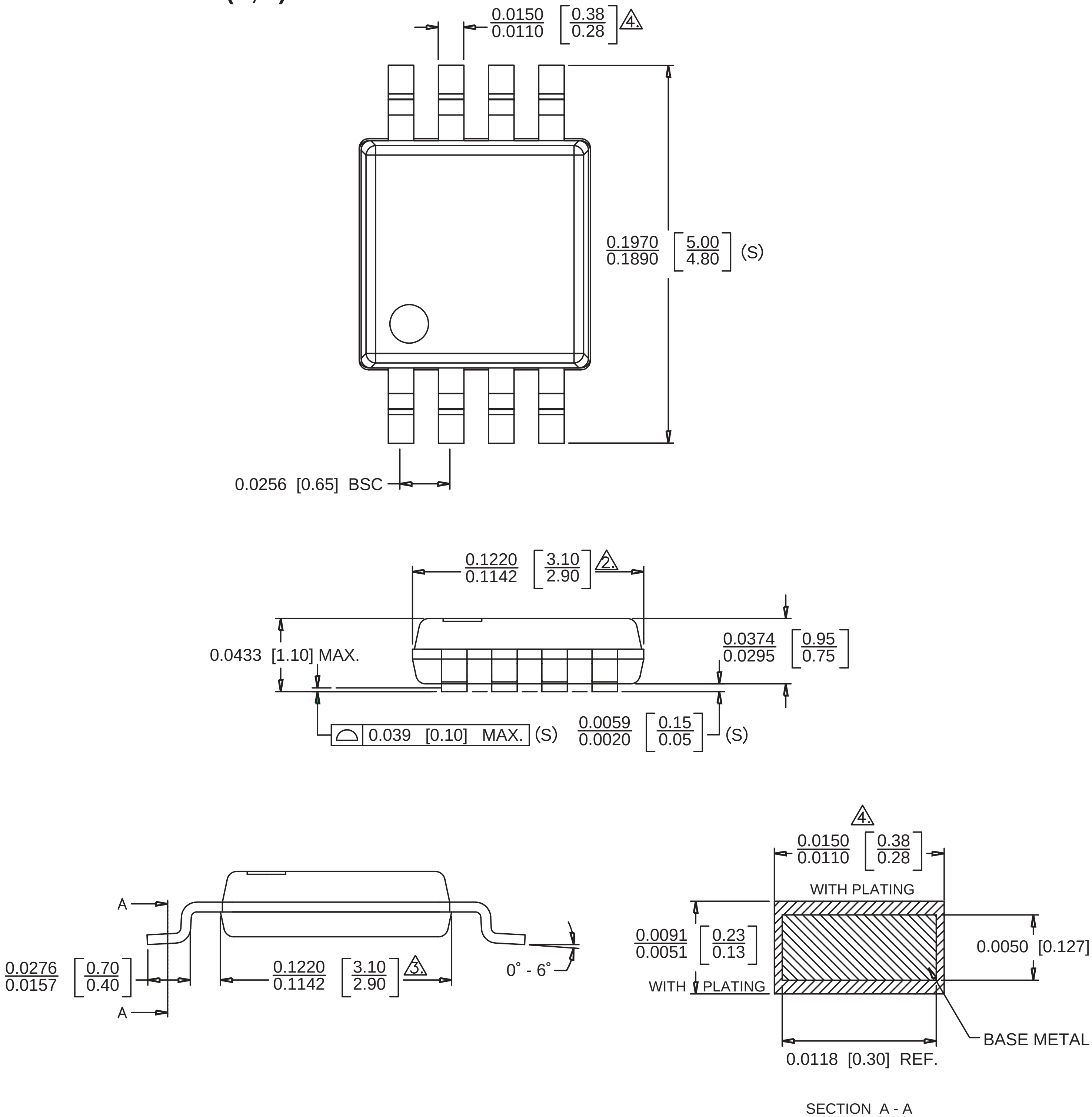
SECTION A–A



DETAIL A

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			.043
A1	0.05		0.15	.002		.006
A2	0.80	0.90	1.05	.031	.035	.041
L	0.50	0.60	0.75	.020	.024	.030
D	2.90	3.00	3.10	.114	.118	.122
E	6.30	6.40	6.50	.248	.252	.256
E1	4.30	4.40	4.50	.169	.173	.177
R	0.09			.004		
R1	0.09			.004		
b	0.19		0.30	.007		.012
b1	0.19	0.22	0.25	.007	.009	.010
c	0.09		0.20	.004		.008
c1	0.09		0.16	.004		.006
L1	1.0 REF.			.039 REF.		
e	0.65 BSC.			.026 BSC.		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		
N	8					
REF	JEDEC MO–153 VARIATION AA					

8 LEAD MSOP (R, Z)



Notes:

(1) All dimensions are in mm Angles in degrees.

2. Does not include Mold Flash, Protrusion or Gate Burrs. Mold Flash, Protrusions or Gate Burrs shall not exceed 0.15 mm. per side.

3. Does not include Interlead Flash orProtrusion. Interlead Flash or Protrusion shall not exceed 0.25 mm per side.

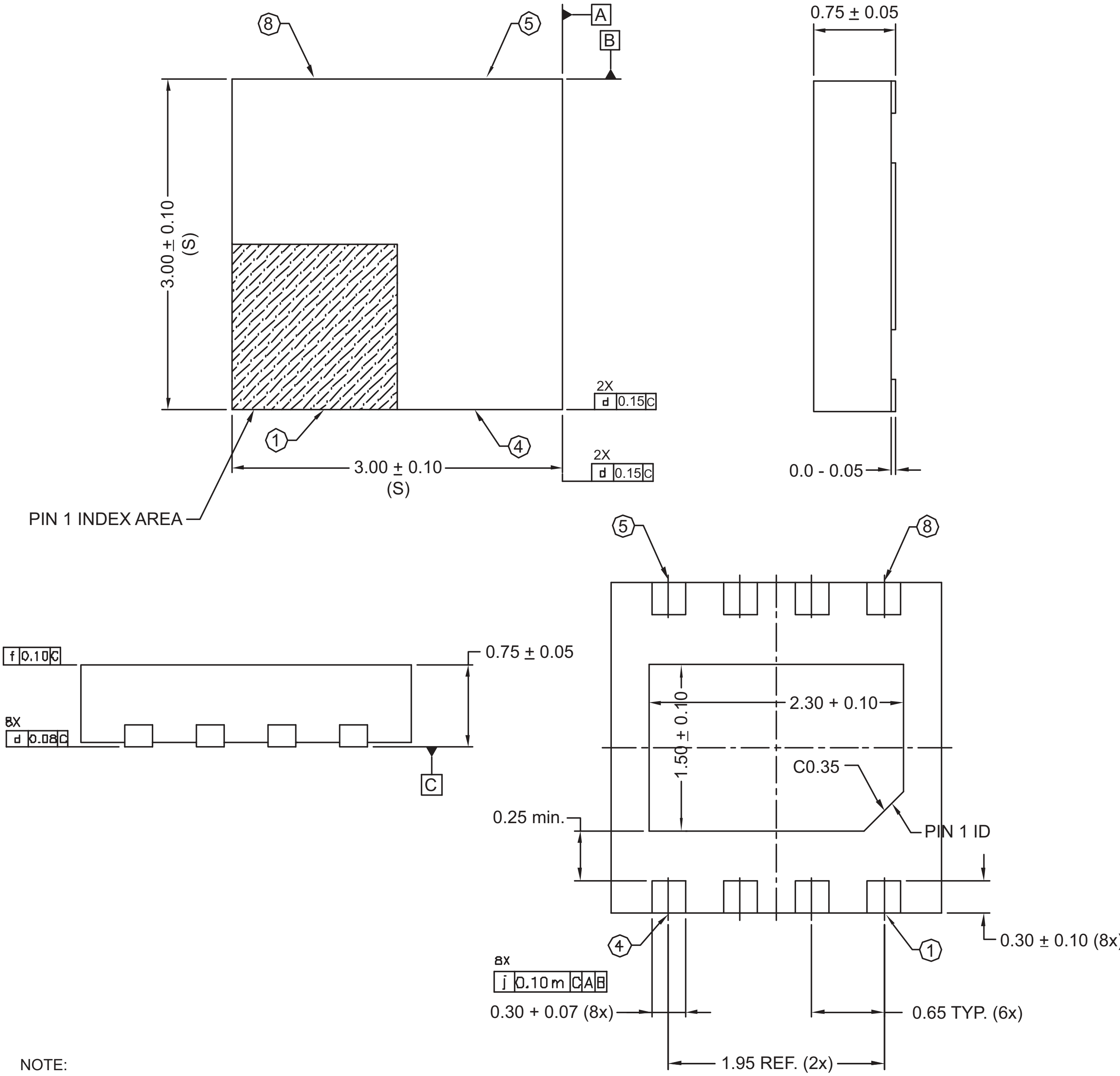
4. Does not include Dambar Protrusion, allowable Dambar Protrusion shall be 0.08 mm.

(5) This part is compliant with JEDEC Specification MO-187 Variations AA.

(6) Lead span/stand off height/coplanarity are considered as special characteristics. (S)

(7) Controlling dimensions in inches. [mm]

TDFN 3X3 PACKAGE (RD4, ZD4)



NOTE:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S)
5. REFER JEDEC MO-229 / WEEC

Ordering Information

Prefix	Device #	Suffix			
CAT	1024	J	I	-30	TE13
Optional Company ID	Product Number	Package	Temperature Range	Reset Threshold Voltage	Tape & Reel

Optional Company ID

Product Number
1024: 2K
1025: 2K

Temperature Range
I = Industrial (-40˚C to 85˚C)
E = Extended Automotive (-40˚C to +125˚C)

Tape & Reel
SOIC: 2000/Reel
TSSOP: 2000/Reel
MSOP: 2500/Reel
TDFN: 2000/Reel

Package
P: PDIP
J: SOIC (JEDEC)
R: MSOP
U: TSSOP
RD4: 8-pad TDFN (3x3mm)
L: PDIP (Lead free, Halogen free)
W: SOIC (JEDEC, Lead free, Halogen free)
Z: MSOP Lead free, Halogen free)
Y: TSSOP (Lead free, Halogen free)
ZD4: 3x3mm TDFN (Lead free, Halogen free)

Reset Threshold Voltage
45: 4.5-4.75V
42: 4.25-4.5V
30: 3.0-3.15V
28: 2.85-3.0V
25: 2.55-2.7V

Note:
(1) The device used in the above example is a CAT1024JI-30TE13 (Supervisory circuit with I^2C serial 2k CMOS EEPROM, SOIC, Industrial Temperature, 3.0-3.15V Reset Threshold Voltage, Tape and Reel).

REVISION HISTORY

Date	Rev.	Reason
11/7/03	I	Eliminated Automotive temperature range
4/12/2004	J	Eliminated data sheet designation Updated Reel Ordering Information
11/1/2004	K	Changed SOIC package designators Eliminated 8-pad TDFN (3x4.9mm) package Added package outlines
11/04/04	L	Update Pin Configuration
11/11/04	M	Update Features Update Description Updae DC Operating Characteristic Update AC Characteristics

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