CAT24FC32A

32K-Bit Fast Mode I²C Serial CMOS EEPROM

FEATURES

- Fast mode I²C bus compatible*
- Max clock frequency:
  400 kHz for V_{cc}=1.8V to 3.6V
- Hardware write protect for entire array
- Cascadable for up to eight devices
- 32-Byte page or byte write modes
- Self-timed write cycle with autoclear
- 5 ms max write cycle time
- Random and sequential read modes
- Schmitt trigger and spike suppression at SDA and SCL inputs
- Output slope control to eliminate ground bounce
- Zero standby current
- Commercial temperature range
- 1,000,000 program/erase cycles
- 100 years data retention
- 8-pin PDIP, 8-pin SOIC (150 and 200 mil) and 8-pin TSSOP packages
- "Green" package options available

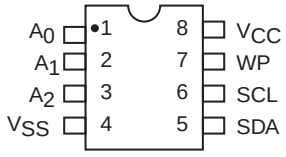
DESCRIPTION

The CAT24FC32A is a 32K-bit Serial CMOS EEPROM internally organized as 4Kx8 bits. The device is compatible with Fast-mode I²C bus specification and operates down to 1.8V with a bit rate up to 400 kbit/s. Extended addressing capability allows up to 8 devices to share the same bus. Catalyst's advanced CMOS technology substantially reduces device power requirements. The device is optimized for high performance applications, where low power, low voltage and high speed operation are required.

CAT24FC32A is available in 8-pin DIP, 8-pin SOIC (JEDEC and EIAJ) and 8-pin TSSOP packages.

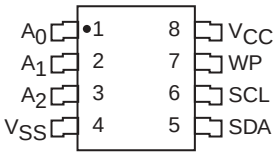
PIN CONFIGURATION

DIP Package (P, L)

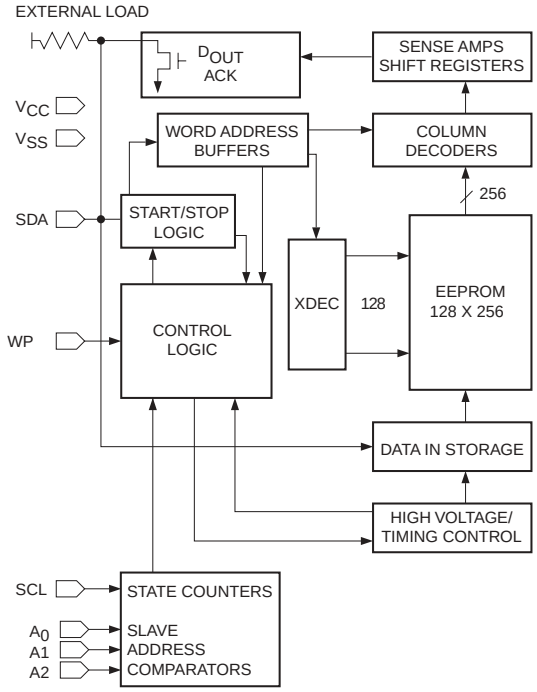


TSSOP Package (U, Y)

SOIC Package (J,W) (K, X)



BLOCK DIAGRAM



* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

Doc. No. 1048, Rev. F

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

RECOMMENDED OPERATING CONDITIONS

Temperature Range	Minimum	Maximum
Commercial	0˚C	+70˚C

Supply Voltage Range	Device
1.8V to 3.6V	CAT24FC32A

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Leakage Current(4)	-10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current(4)	-10		10	µA	V_{IN} = GND to V_{CC}
I_{CC1}	Power Supply Current (Operating Write)			3	mA	f_{SCL} = 400kHz V_{CC} = 3.6V
I_{CC2}	Power Supply Current (Operating Read)			400	µA	f_{SCL} = 400kHz V_{CC} = 3.6V
I_{SB}(1)	Standby Current			0	µA	V_{CC} = 3.6V V_{IN} = GND or V_{CC}
V_{IL}(2)	Input Low Voltage	-0.5		$0.3V_{CC}$	V	
V_{IH}(2)	Input High Voltage	$0.7V_{CC}$		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	2.5V ≤ V_{CC} ≤ 3.6V I_{OL} = 3.0 mA
V_{OL2}	Output Low Voltage			$0.2V_{CC}$	V	1.8V ≤ V_{CC} < 2.5V I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 3.6V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL, WP)	6	pF	V_{IN} = 0V

Note:
(1) Standby current, I_{SB} < 900 nA; A0, A1, A2, WP connected to GND; SCL, SDA = GND or VCC.
(2) V_{IL} min and V_{IH} max are reference values only and are not tested.
(3) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
(4) I/O pins, SDA and SCL do not obstruct the bus lines if V_{CC} is switched off.

A.C. CHARACTERISTICS

Over recommended operating conditions, unless otherwise specified (Note 1).

Symbol	Parameter	VCC=1.8V - 3.6V			Units
		Min	Typ	Max	
f_{SCL}	Clock Frequency			400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)			50	ns
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	0.6			µs
t_R (2)	SDA and SCL Rise Time	20		300	ns
t_F (2)	SDA and SCL Fall Time	20		300	ns
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start)	0.6			µs
$t_{HD:DAT}$	Data Input Hold Time	0			ns
$t_{SU:DAT}$	Data In Setup Time	100			ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs
$t_{SU:WP}$	WP Setup Time	0			µs
$t_{HD:WP}$	WP Hold Time	2.5			µs
t_{AA}	SCL Low to Data Out Valid			900	ns
t_{DH}	Data Out Hold Time	50			ns
t_{BUF} (2)	Time the Bus must be Free Before a New Transmission Can Start	1.3			µs
t_{OF} (2)	Output Fall Time from V_{IH} min to V_{IL} max	20		250	ns
t_{WC} (3)	Write Cycle Time (Byte or Page)			5	ms

Power-Up Timing (2)(4)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-Up to Read Operation			1	ms
t_{PUW}	Power-Up to Write Operation			1	ms

Note:
(1) Test Conditions according to "AC Test Conditions" Table.
(2) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
(3) The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

AC TEST CONDITIONS

Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input rise and fall times	≤ 50 ns
Input reference voltages	$0.3V_{CC}$, $0.7V_{CC}$
Output reference voltages	$0.5V_{CC}$
Output load	Current source: I_{OL} = 3mA; CL: 400pF for f_{SCl} max = 400kHz / 100pF for f_{SCL} max = 1 MHz

Figure 1. Bus Timing

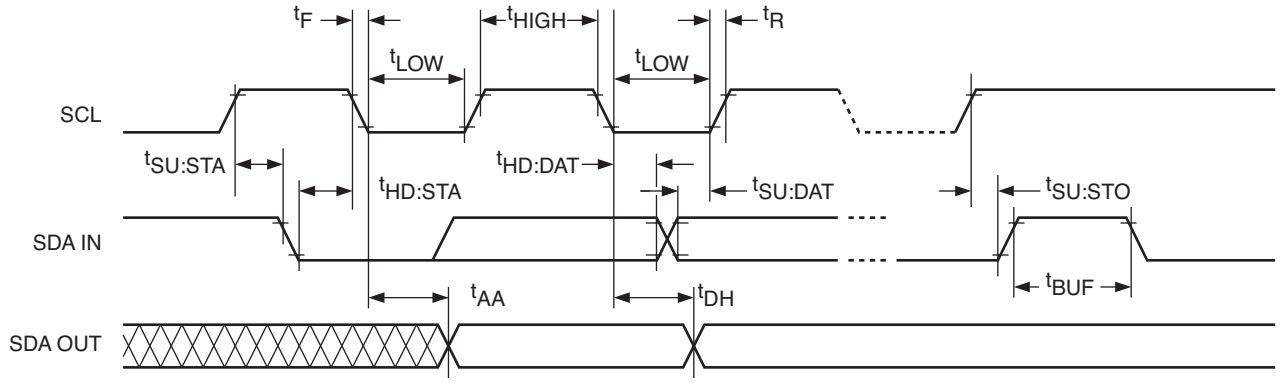


Figure 2. WP Timing

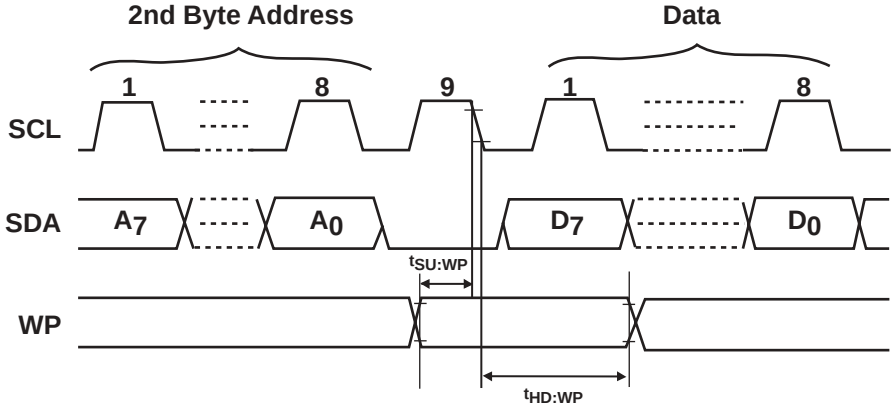
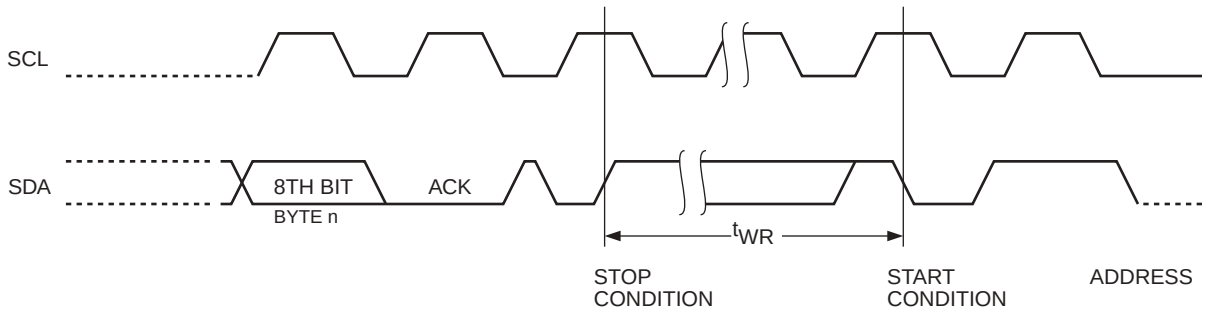


Figure 3. Write Cycle Timing



PIN DESCRIPTION

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull-up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs. A pull-up resistor must be connected from SDA line to Vcc. The value of the pull-up resistor, Rp, can be calculated based on minimum and maximum values from Figure 4 and Figure 5. (see Note).

WP: Write Protect

This input controls the device write protect feature. WP pin connected to V_{SS} allows write operations to the entire memory. When this pin is connected to Vcc, the entire memory is write protected. When left floating, an internal pull-down resistor on this input will keep the memory unprotected. Read operations are not affected.

A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins can be hardwired to V_{CC} or V_{SS}, or left unconnected. When hardwired, up to eight CAT24FC32As may be addressed on a single bus system. When the pins are left unconnected, the default values are zero. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

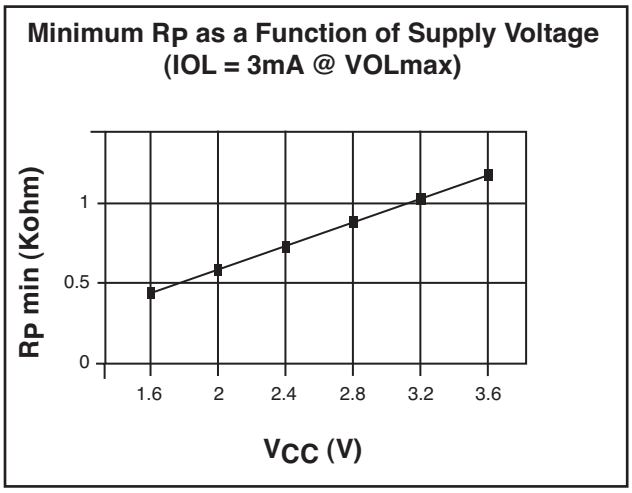


Figure 4

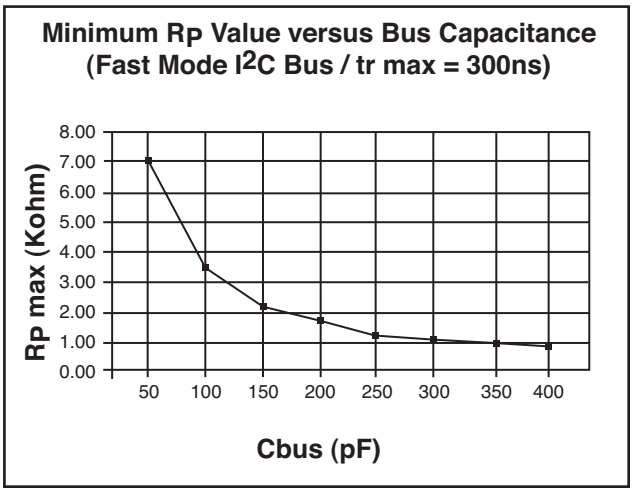


Figure 5

Note: According to the Fast Mode I^2C bus specification, for bus capacitance up to 200pF, the pull up device can be a resistor. For bus loads between 200pF and 400pF, the pull-up device can be a current source (Imax=3mA) or a switched resistor circuit.

FUNCTIONAL DESCRIPTION

The CAT24FC32A supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24FC32A operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 6).

START Condition

The START condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24FC32A monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

After the bus Master sends a START condition, a slave address byte is required to enable the CAT24FC32A for a read or write operation (Figure 7). The four most significant bits of the 8-bit slave address are fixed as binary 1010. The CAT24FC32A uses the next three bits as address bits. The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The last bit of the slave address specifies whether a read or write operation is to be performed. When this bit is set to "1", a read operation is initiated, and when set to "0", a write operation is selected.

Following the START condition and the slave address byte, the CAT24FC32A monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24FC32A then performs a read or write operation depending on the state of the R/W bit.

Figure 6. Start/Stop Timing

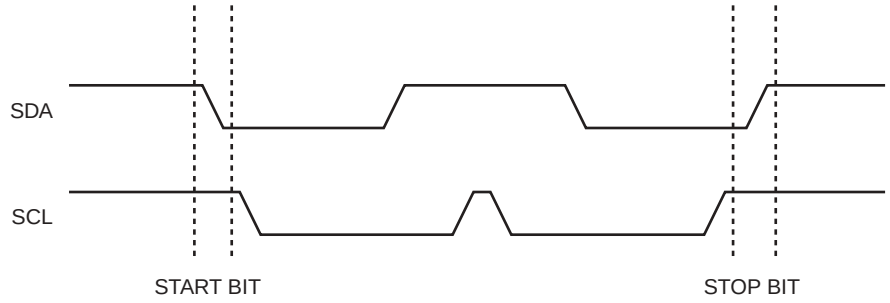


Figure 7. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 8).

The CAT24FC32A responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte. The CAT24FC32A does not generate acknowledge if an internal write cycle is in progress.

When the CAT24FC32A begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24FC32A will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT24FC32A to the standby power mode and place the device in a known state.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8-bit address words that are to be written into the address pointers of the CAT24FC32A. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24FC32A acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24FC32A writes up to 32 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 31 additional bytes. After each byte has

Figure 8. Acknowledge Timing

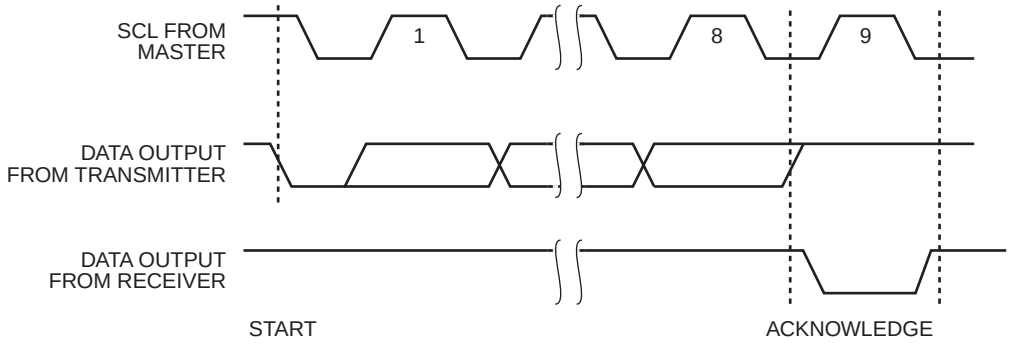
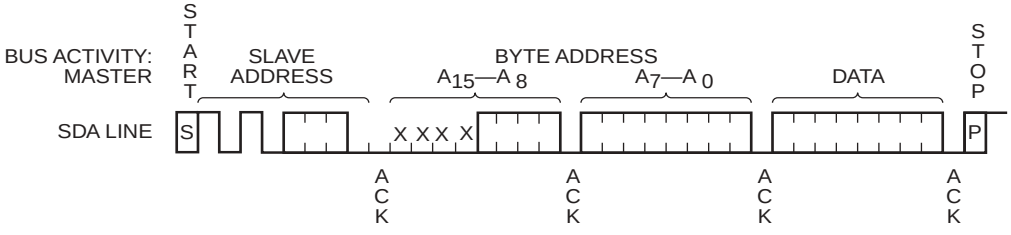


Figure 9. Byte Write Timing



X = Don't care bit

been transmitted, CAT24FC32A will respond with an acknowledge, and internally increment the five low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 32 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 32 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24FC32A in a single write cycle.

Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, CAT24FC32A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24FC32A is still busy with the write operation, no ACK will be returned. If CAT24FC32A has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is connected to V_{CC}, the entire memory array is protected and becomes read only. The CAT24FC32A will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received. The WP input is sampled in the end of acknowledge pulse after second address byte, accordingly with setup and hold times relative to negative clock edge (Figure 2).

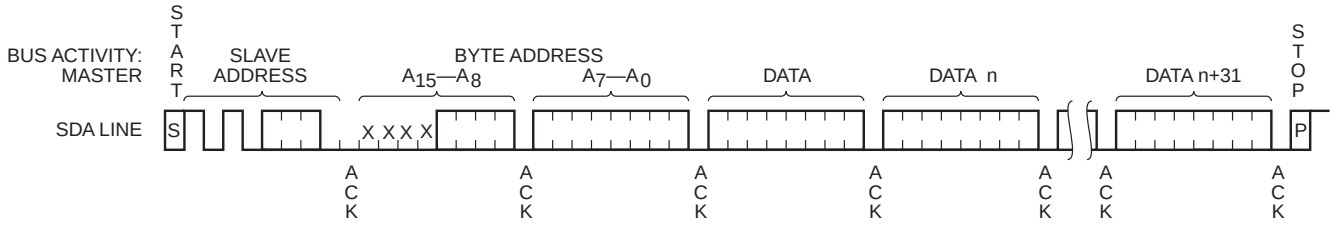
READ OPERATIONS

The READ operation for the CAT24FC32A is initiated in the same manner as the write operation with one exception, that R/W bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Immediate/Current Address Read

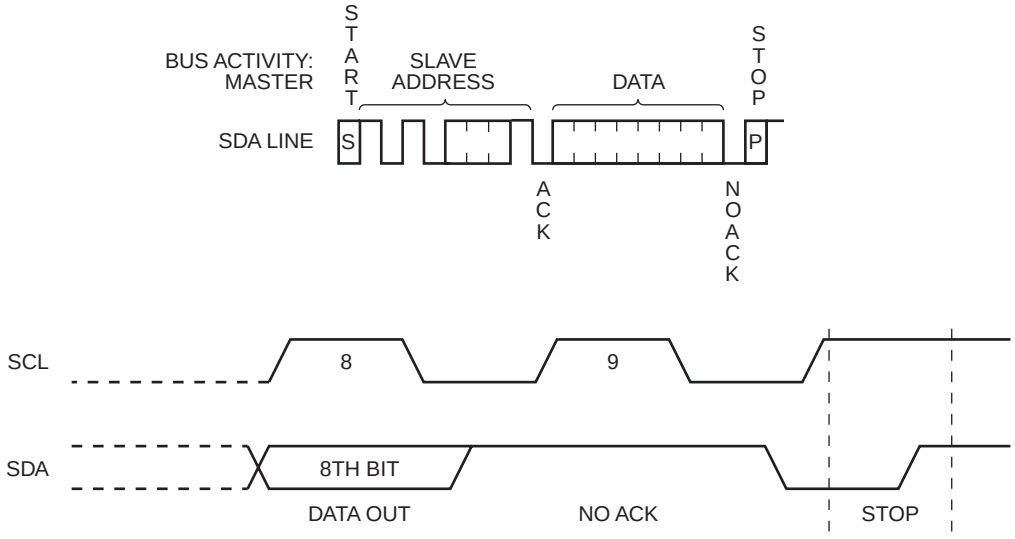
The CAT24FC32A's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was

Figure 10. Page Write Timing



X=Don't care bit

Figure 11. Immediate Address Read Timing



to address N, the READ immediately following would access data from address N+1. If N=E (where E=4095), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24FC32A receives its slave address information (with the R/W bit set to one), it issues an acknowledge, then transmits the 8 bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

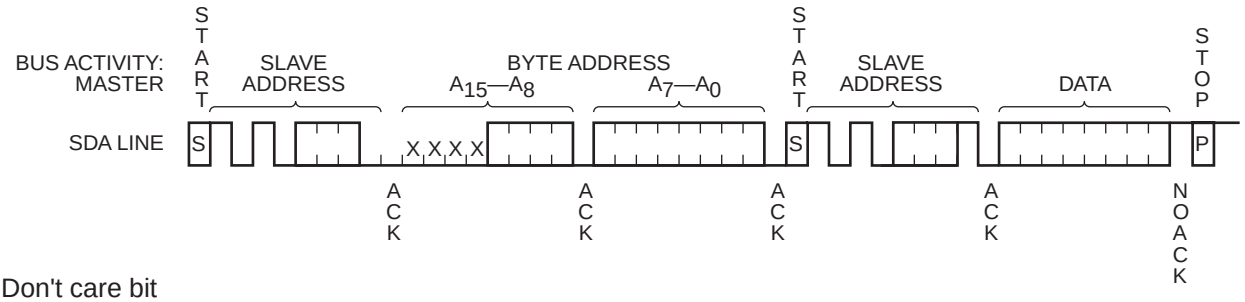
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24FC32A acknowledges, the Master device sends the START condition and the slave address again, this time with the R/W bit set to one. The CAT24FC32A then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24FC32A sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24FC32A will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

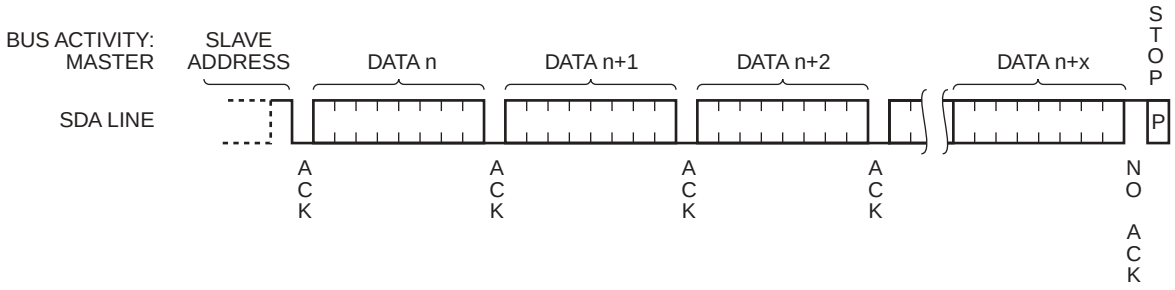
The data being transmitted from CAT24FC32A is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24FC32A address bits so that the entire memory array can be read during one operation. After the last memory address is read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 12. Selective Read Timing

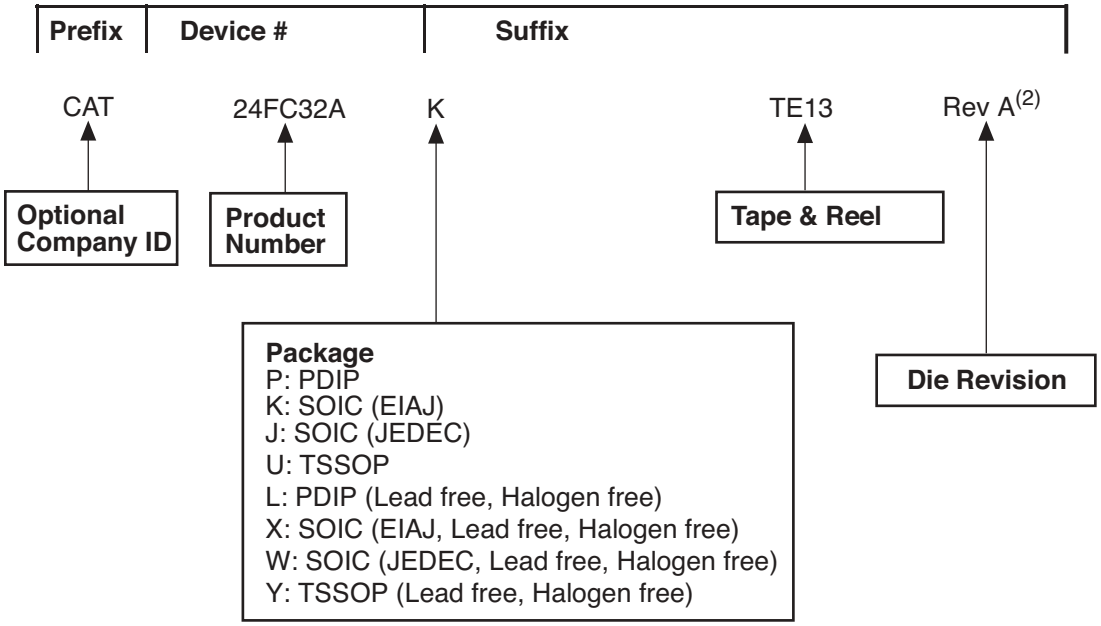


X = Don't care bit

Figure 13. Sequential Read Timing



ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT24FC32AK-TE13 (SOIC, Commercial Temperature, Tape & Reel)
(2) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWA). For additional information, please contact your Catalyst sales office.

REVISION HISTORY

Date	Revision	Comments
12/10/2003	C	Eliminated Commercial temperature range
04/18/2004	D	Delete data sheet designation Add Lead Free Logo Update Features Update Ordering Information Add Revision History Update Rev Number
7/7/2004	E	Add die revision to Ordering Information
11/04/2004	F	Update Features Update Recommended Operating Conditions Update Ordering Information

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