CAT28F002

2 Megabit CMOS Boot Block Flash Memory

Licensed Intel second source

FEATURES

- **Fast Read Access Time: 90/120/150 ns**
- **On-Chip Address and Data Latches**
- **Blocked Architecture:**
  - **— One 16-KB Protected Boot Block**
    - **• Top or Bottom Locations**
  - **— Two 8-KB Parameter Blocks**
  - **— One 96-KB Main Block**
  - **— One 128-KB Main Block**
- **Hardware Data Protection**
- **Automated Program and Erase Algorithms**
- **Automatic Power Savings Feature**
- **Low Power CMOS Operation**
- **12.0V ± 5% Programming and Erase Voltage**
- **Electronic Signature**
- **100,000 Program/Erase Cycles and 10 Year Data Retention**
- **Standard Pinouts:**
  - **— 40-Lead TSOP**
  - **— 40-Lead PDIP**
- **High Speed Programming**
- **Commercial, Industrial and Automotive Temperature Ranges**
- **Reset/Deep PowerDown Mode**
  - **— 0.2μA I_{CC} Typical**
  - **— Acts as Reset for Boot Operations**

DESCRIPTION

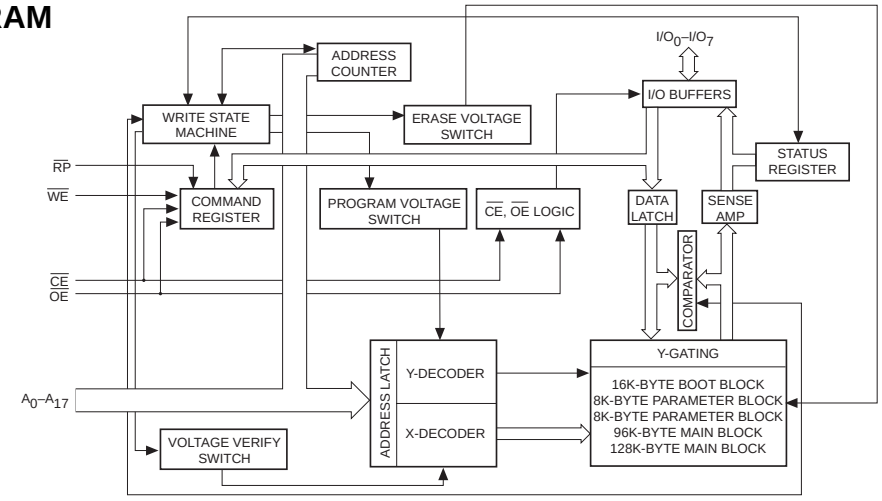
The CAT28F002 is a high speed 256K X 8-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after sale code updates.

The CAT28F002 has a blocked architecture with one 16 KB Boot Block, two 8 KB Parameter Blocks, one 96 KB Main Block and one 128 KB Main Block. The Boot Block section can be at the top or bottom of the memory map. The Boot Block section includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to other locations of CAT28F002.

The CAT28F002 is designed with a signature mode which allows the user to identify the IC manufacturer and device type. The CAT28F002 is also designed with on-Chip Address Latches, Data Latches, Programming and Erase Algorithms. A deep power-down mode lowers the total V_{CC} power consumption 1μw typical.

The CAT28F002 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 40-pin TSOP and 40-pin PDIP packages.

BLOCK DIAGRAM



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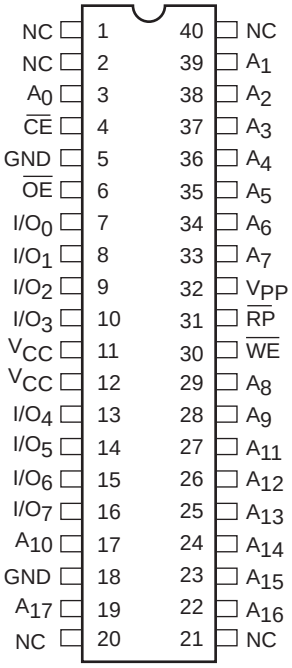
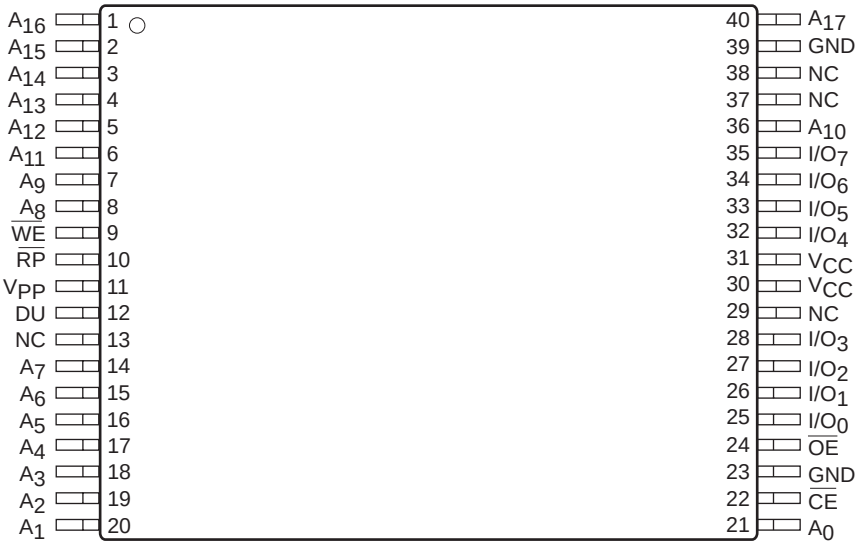
Doc. No. 25072-00 2/98 F-1

PIN CONFIGURATION

PDIP Package (P)



TSOP Package (T)



PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{17}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply
$\overline{RP}$	Input	Power Down
DU		Do Not Use

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) ..... –2.0V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		8	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		12	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V
I_{LO}	Output Leakage Current		±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.2V = $\overline{RP}$ V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.5	mA	$\overline{CE} = \overline{RP} = V_{IH}$, V_{CC} = 5.5V
I_{PPD}	V_{PP} Deep Powerdown Current		5.0	µA	$\overline{RP}$ = GND±0.2V
I_{CC1}	V_{CC} Active Read Current		55	mA	V_{CC} = 5.5V, CE = GND, I_{OUT} = 0mA, f = 10 MHz
I_{CC2}(1)	V_{CC} Programming Current		50	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		30	mA	V_{CC} = 5.5V, Erase in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} \leq V_{CC}$
			200	µA	$V_{PP} > V_{CC}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(1)	V_{PP} Programming Current		20	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current		15	mA	$V_{PP} = V_{PPH}$, Erase in Progress
V_{IL}	Input Low Level	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level	2.0	V_{CC}+0.5	V	
V_{OH1}	Output High Level TTL	2.4		V	I_{OH} = -2.5mA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	10.8	13.2	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		500	µA	$A_9 = V_{ID}$
I_{CCD}	V_{CC} Deep Powerdown Current		1.0	µA	$\overline{RP}$ = GND±0.2V
I_{CCES}	V_{CC} Erase Suspend Current		10	mA	Erase Suspended $\overline{CE} = V_{IH}$
I_{PPES}	V_{PP} Erase Suspend Current		200	µA	Erase Suspended $V_{PP}=V_{PPH}$
$I_{\overline{RP}}$	$\overline{RP}$ Boot Block Unlock Current		500	µA	$\overline{RP} = V_{HH}$
V_{OH2}	Output High Level TTL	0.85 V_{CC}		V	$V_{CC} = V_{CCMIN}$ I_{OH} = -1.5mA

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	2.0		V
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Erase/Program	11.4	12.6	V
V_{HH}	$\overline{RP}$, $\overline{OE}$ Unlock Voltage	10.8	13.2	V
V_{PPLK}	V_{PP} Lock-Out Voltage	0	6.5	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F002-90		28F002-12		28F002-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	90			120		150	ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		90		120		150	ns
t_{AVQV}	t_{ACC}	Address Access Time		90		120		150	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		40		40		40	ns
-	t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{GLQX}	t_{OLZ}(1)(6)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{ELQX}	t_{LZ}(1)(6)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{GHQZ}	t_{DF}(1)(2)	$\overline{OE}$ High to Output High-Z		30		30		30	ns
t_{EHQZ}	t_{HZ}(1)(2)	$\overline{CE}$ High to Output High-Z		30		30		30	ns
t_{PHQV}	t_{PWH}	$\overline{RP}$ High to Output Delay		300		300		300	ns

Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)

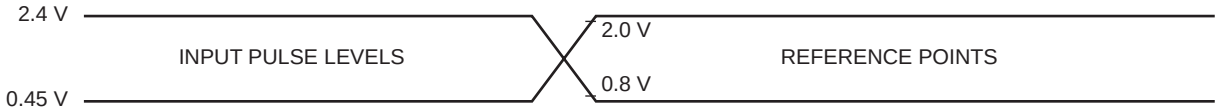

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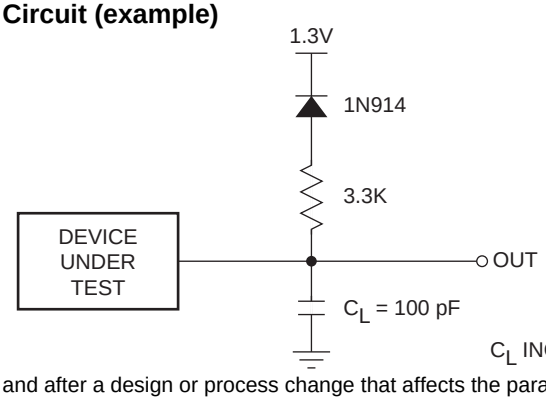
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

V_{CC} = +5V ±10%, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	28F002-90		28F002-12		28F002-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVWH}	t_{AS}	Address Setup to $\overline{WE}$ Going High	50		50		50		ns
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{WE}$ Going High	0		0		0		ns
t_{DVWH}	t_{DS}	Data Setup Time to $\overline{WE}$ Going High	40		40		40		ns
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{WE}$ Going High	0		0		0		ns
t_{ELWL}	t_{CS}	CE Setup Time to $\overline{WE}$ Going Low	0		0		0		ns
t_{WHEH}	t_{CH}	CE Hold Time from $\overline{WE}$ Going High	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{PHWL}	t_{PS}(1)	$\overline{RP}$ to $\overline{WE}$ Going Low	215		215		215		ns
t_{PHHWH}	t_{PHS}(1)	$\overline{RP}$ V_{HH} Setup to $\overline{WE}$ Going High	100		100		100		ns
t_{VPWH}	t_{VPS}(1)	V_{PP} Setup to $\overline{WE}$ Going High	100		100		100		ns
t_{WHQV1}	—	Duration of Programming Operations	6		6		6		µs
t_{WHQV2}	—	Duration of Erase Operations (Boot)	0.3		0.3		0.3		Sec
t_{WHQV3}	—	Duration of Erase Operations (Parameter)	0.3		0.3		0.3		Sec
t_{WHQV4}	—	Duration of Erase Operations (Main)	0.6		0.6		0.6		Sec
t_{QVVL}	t_{VPH}(1)	V_{PP} Hold from Valid Status Reg Data	0		0		0		ns
t_{QVPH}	t_{PHH}(1)	$\overline{RP}$ V_{HH} Hold from Status Reg Data	0		0		0		ns
t_{PHBR}(1)	—	Boot Block Relock Delay		100		100		100	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	28F002-90			28F002-12			28F002-15			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Boot Block Erase Time		1.0	7		1.0	7		1.0	7	Sec
Parameter Block Erase Time		1.0	7		1.0	7		1.0	7	Sec
Main Block Erase Time		2.4	14		2.4	14		2.4	14	Sec
Main Block Program Time		1.2	4.2		1.2	4.2		1.2	4.2	Sec

FUNCTION TABLE(1)

Mode	Pins						Notes
	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	
Signature (MFG)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, A_9 = 12V
Signature (Device)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	7CH-28F002T 7DH-28F002B	$A_0 = V_{IH}$, A_9 = 12V
Write Cycle	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	During Write Cycle
Deep Power Down	V_{IL}	X	X	X	X	HIGH-Z	

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Read Array/Reset	Write	X	FFH				
Program Setup/ Program	Write	A_{IN}	40H 10H	Write	A_{IN}	D_{IN}	
Read Status Reg.	Write	X	70H	Read	X	St. Reg. Data	
Clear Status Reg.	Write	X	50H				
Erase Setup/Erase Confirm	Write	Block ad	20H	Write	Block ad	D0H	
Erase Suspend/ Erase Resume	Write	X	B0H	Write	X	D0H	
Read Sig (Mfg)	Write	X	90H	Read	0000H		31H
Read Sig (Dev)	Write	X	90H	Read	0001H		7CH-28F002T 7DH-28F002B

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

The CAT28F002 memory can be read from any of its Blocks (Boot Block, Main Block or Parameter Block), Status Register and Signature Information by sending the Read Command Mode to the Command Register.

CAT28F002 automatically resets to Read Array mode upon initial device power up or after exit from deep power down. A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{RP}$ and $\overline{WE}$ high. Vpp can be either high or low. The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 18 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of the device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A9 or by sending an instruction to the command register (see Write Operations).

The conventional method is entered as a regular read mode by driving the $\overline{CE}$ and $\overline{OE}$ low (with $\overline{WE}$ high), and applying the required high voltage on address pin A9 while the other address line are held at VIL.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_7 to I/O_0:

Catalyst Code = 0011 0001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_7 to I/O_0:

CAT28F002T = 0111 1100 (7CH)

CAT28F002B = 0111 1101 (7DH)

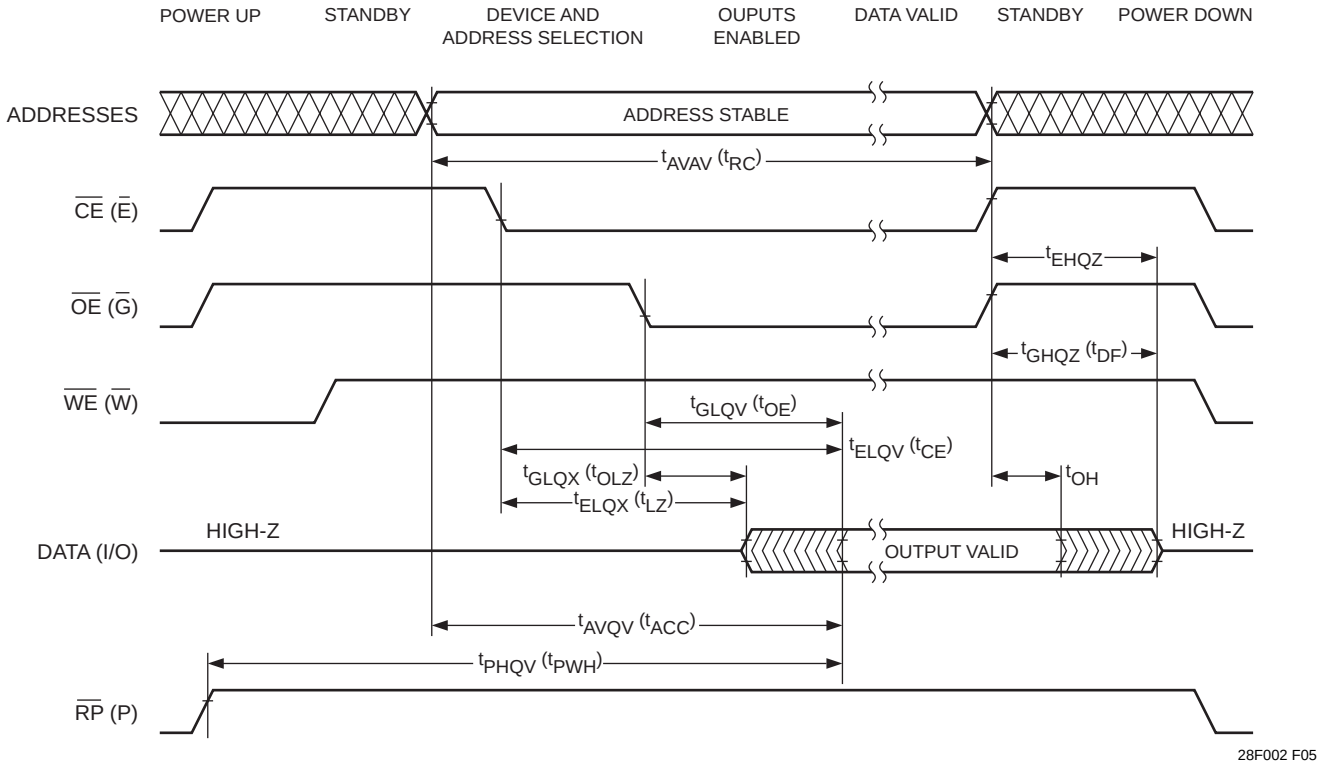
Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F002 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impendance state independent of the $\overline{OE}$ status.

Deep Power-Down

When $\overline{RP}$ is at logic-low level, the CAT28F002 is placed in a Deep Power-Down mode where all the device circuitry are disabled, thereby reducing the power consumption to 0.25µW.

Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Array

The device can be put into a Read Array Mode by initiating a write cycle with FFH on the data bus. The device is also in a standard Read Array Mode after the initial device power up and when comes out of the Deep Power-Down mode.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

Catalyst Code = Catalyst Code = 0011 0001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_7 to I/O_0:

CAT28F002T = 0111 1100 (7CH)
CAT28F002B = 0111 1101 (7DH)

To terminate the operations, it is necessary to write another valid command into the register.

STATUS REGISTER

The 28F002 contains an 8-bit Status Register. The Status Register is polled to check for write or erase completion or any related errors. The Status Register may be read at any time by issuing a Read Status Register (70H) command. All subsequent read operations output data from the Status Register, until another valid command is issued. The contents of the Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle. $\overline{OE}$ or $\overline{CE}$ must be toggled to VIH before further reads to update the status register latch.

The Erase Status (SR.5) and Program Status (SR.4) are set to 1 by the WSM and can only be reset issuing Clear Status Register (50H) These two bits can be polled for failures, thus allowing more flexibility to the designer when using the CAT28F002. Also, VPP Status (SR.3) when set to 1 must be reset by system software before any further byte programs or block erases are attempted.

ERASE SETUP/ERASE CONFIRM

Erase is executed one block at a time, initiated by a two cycle command sequence. The two cycle command sequence provides added security against accidental block erasure. During the first write cycle, a Command 20H (Erase Setup) is first written to the Command Register, followed by the Command D0H (Erase Confirm). These commands require both appropriate command data and an address within Block to be erased. Also, Block erasure can only occur when VPP= VPPH.

Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After receiving the two command erase sequence the CAT28F002 automatically outputs Status Register data when read (Fig.5). The CPU can detect the completion of the erase event by checking if the SR.7 of the Status Register is set.

SR.5 will indicate whether the erase was successful. If an erase error is detected, the Status Register should be cleared. The device will be in the Status Register Read Mode until another command is issued.

ERASE SUSPEND/ERASE RESUME

The Erase Suspend Command allows erase sequence interruption in order to read data from another block of memory. Once the erase sequence is started, writing the Erase Suspend command (B0H) to the Command Register requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The CAT28F002 continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to “1s”).

The device may now be given a Read ARRAY Command, which allows any locations 'not within the block being erased' to be read. Also, you can either perform a Read Status Register or resume the Erase Operation by sending Erase Resume (D0H), at which time the WSM will continue with the erase sequence. The Erase Suspend Status and WSM Status bits of the Status Register will be cleared.

PROGRAM SETUP/PROGRAM COMMANDS

Programming is executed by a two-write sequence. The program Setup command (40H) is written to the Command Register, followed by a second write specifying the address and data (latched on the rising edge of $\overline{WE}$) to be programmed. The WSM then takes over, controlling the program and verify algorithms internally. After the two-command program sequence is written to it, the CAT28F002 automatically outputs Status Register data when read (see figure 4; Byte Program Flowchart). The CPU can detect the completion of the program event by analyzing the WSM Status bit of the Status Register. Only the Read Status Register Command is valid while programming is active.

WSMS	ESS	ES	PS	VPPS	R	R	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy
SR.6 = ERASE SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed
SR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase
SR.4 = PROGRAM STATUS
1 = Error in Byte Program
0 = Successful Byte Program
SR.3 = VPP STATUS
1 = V_{PP} Low Detect; Operation Abort
0 = V_{PP} Okay
SR.2 -SR.0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use and should be masked out when polling the Status Register.

NOTES:
The Write State Machine Status Bit must first be checked to determine program or erase completion, before the Program or Erase Status bits are checked for success.
If the Program AND Erase Status bits are set to "1s" during an erase attempt, an improper command sequence was entered. Attempt the operation again.
If V_{PP} low status is detected, the Status Register must be cleared before another program or erase operation is attempted.
The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the program or erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

When the Status Register indicates that programming is complete, the Program Status bit should be checked. If program error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1s" that do not successfully program to "0s". The Command Register remains in Read Status Register mode until further commands are issued to it.

If erase/byte program is attempted while $V_{PP} = V_{PPL}$, the Status bit (SR.5/SR.4) will be set to "1". Erase/Program attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

EMBEDDED ALGORITHMS

The CAT28F002 integrates the Quick Pulse programming algorithm on-chip, using the Command Register, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor-like interface timings to the Command and Status Registers. WSM operation, internal program verify, and V_{PP} high voltage presence are monitored and reported via appropriate Status Register bits. Figure 4 shows a system software flowchart for device programming.

As above, the Quick Erase algorithm is now implemented internally, including all preconditioning of block data. WSM operation, erase verify and V_{PP} high voltage presence are monitored and reported through the Status Register. Additionally, if a command other than Erase Confirm is written to the device after Erase Setup has been written, both the Erase Status and Program Status bits will be set to "1". When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 5 shows a system software flowchart for block erase.

The entire sequence is performed with V_{PP} at V_{PPH}. Abort occurs when $\overline{RP}$ transitions to V_{IL}, or V_{PP} drops to V_{PPL}. Although the WSM is halted, byte data is partially programmed or Block data is partially erased at the location where it was aborted. Block erasure or a repeat of byte programming will initialize this data to a known value.

BOOT BLOCK PROGRAM AND ERASE

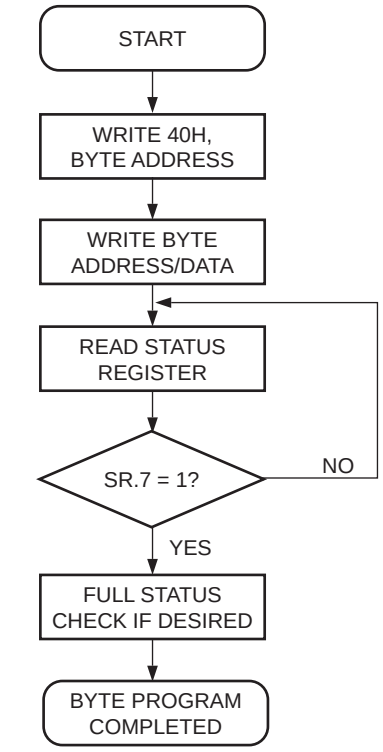
The boot block is intended to contain secure code which will minimally bring up a system and control programming and erase of other blocks of the device, if needed. Therefore, additional "lockout" protection is provided to guarantee data integrity. Boot block program and erase operations are enabled through high voltage V_{HH} on either $\overline{RP}$ or $\overline{OE}$, and the normal program and erase command sequences are used. Reference the AC Waveforms for Program/Erase.

If boot block program or erase is attempted while $\overline{RP}$ is at V_{IH}, either the Program Status or Erase Status bit will be set to "1", reflective of the operation being attempted and indicating boot block lock. Program/erase attempts while $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

IN-SYSTEM OPERATION

For on-board programming, the $\overline{RP}$ pin is the most convenient means of altering the boot block. Before issuing Program or Erase confirms commands, $\overline{RP}$ must transition to V_{HH}. Hold $\overline{RP}$ at this high voltage throughout the program or erase interval (until after Status Register confirm of successful completion). At this time, it can return to V_{IH} or V_{IL}.

Figure 4 Byte Programming Flowchart



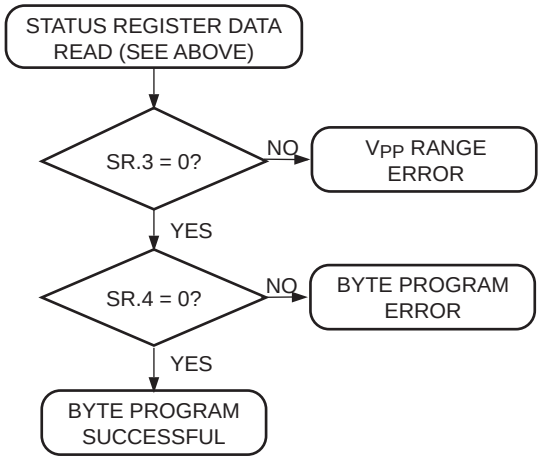
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H Address = Bytes to be Programmed
Write	Program	Data to be programmed Address = Byte to be Programmed
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register Check SR.7
Standby		1 = Ready, 0 = Busy

Repeat for subsequent bytes.

Full Status check can be done after each byte or after a sequence of bytes.

Write FFH after the last byte programming operation to reset the device to Read Array Mode.

FULL STATUS CHECK PROCEDURE



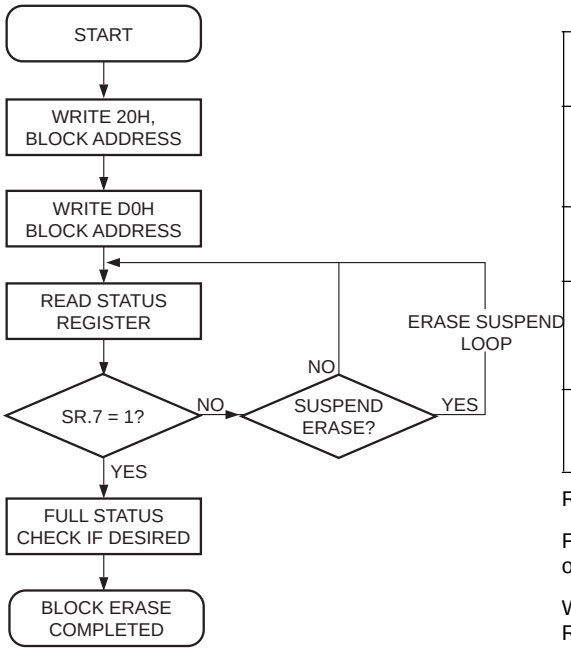
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.3 1 = Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.3 is only cleared by the Clear Status Register Command, in case where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 5 Block Erase Flowchart



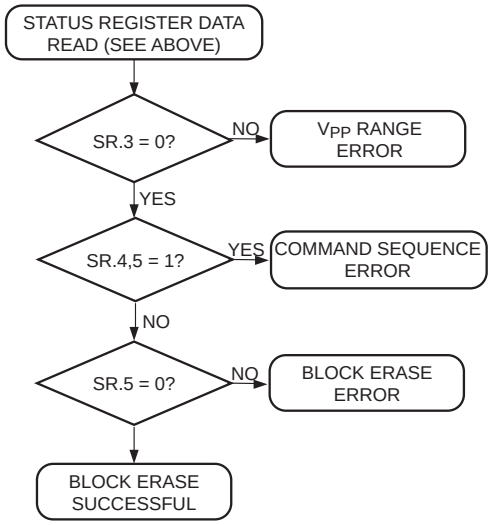
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Address = Within Block to be erased
Write	Erase	Data - D0H Address = Within Block to be erased
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.7 1 = Ready, 0 = Busy

Repeat for subsequent blocks.

Full Status check can be done after each block or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to Read Array Mode.

FULL STATUS CHECK PROCEDURE



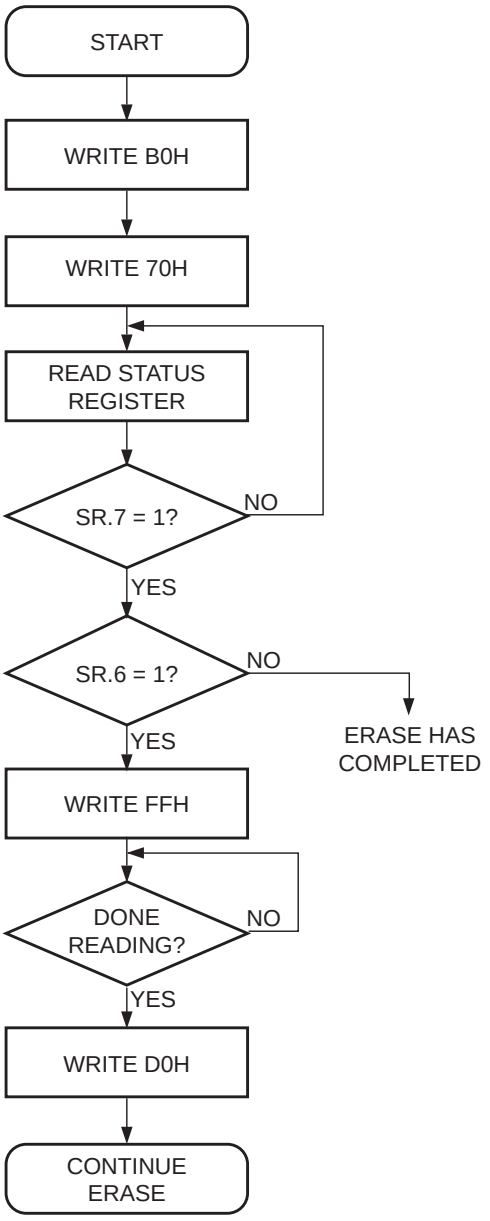
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a erase attempt, before further attempts are allowed by the Write State Machine.

SR.3 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

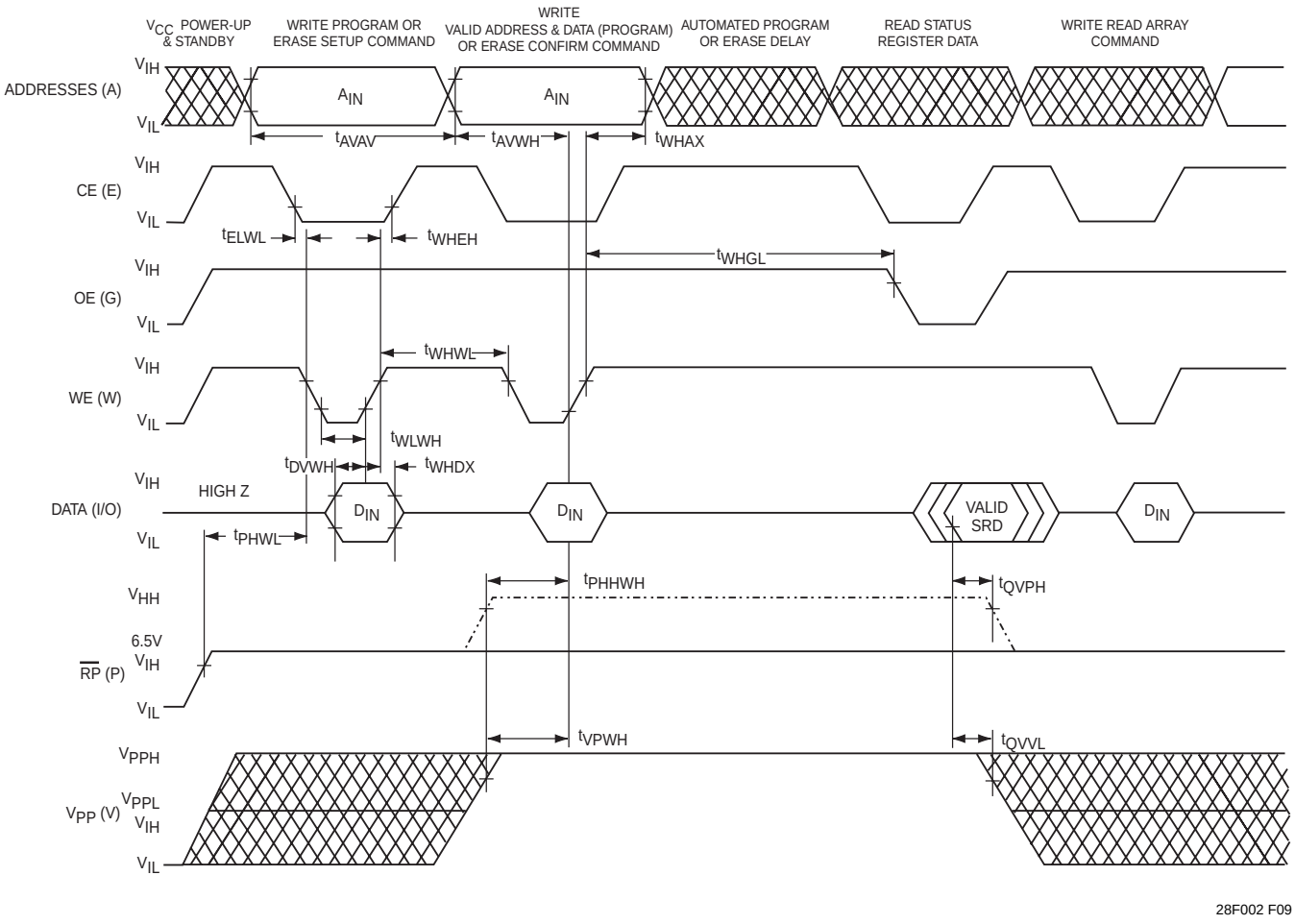
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6 Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Erase Status Register	Data = 70H
Standby/ Ready		Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to Update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

Figure 7. A.C. Timing for Program/Erase Operation



POWER UP/DOWN PROTECTION

The CAT28F002 offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F002 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

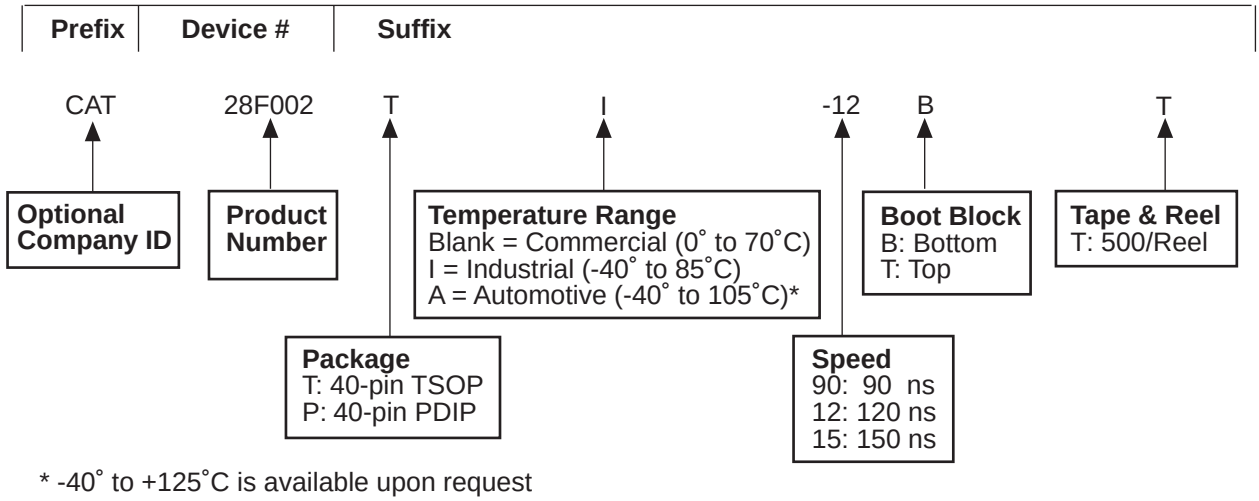
ALTERNATE $\overline{CE}$-CONTROLLED WRITES

V_{CC} = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F002-90		28F002-12		28F002-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	90		120		150		ns
t_{AVEH}	t_{AS}	Address Setup to $\overline{CE}$ Going High	50		50		50		ns
t_{EHAX}	t_{AH}	Address Hold Time from $\overline{CE}$ Going High	0		0		0		ns
t_{DVEH}	t_{DS}	Data Setup Time to $\overline{CE}$ Going High	40		40		40		ns
t_{EHDX}	t_{DH}	Data Hold Time from $\overline{CE}$ Going High	0		0		0		ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time to $\overline{CE}$ Going Low	0		0		0		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time from $\overline{CE}$ Going High	0		0		0		ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	50		50		50		ns
t_{EHEL}	t_{EPH}	$\overline{CE}$ Pulse Width High	30		30		30		ns
t_{PHEL}	t_{PS}(1)	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	215		215		215		ns
t_{PHHEH}	t_{PHS}(1)	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going High	100		100		100		ns
t_{VPEH}	t_{VPS}(1)	V_{PP} Setup to $\overline{CE}$ Going High	100		100		100		ns
t_{EHQV1}	—	Duration of Programming Operations	6		6		6		µs
t_{EHQV2}	—	Duration of Erase Operations (Boot)	0.3		0.3		0.3		Sec
t_{EHQV3}	—	Duration of Erase Operations (Parameter)	0.3		0.3		0.3		Sec
t_{EHQV4}	—	Duration of Erase Operations (Main)	0.6		0.6		0.6		Sec
t_{QVVL}	t_{VPH}(1)	V_{PP} Hold from Valid Status Reg Data	0		0		0		ns
t_{QVPH}	t_{PHH}(1)	$\overline{RP}$ V_{HH} Hold from Status Reg Data	0		0		0		ns
t_{PHBR}(1)	—	Boot Block Relock Delay		100		100		100	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ORDERING INFORMATION



* -40˚ to +125˚C is available upon request

28F002 F13

Note:

(1) The device used in the above example is a CAT28F002TI-12BT (TSOP, Industrial Temperature, 120ns access time, Bottom Boot Block, Tape & Reel)