CAT9554, CAT9554A

8-bit I²C and SMBus I/O Port with Interrupt

FEATURES

- 400kHz I²C bus compatible*
- 2.3V to 5.5V operation
- Low stand-by current
- 5V tolerant I/Os
- 8 I/O pins that default to inputs at power-up
- High drive capability
- Individual I/O configuration
- Polarity inversion register
- Active low interrupt output
- Internal power-on reset
- No glitch on power-up
- Noise filter on SDA/SCL inputs
- Cascadable up to 8 devices
- Industrial temperature range
- RoHS-compliant 16-lead SOIC and TSSOP, and 16-pad TQFN (4 x 4 mm) packages

APPLICATIONS

- White goods (dishwashers, washing machines)
- Handheld devices (cell phones, PDAs, digital cameras)
- Data Communications (routers, hubs and servers)

DESCRIPTION

The CAT9554 and CAT9554A are CMOS devices that provide 8-bit parallel input/output port expansion for I²C and SMBus compatible applications. These I/O expanders provide a simple solution in applications where additional I/Os are needed: sensors, power switches, LEDs, pushbuttons, and fans.

The CAT9554/9554A consist of an input port register, an output port register, a configuration register, a polarity inversion register and an I²C/SMBus-compatible serial interface.

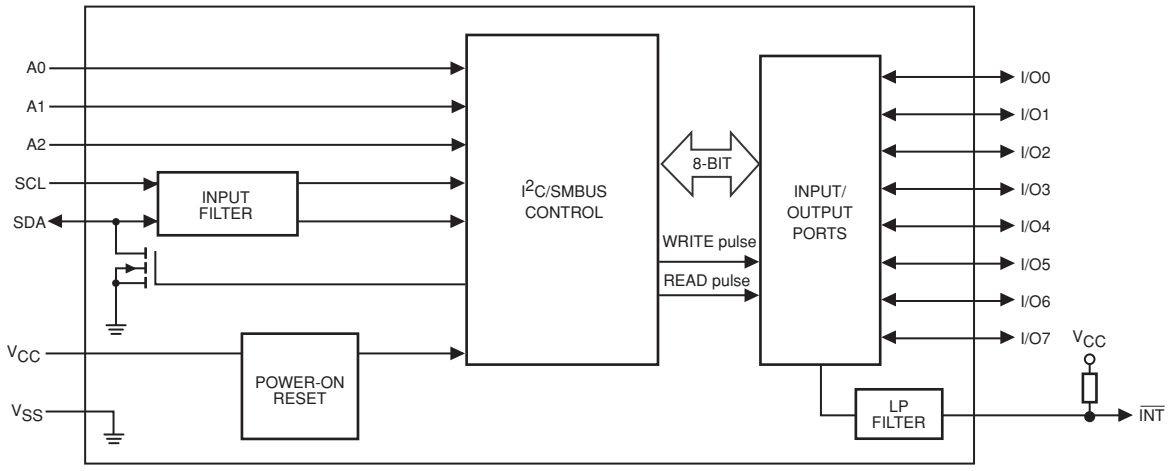
Any of the eight I/Os can be configured as an input or output by writing to the configuration register. The system master can invert the CAT9554/9554A input data by writing to the active-high polarity inversion register.

The CAT9554/9554A features an active low interrupt output which indicates to the system master that an input state has changed.

The device's extended addressing capability allows up to 8 devices to share the same bus. The CAT9554A is identical to the CAT9554 except the fixed part of the I²C slave address is different. This allows up to 16 of devices (eight CAT9554 and eight CAT9554A) to be connected on the same bus.

For Ordering Information details, see page 15.

BLOCK DIAGRAM



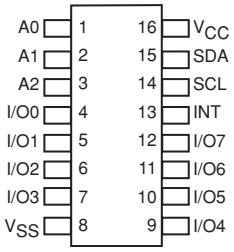
NOTE: ALL I/Os ARE SET TO INPUTS AT RESET

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

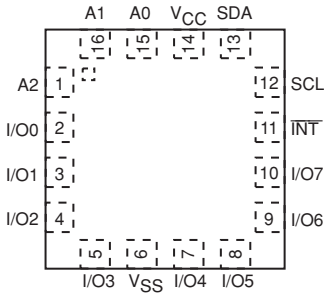
Doc. No. 25088, Rev. B

PIN CONFIGURATION

SOIC (W)
TSSOP (Y)



TQFN (HV4)



4 x 4 mm
Top View

PIN DESCRIPTION

SOIC / TSSOP	TQFN	PIN NAME	FUNCTION
1	15	A_0	Address Input 0
2	16	A_1	Address Input 1
3	1	A_2	Address Input 2
4-7	2-5	I/O_{0-3}	Input/Output Port 0 to Input/Output Port 3
8	6	V_{SS}	Ground
9-12	7-10	I/O_{4-7}	Input/Output Port 4 to Input/Output Port 7
13	11	INT	Interrupt Output (open drain)
14	12	SCL	Serial Clock
15	13	SDA	Serial Data
16	14	V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} with Respect to Ground ..... –0.5V to +6.5V

Voltage on Any Pin with Respect to Ground ..... –0.5V to +5.5V

DC Current on I/O_0 to I/O_7 ..... ±50 mA

DC Input Current ..... ±20 mA

V_{CC} Supply Current 85mA

V_{SS} Supply Current 100mA

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Junction Temperature ..... +150°C

Storage Temperature ..... -65°C to +150°C

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
VZAP(2)	ESD Susceptibility	JEDEC Standard JESD 22	2000	Volts
ILTH(2)(3)	Latch-up	JEDEC Standard 17	100	mA

Notes:
(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
(2) This parameter is tested initially and after a design or process change that affects the parameter.
(3) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

V_{CC} = 2.3 to 5.5 V; T_A = -40°C to +85°C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CC}	Supply voltage		2.3	—	5.5	V
I_{CC}	Supply current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	—	104	175	µA
I_{stbl}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	550	700	µA
I_{stbh}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{CC}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{CC}$ or V_{SS}	—	1.5	1.65	V
SCL, SDA, $\overline{INT}$						
V_{IL} (1)	Low level input voltage		-0.5	—	0.3 V_{CC}	V
V_{IH} (1)	High level input voltage		0.7 V_{CC}	—	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4V	3	—	—	mA
I_L	Leakage current	$V_I = V_{CC}$ or V_{SS}	– 1	—	+1	µA
C_I (2)	Input capacitance	$V_I = V_{SS}$	—	—	6	pF
C_O (2)	Output capacitance	$V_O = V_{SS}$	—	—	8	pF
A_0, A_1, A_2						
V_{IL} (1)	Low level input voltage		-0.5	—	0.8	V
V_{IH} (1)	High level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		-1	—	1	µA
I/Os						
V_{IL}	Low level input voltage		-0.5	—	0.8	V
V_{IH}	High level input voltage		2.0	—	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.5 V; V_{CC} = 2.3 V; (3)	8	10	—	mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V; (3)	10	13	—	mA
		V_{OL} = 0.5 V; V_{CC} = 4.5 V; (3)	8	17	—	mA
		V_{OL} = 0.7 V; V_{CC} = 4.5 V; (3)	10	24	—	mA
		V_{OL} = 0.5 V; V_{CC} = 3.0 V; ((3)	8	14	—	mA
		V_{OL} = 0.7 V; V_{CC} = 3.0 V; (3)	10	19	—	mA
V_{OH}	High level output voltage	I_{OH} = – 8 mA; V_{CC} = 2.3 V; (4)	1.8	—	—	V
		I_{OH} = – 10 mA; V_{CC} = 2.3 V; (4)	1.7	—	—	V
		I_{OH} = – 8 mA; V_{CC} = 3.0 V; (4)	2.6	—	—	V
		I_{OH} = – 10 mA; V_{CC} = 3.0 V; (4)	2.5	—	—	V
		I_{OH} = – 8 mA; V_{CC} = 4.75 V; (4)	4.1	—	—	V
		I_{OH} = – 10 mA; V_{CC} = 4.75 V; (4)	4.0	—	—	V
I_{IH}	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$	—	—	1	µA
I_{IL}	Input leakage current	V_{CC} = 5.5 V; $V_I = V_{SS}$	—	—	-100	µA
C_I (2)	Input capacitance		—	—	5	pF
C_O (2)	Output capacitance		—	—	8	pF

Notes:
1. V_{IL} min and V_{IH} max are reference values only and are not tested.
2. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
3. The total current sunk by all I/Os must be limited to 100 mA and each I/O limited to 25 mA maximum.
4. The total current sourced by all I/Os must be limited to 85 mA.

A.C. CHARACTERISTICS

V_{CC} = 2.3V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified(1).

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency		400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)		50	ns
t_{LOW}	Clock Low Period	1.3		µs
t_{HIGH}	Clock High Period	0.6		µs
t_R(2)	SDA and SCL Rise Time	20	300	ns
t_F(2)	SDA and SCL Fall Time	20	300	ns
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start)	0.6		µs
$t_{HD:DAT}$	Data Input Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{AA}	SCL Low to Data Out Valid		900	ns
t_{DH}	Data Out Hold Time	50		ns
t_{BUF}(2)	Time the Bus must be Free Before a New Transmission Can Start	1.3		µs
Port Timing				
t_{PV}	Output Data Valid		200	ns
t_{PS}	Input Data Setup Time	100		ns
t_{PH}	Input Data Hold Time	1		µs
Interrupt Timing				
t_{IV}	Interrupt Valid		4	µs
t_{IR}	Interrupt Reset		4	µs

Notes:
1. Test conditions according to "AC Test Conditions" table.
2. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

AC TEST CONDITIONS

Input Rise and Fall time	< = 10ns
CMOS Input Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
CMOS Input Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
TTL Input Voltages	0.4V to 2.4V
TTL Input Reference Voltages	0.8V, 2.0V
Output Reference Voltages	$0.5V_{CC}$
Output Load: SDA, INT	Current Souce I_{OL} = 3mA; C_L = 100pF
Output Load: I/Os	Current Source: I_{OL}/I_{OH} = 10mA; C_L = 50pF

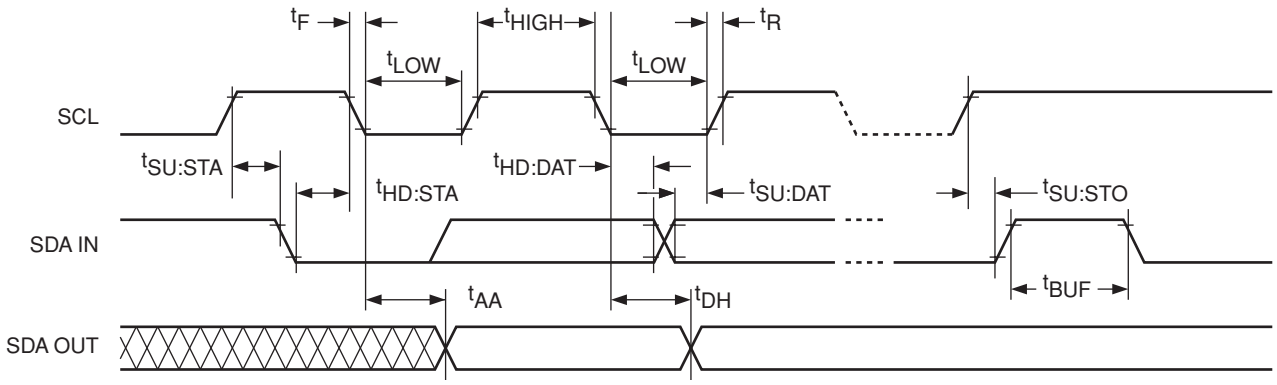


Figure 1. 2-Wire Serial Interface Timing

PIN DESCRIPTION

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull-up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs. A pull-up resistor must be connected from SDA line to Vcc. The value of the pull-up resistor, R_P, can be calculated based on minimum and maximum values from Figure 2 and Figure 3 (see Note).

A_0, A_1, A_2: Device Address Inputs

These inputs are used for extended addressing capability. The A_0, A_1, A_2 pins should be hardwired to V_{CC} or V_{SS}. When hardwired, up to eight CAT9554/9554As may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A_2, A_1, A_0, from the slave address byte.

I/O_0 to I/O_7: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/O_0 to I/O_7 is shown in Figure 4. When an I/O is configured as an input, the Q1 and Q2 output transistors are off creating a high impedance input with a weak pull-up resistor (typical 100 kΩ). If the I/O pin is configured as an output, the push-pull output stage is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either V_{CC} or V_{SS}.

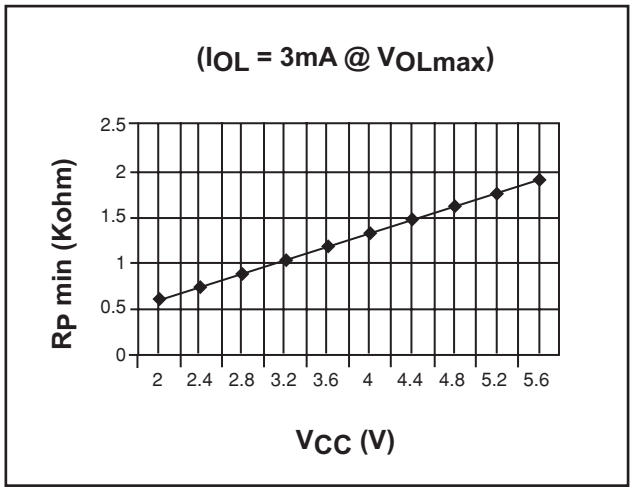


Figure 2. Minimum R_P Value versus Supply Voltage

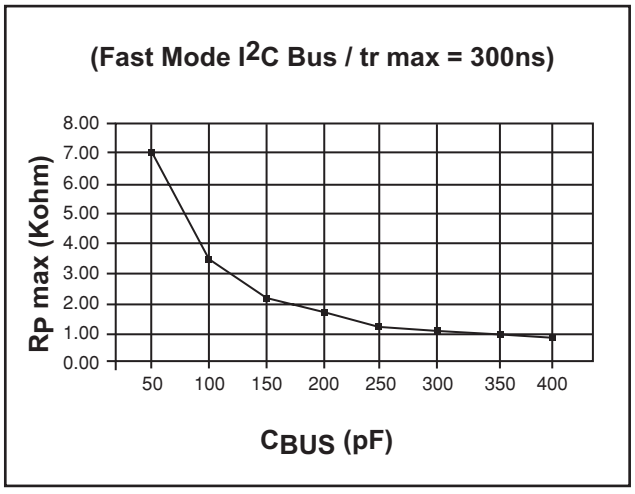


Figure 3. Maximum R_P Value versus Bus Capacitance

Note: According to the Fast Mode I^2C bus specification, for bus capacitance up to 200pF, the pull up device can be a resistor. For bus loads between 200pF and 400pF, the pull-up device can be a current source (Imax = 3mA) or a switched resistor circuit.

INT: Interrupt Output

The open-drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read. Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

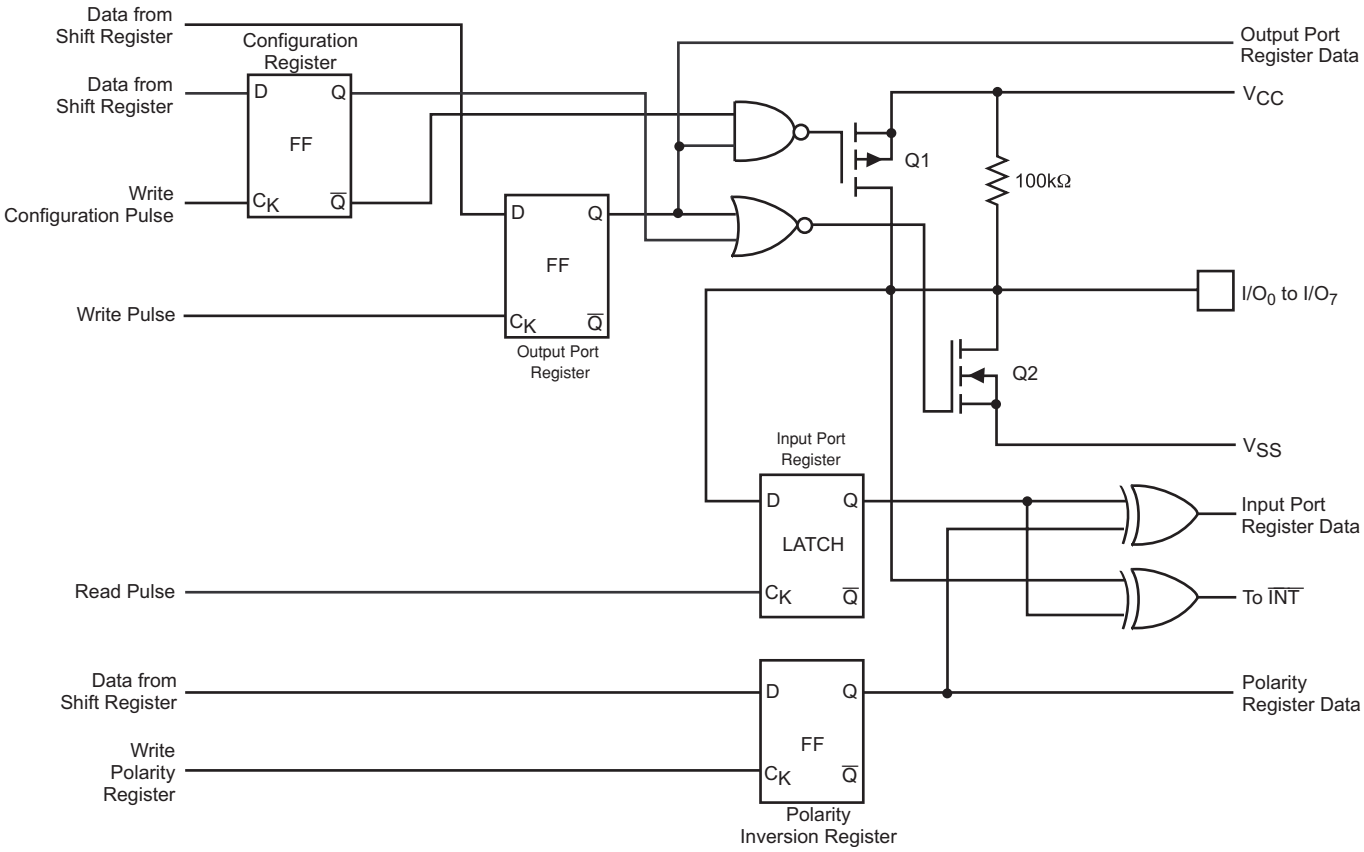


Figure 4. Simplified Schematic of I/O_0 to I/O_7

FUNCTIONAL DESCRIPTION

The CAT9554 and CAT9554A general purpose input/output (GPIO) peripherals provide up to eight I/O ports, controlled through an I²C compatible serial interface

The CAT9554/54A support the I²C Bus data transmission protocol. This I²C Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9554/9554A operate as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I²C Bus Protocol

The features of the I²C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 5).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9554/9554A monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9554/9554A for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 for the CAT9554 (Figure 6) and as 0111 for the CAT9554A (Figure 7). The CAT9554/9554A uses the next three bits as address bits.

The address bits A_2, A_1 and A_0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7-bit slave address is the R/W bit that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the CAT9554/9554A monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9554/9554A then performs a read or a write operation depending on the state of the R/W bit.

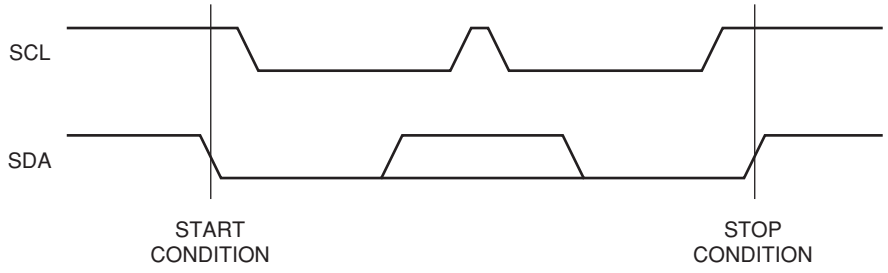


Figure 5. START/STOP Conditions

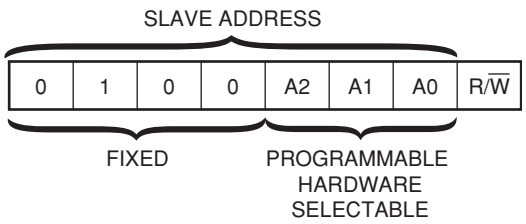


Figure 6. CAT9554 Slave Address

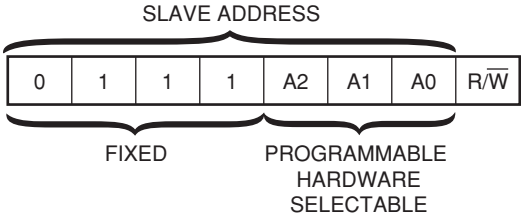


Figure 7. CAT9554A Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 5).

The CAT9554/9554A respond with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT9554/9554A begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9554/9554A will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a STOP condition to return the CAT9554/9554A to the standby power mode and place the device in a known state.

Registers and Bus Transactions

The CAT9554/9554A consist of an input port register, an output port register, a polarity inversion register and a configuration register. Table 1 shows the register address table. Tables 2 to 5 list Register 0 through Register 3 information.

Table 1. Register Command Byte

Command (hex)	Protocol	Function
0x00	Read byte	Input port register
0x01	Read/write byte	Output port register
0x02	Read/write byte	Polarity inversion register
0x03	Read/write byte	Configuration register

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 2. Register 0 – Input Port Register

bit	I7	I6	I5	I4	I3	I2	I1	I0
default	1	1	1	1	1	1	1	1

Table 3. Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	1	1	1	1	1	1	1	1

Table 4. Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	0	0	0	0	0	0	0	0

Table 5. Register 3 – Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

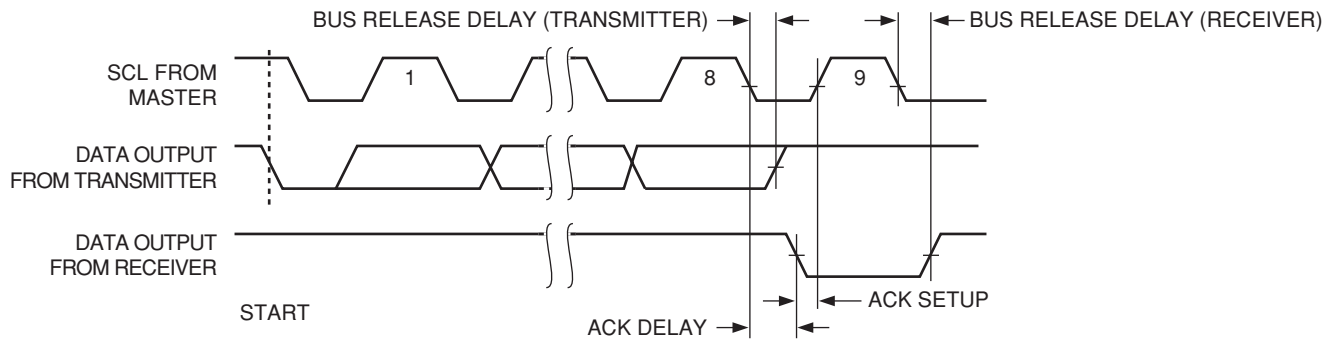


Figure 8. Acknowledge Timing

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip-flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set ("1") the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared ("0"), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power-up, the I/Os are configured as inputs with a weak pull-up resistor to V_{CC}.

Data is transmitted to the CAT9554/9554A registers using the write mode shown in Figure 9 and Figure 10.

The CAT9554/9554A registers are read according to the timing diagrams shown in Figure 11 and Figure 12. Once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte will be sent.

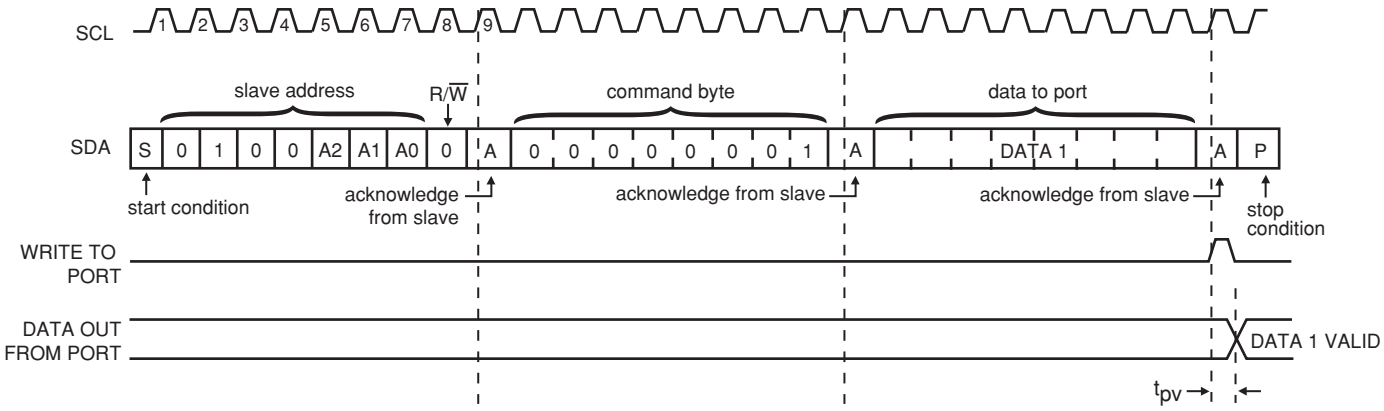


Figure 9. Write to Output Port Register

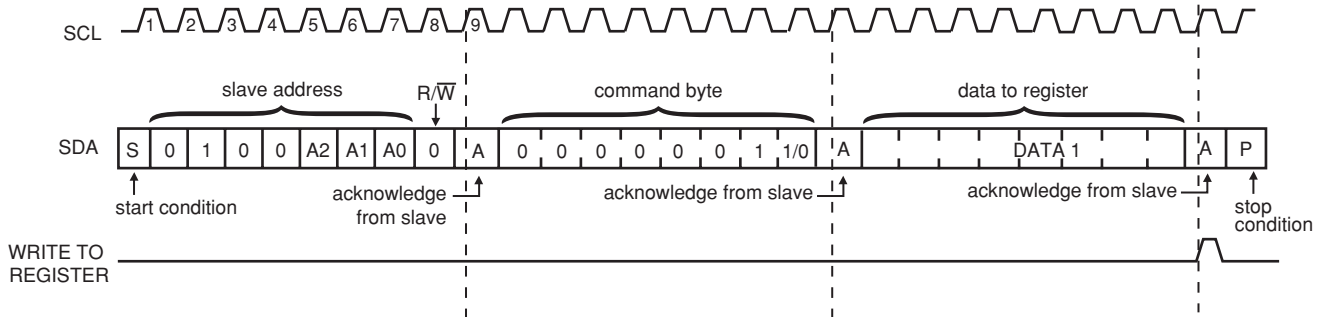


Figure 10. Write to Configuration or Polarity Inversion Register

Power-On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power-on reset pulse holds the CAT9554/9554A in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset condition is released and the internal state machine and the CAT9554/9554A registers are initialized to their default state.

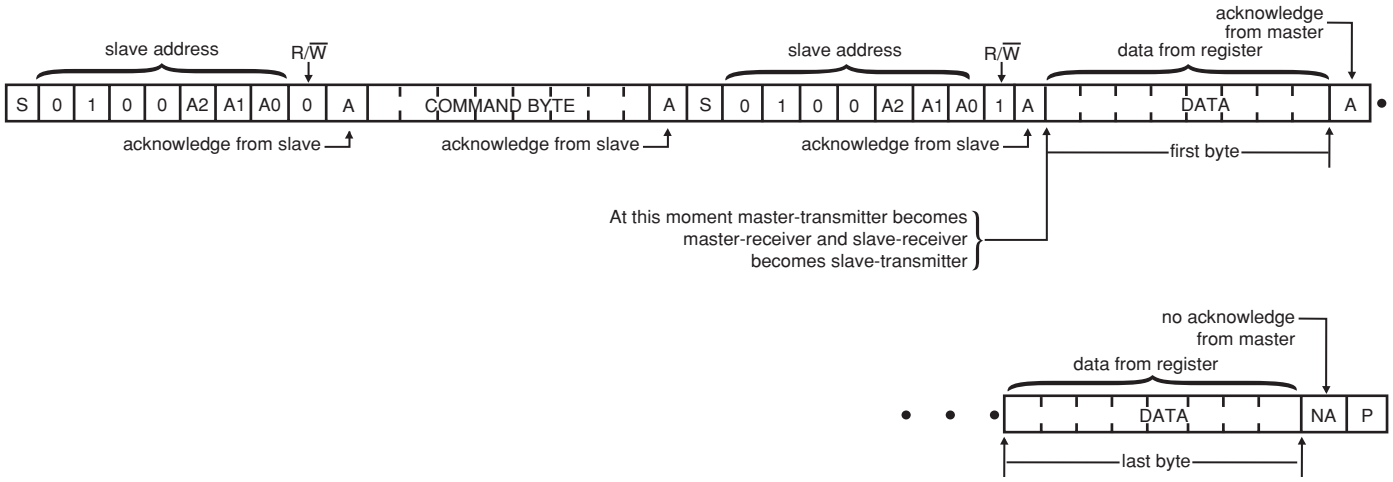


Figure 11. Read from Register

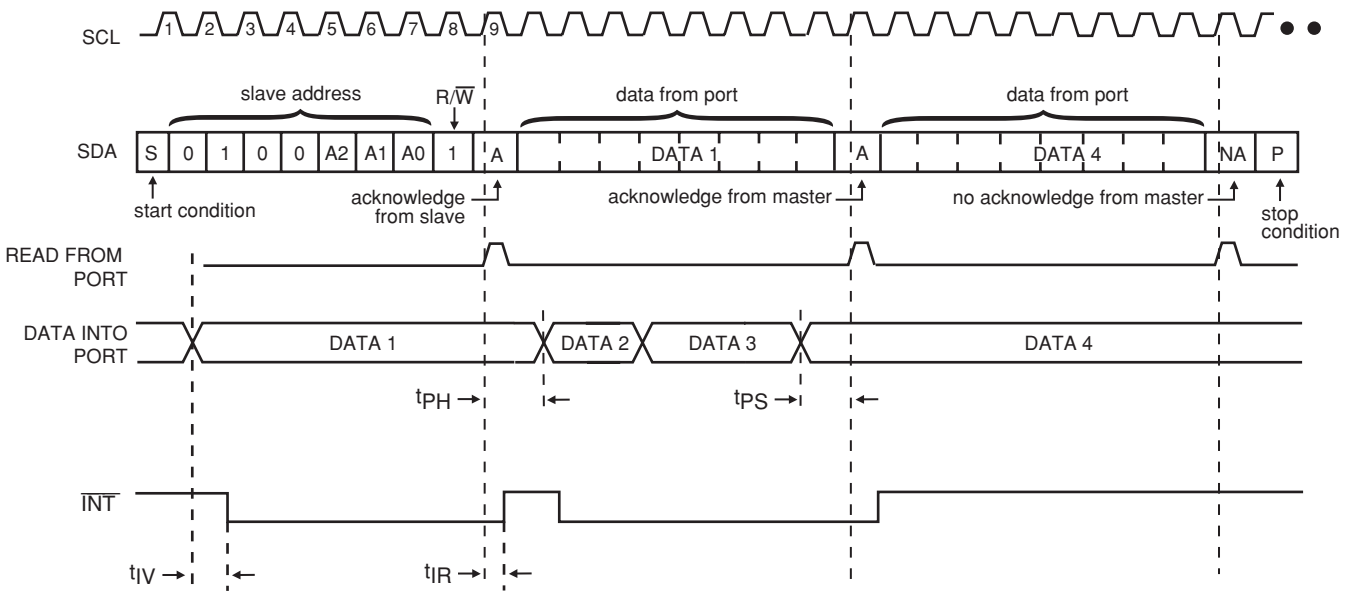
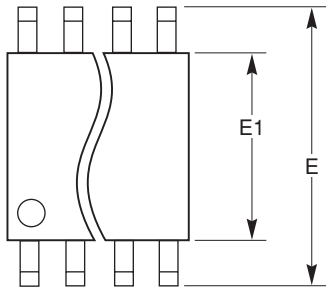
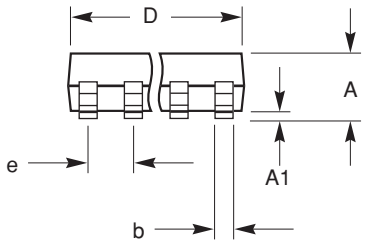


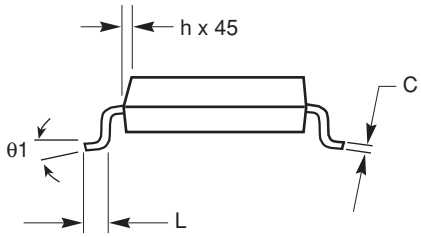
Figure 12. Read Input Port Register

PACKAGE DRAWINGS

16-LEAD 150 MIL WIDE SOIC (W)







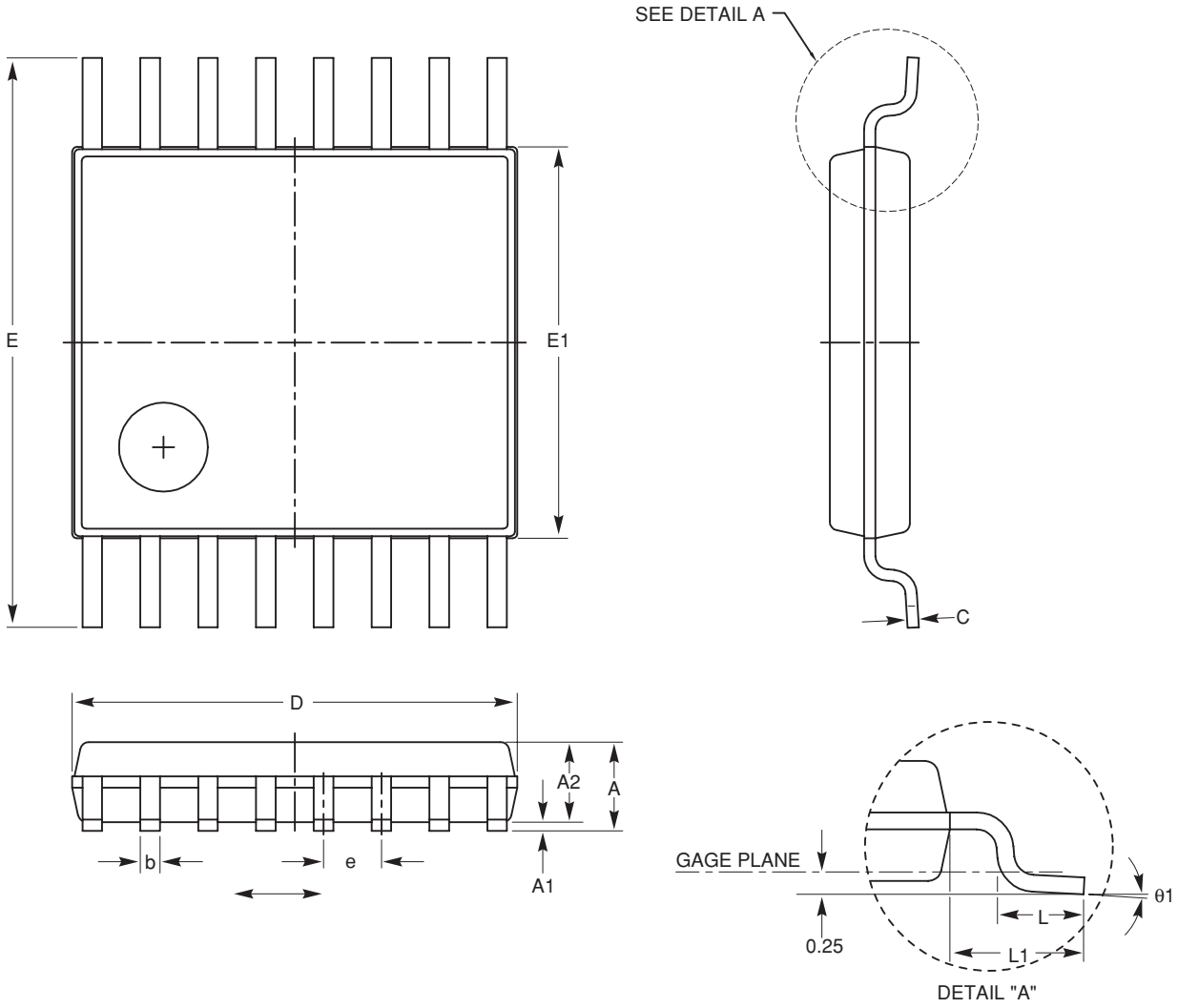
SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ1	0°		8°

16-Lead_SOIC.eps

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-013.

PACKAGE DRAWINGS

16-LEAD TSSOP (Y)

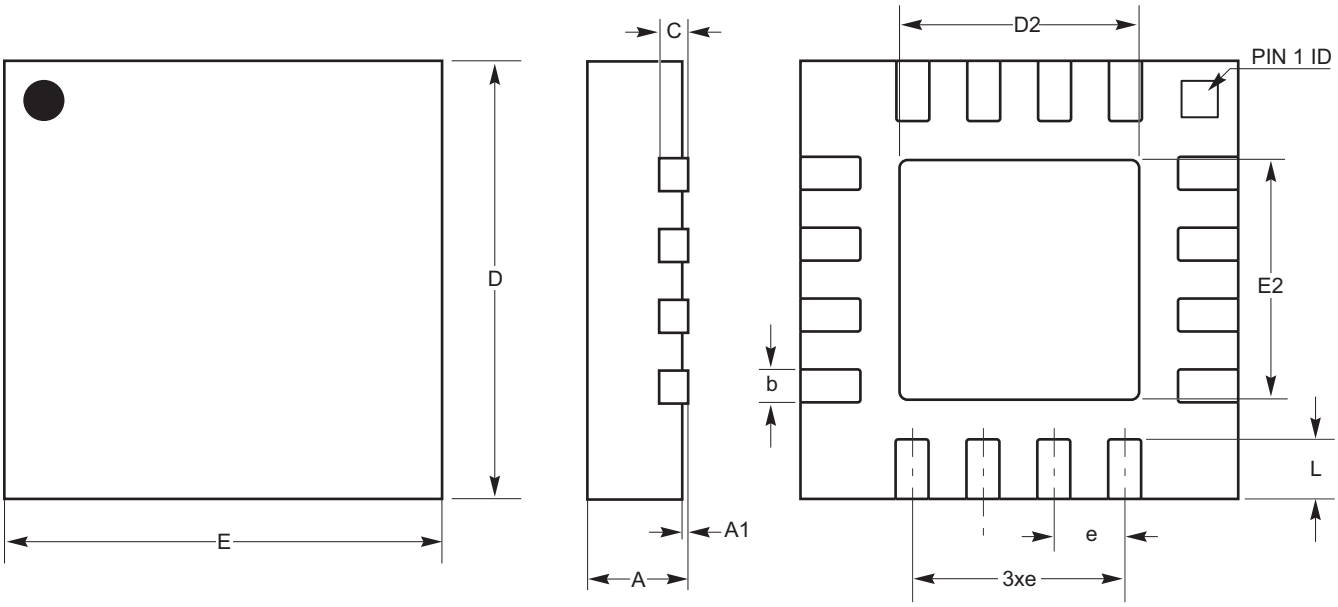


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ1	0.00		8.00

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC specification MO-153.

PACKAGE DRAWINGS

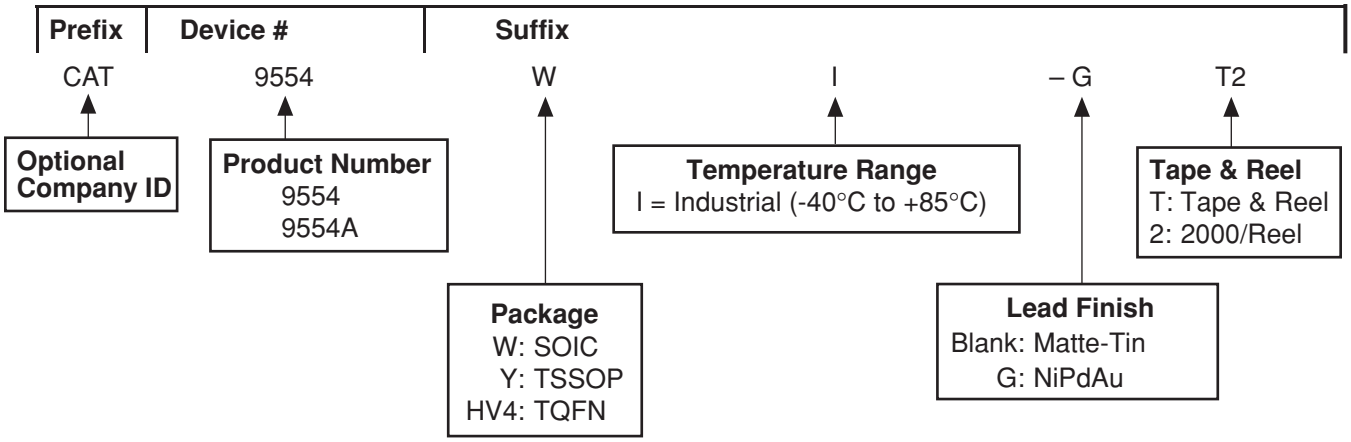
16-PAD TQFN (4 x 4 mm)
(HV4)



SYMBOL	MIN	MIN	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
C		0.20 REF	
D	3.95	4.00	4.05
D2	2.15	2.20	2.25
e		0.65 BSC	
E	3.95	4.00	4.05
E2	2.15	2.20	2.25
L	0.50	0.55	0.60

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC specification MO-229.

ORDERING INFORMATION



Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu pre-plated on SOIC and TSSOP packages and Matte-Tin on TQFN packages.
(3) The device used in the above example is a CAT9554WI-GT2 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).
(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

Ordering Part Number	Package	Lead Finish
CAT9554WI-G	SOIC	NiPdAu
CAT9554WI-GT2	SOIC	NiPdAu
CAT9554YI-G	TSSOP	NiPdAu
CAT9554YI-GT2	TSSOP	NiPdAu
CAT9554HV4I	TQFN	Matte-Tin
CAT9554HV4I-T2	TQFN	Matte-Tin

Ordering Part Number	Package	Lead Finish
CAT9554AWI-G	SOIC	NiPdAu
CAT9554AWI-GT2	SOIC	NiPdAu
CAT9554AYI-G	TSSOP	NiPdAu
CAT9554AYI-GT2	TSSOP	NiPdAu
CAT9554AHV4I	TQFN	Matte-Tin
CAT9554AHV4I-T2	TQFN	Matte-Tin

REVISION HISTORY

Date	Rev.	Comments
07/08/2005	A	Initial Issue
06/28/2006	B	Update Features Add Applications Update Descriptions Update Pin Description Table Update Absolute Maximum Ratings Update D.C Operating Characteristics Update A.C Characteristics Update AC Test Conditions Update Pin Description Update Figure 2, Figure 4, Figure 5, Figure 8 and Figure 12 Update Functional Description Update Package Drawings Update Ordering Information

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