

CD40160B, CD40161B, CD40162B, CD40163B Types

CMOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

CD40160B – Decade with Asynchronous Clear

CD40161B – Binary with Asynchronous Clear

CD40162B – Decade with Synchronous Clear

CD40163B – Binary with Synchronous Clear

■ CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the CLEAR input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the CLEAR input sets all four outputs low regardless of the state of the CLOCK, LOAD, or ENABLE inputs. A low level at the LOAD input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a

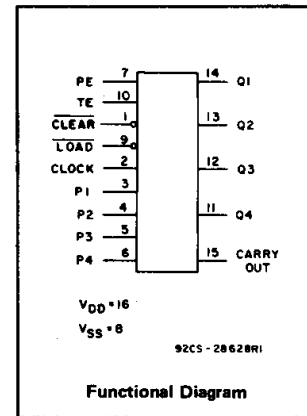
Features:

- Internal look-ahead for fast counting
- Carry output for cascading
- Synchronously programmable
- Clear asynchronous input (CD40160B, CD40161B)
- Clear synchronous input (CD40162B, CD40163B)
- Synchronous load control input
- Low-power TTL compatibility
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V
2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix). The CD40161B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.



Applications:

- Programmable binary and decade counting
- Counter control/timers
- Frequency dividing

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|-------------------------------------------------------------------------|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | |
| Voltages referenced to V _{SS} Terminal) | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +285°C |

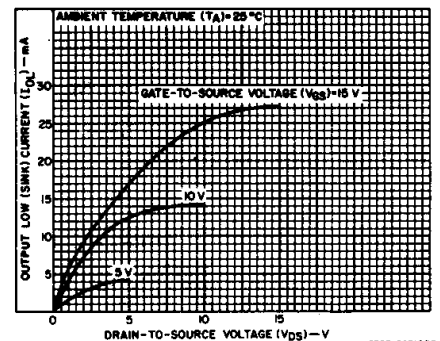


Fig. 1— Typical output low (sink) current characteristics.

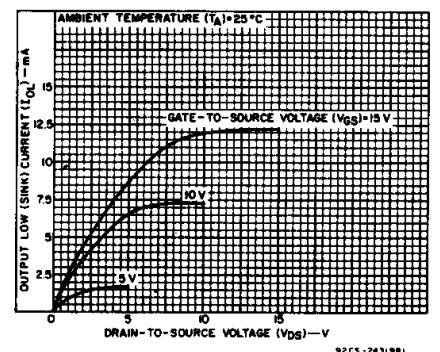


Fig. 2— Minimum output low (sink) current characteristics.

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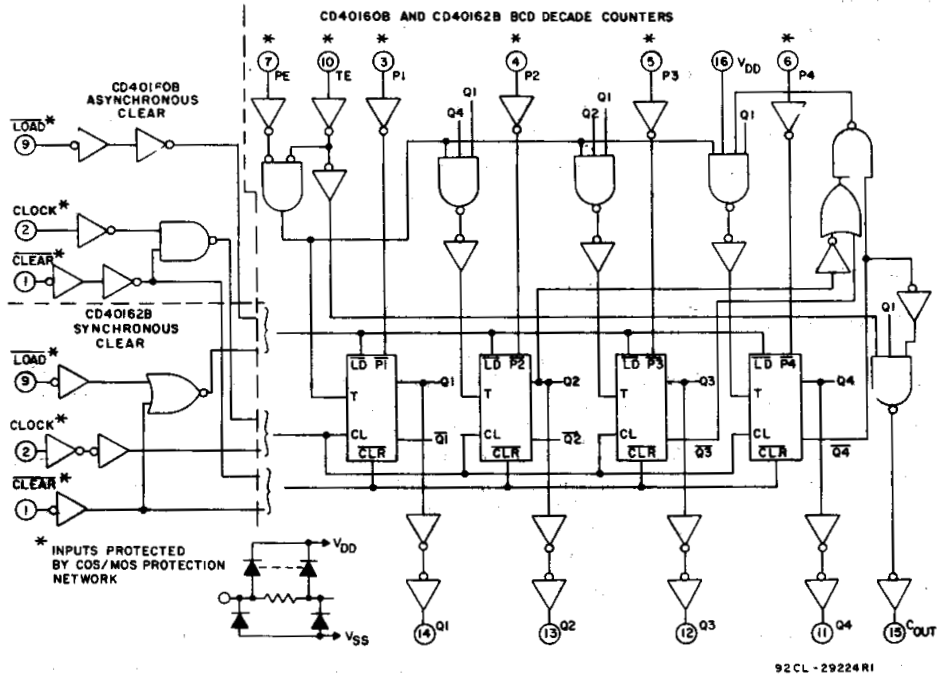


Fig. 3— Logic diagrams for CD40160B and CD40162B BCD decade counters.

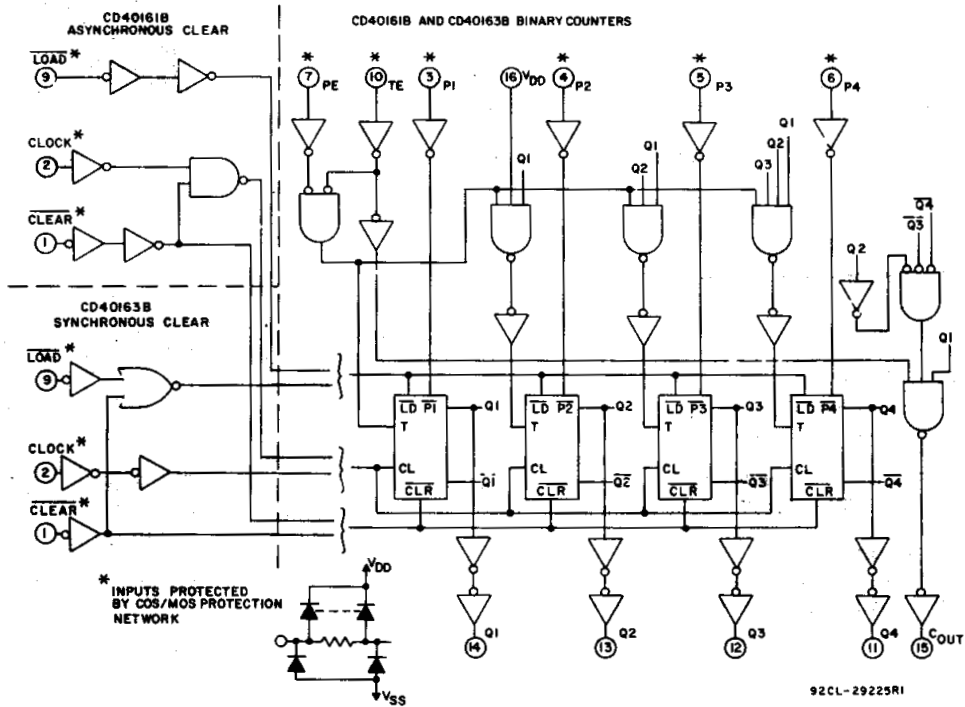


Fig. 4— Logic diagrams for CD40161B and CD40163B binary counters.

CD40160B, CD40161B, CD40162B, CD40163B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | UNITS |
|--------------------------------------------------------------------|-----------------|--------|------|---------------|
| | | MIN. | MAX. | |
| Supply Voltage Range (Full T_A = Full Package-Temperature Range) | — | 3 | 18 | V |
| Setup Time: t_{SU} Data to Clock | 5 | 240 | — | ns |
| | 10 | 90 | — | |
| | 15 | 60 | — | |
| Load to Clock | 5 | 240 | — | ns |
| | 10 | 90 | — | |
| | 15 | 60 | — | |
| PE or TE to Clock | 5 | 340 | — | ns |
| | 10 | 140 | — | |
| | 15 | 100 | — | |
| Clear to Clock (CD40162B, CD40163B) | 5 | 340 | — | ns |
| | 10 | 140 | — | |
| | 15 | 100 | — | |
| All Hold Times, t_H | 5 | 0 | — | ns |
| | 10 | 0 | — | |
| | 15 | 0 | — | |
| Clear Removal Time, t_{rem} (CD40160B, CD40161B) | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 70 | — | |
| Clear Pulse Width, t_{WL} (CD40160B, CD40161B) | 5 | 170 | — | ns |
| | 10 | 70 | — | |
| | 15 | 50 | — | |
| Clock Input Frequency, f_{CL} | 5 | — | 2 | MHz |
| | 10 | — | 5.5 | |
| | 15 | — | 8 | |
| Clock Pulse Width, t_W | 5 | 170 | — | ns |
| | 10 | 70 | — | |
| | 15 | 50 | — | |
| Clock Rise or Fall Time, t_{rCL} or t_{fCL} | 5 | — | 200 | μs |
| | 10 | — | 70 | |
| | 15 | — | 15 | |

TRUTH TABLE

| CLOCK | $\overline{\text{CLR}}$ | $\overline{\text{LOAD}}$ | PE | TE | OPERATION |
|-------|-------------------------|--------------------------|----|----|----------------------------|
| | 1 | 0 | X | X | PRESET |
| | 1 | 1 | 0 | X | NC |
| | 1 | 1 | X | 0 | NC |
| | 1 | 1 | 1 | 1 | COUNT |
| X | 0 | X | X | X | RESET (CD40160B, CD40161B) |
| | 0 | X | X | X | RESET (CD40162B, CD40163B) |
| | 1 | X | X | X | NC (CD40162B, CD40163B) |

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE NC = NO CHANGE

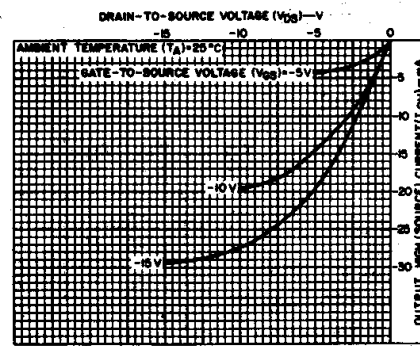


Fig. 5— Typical output high (source) current characteristics.

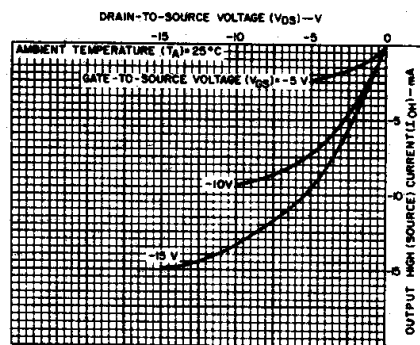


Fig. 6— Minimum output high (source) current characteristics.

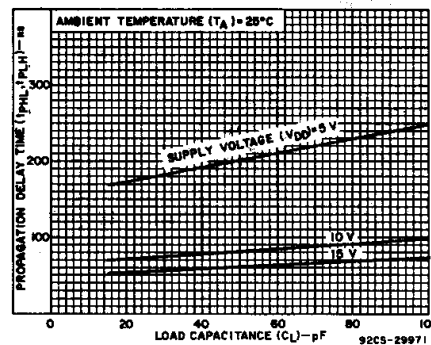


Fig. 7— Typical propagation delay time as a function of load capacitance (CLOCK to Q).

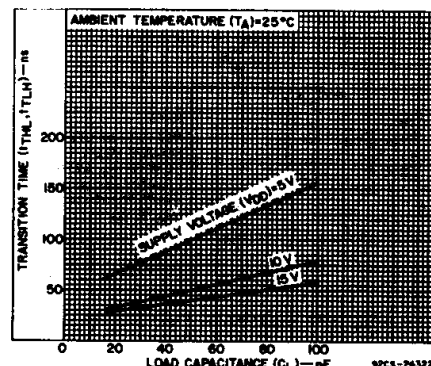


Fig. 8— Typical transition time as a function of load capacitance.

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STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|----------------------------------------------------|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0,04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0,04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0,04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0,08 | 100 | |
| Output Low (Sink) Current, I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | — | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | — | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | — | |
| Output High (Source) Current, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | — | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | — | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | — | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0,5 | 5 | 0,05 | | | | — | 0 | 0,05 | V |
| | — | 0,10 | 10 | 0,05 | | | | — | 0 | 0,05 | |
| | — | 0,15 | 15 | 0,05 | | | | — | 0 | 0,05 | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0,5 | 5 | 4,95 | | | | 4,95 | 5 | — | V |
| | — | 0,10 | 10 | 9,95 | | | | 9,95 | 10 | — | |
| | — | 0,15 | 15 | 14,95 | | | | 14,95 | 15 | — | |
| Input Low Voltage, V _{IL} Max. | 0,5,4,5 | — | 5 | 1,5 | | | | — | — | 1,5 | V |
| | 1,9 | — | 10 | 3 | | | | — | — | 3 | |
| | 1,5,13,5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, V _{IH} Min. | 0,5,4,5 | — | 5 | 3,5 | | | | 3,5 | — | — | V |
| | 1,9 | — | 10 | 7 | | | | 7 | — | — | |
| | 1,5,13,5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current, I _{IN} Max. | — | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0,1 | μA |

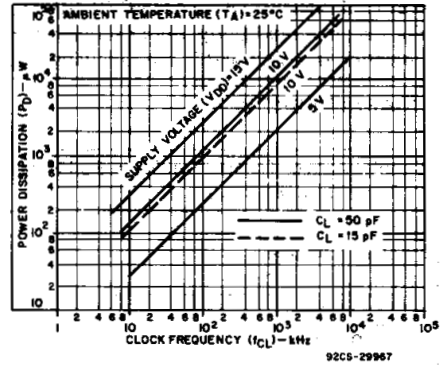


Fig. 9— Typical power dissipation as a function of CLOCK frequency.

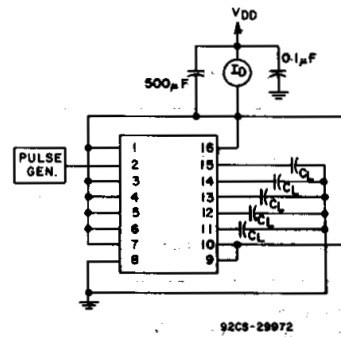


Fig. 10— Dynamic power dissipation test circuit.

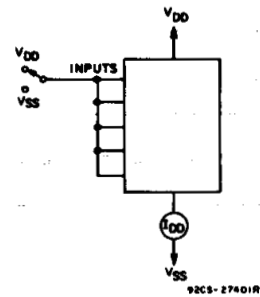


Fig. 11— Quiescent-device-current test circuit.

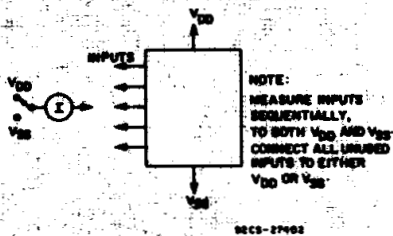


Fig. 12— Input-current test circuit.

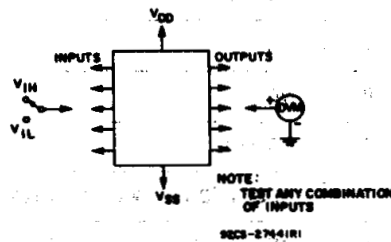


Fig. 13— Input-voltage test circuit.

TERMINAL ASSIGNMENT

| | | | |
|-----------------|---|----|-----------------|
| CLEAR | 1 | 16 | V _{DD} |
| CLOCK | 2 | 15 | CARRY OUT |
| P1 | 3 | 14 | Q1 |
| P2 | 4 | 13 | Q2 |
| P3 | 5 | 12 | Q3 |
| P4 | 6 | 11 | Q4 |
| PE | 7 | 10 | TE |
| V _{SS} | 8 | 9 | LOAD |

TOP VIEW

92CS-29459

CD40160B, CD40161B, CD40162B, CD40163B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$;
 Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS V_{DD} (V) | LIMITS ALL TYPES* | | | UNITS |
|-------------------------------------------------------------------------|---------------------------------|----------------------|------|------|---------------|
| | | Min. | Typ. | Max. | |
| CLOCK OPERATION | | | | | |
| Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Q | 5 | — | 200 | 400 | ns |
| | 10 | — | 80 | 160 | |
| | 15 | — | 60 | 120 | |
| Clock to C_{OUT} | 5 | — | 225 | 450 | ns |
| | 10 | — | 95 | 190 | |
| | 15 | — | 70 | 140 | |
| TE to C_{OUT} | 5 | — | 125 | 250 | ns |
| | 10 | — | 55 | 110 | |
| | 15 | — | 40 | 80 | |
| Minimum Setup Time, t_{SU} Data to Clock | 5 | — | 120 | 240 | ns |
| | 10 | — | 45 | 90 | |
| | 15 | — | 30 | 60 | |
| Load to Clock | 5 | — | 120 | 240 | ns |
| | 10 | — | 45 | 90 | |
| | 15 | — | 30 | 60 | |
| PE to TE to Clock | 5 | — | 170 | 340 | ns |
| | 10 | — | 70 | 140 | |
| | 15 | — | 50 | 100 | |
| Minimum Hold Time, t_H | 5 | — | — | 0 | ns |
| | 10 | — | — | 0 | |
| | 15 | — | — | 0 | |
| Transition Time, t_{THL}, t_{TLH} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Clock Pulse Width, t_W | 5 | — | 85 | 170 | ns |
| | 10 | — | 35 | 70 | |
| | 15 | — | 25 | 50 | |
| Maximum Clock Frequency, f_{CL} | 5 | 2 | 3 | — | MHz |
| | 10 | 5.5 | 8.5 | — | |
| | 15 | 8 | 12 | — | |
| Maximum Clock Rise or Fall Time, † t_{rCL}, t_{fCL} | 5 | 200 | — | — | μs |
| | 10 | 70 | — | — | |
| | 15 | 15 | — | — | |
| CLEAR OPERATION | | | | | |
| Propagation Delay Time, t_{PHL} (CD40160B, CD40161B) Clear to Q | 5 | — | 250 | 500 | ns |
| | 10 | — | 110 | 220 | |
| | 15 | — | 80 | 160 | |
| Minimum Setup Time, t_{SU} (CD40162B, CD40163B) Clear to Clock | 5 | — | 170 | 340 | ns |
| | 10 | — | 70 | 140 | |
| | 15 | — | 50 | 100 | |
| Minimum Hold Time, t_H (CD40162B, CD40163B) Clear to Clock | 5 | — | — | 0 | ns |
| | 10 | — | — | 0 | |
| | 15 | — | — | 0 | |
| Minimum Clear Removal Time, t_{rem} (CD40160B, CD40161B) | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 35 | 70 | |
| Minimum Clear Pulse Width, t_{WL} (CD40160B, CD40161B) | 5 | — | 85 | 170 | ns |
| | 10 | — | 35 | 70 | |
| | 15 | — | 25 | 50 | |

* Except as noted.

† If more than one unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

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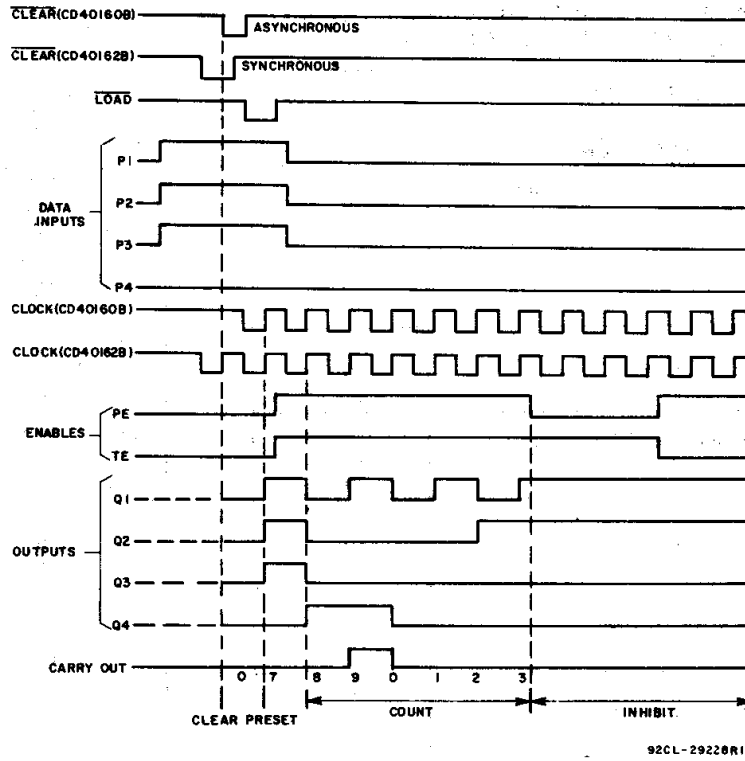


Fig. 14— Timing diagram for CD40160B, CD40162B.

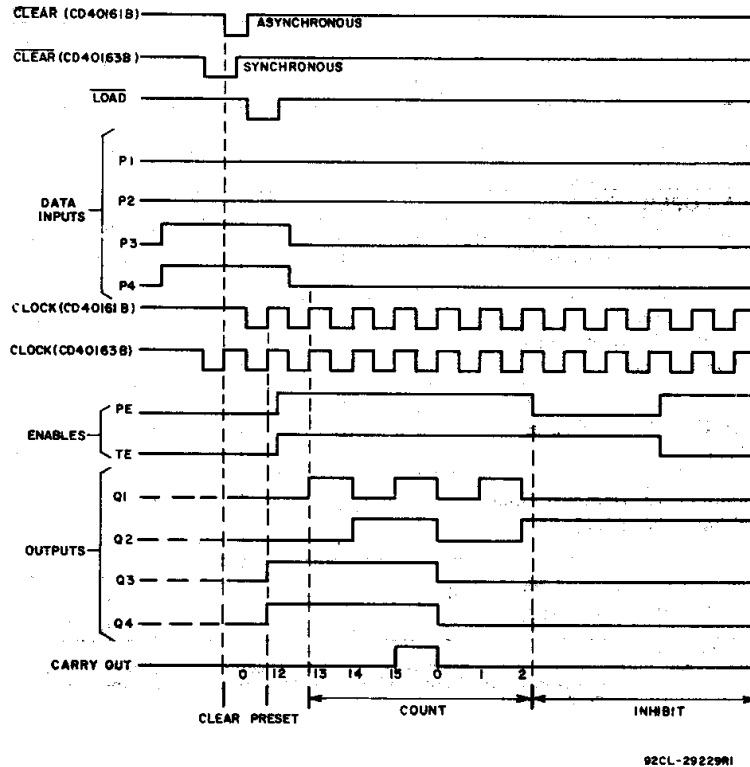


Fig. 15— Timing diagram for CD40161B, CD40163B.

CD40160B, CD40161B, CD40162B, CD40163B Types

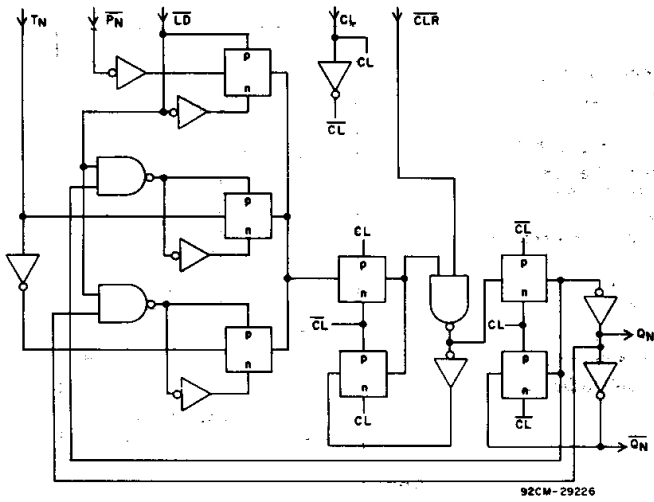


Fig. 16— Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

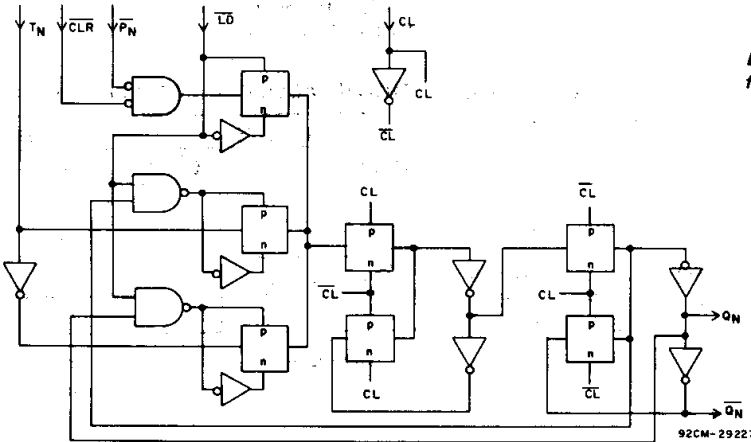
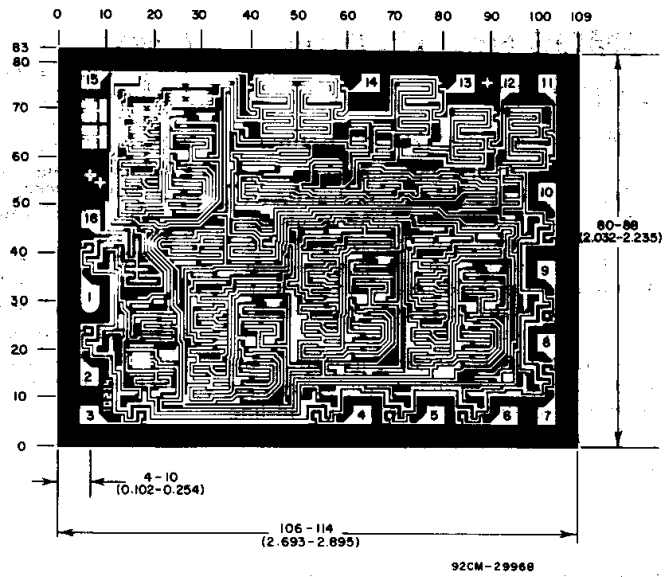


Fig. 17— Detail of flip-flops for CD40162B and CD40163B (synchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

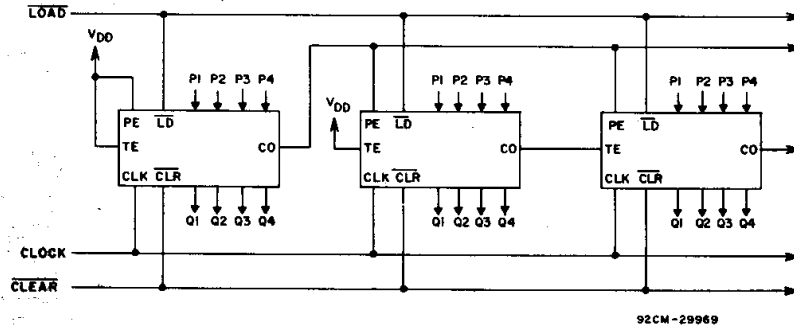


Fig. 18 — Cascaded counter packages in the parallel-clocked mode.

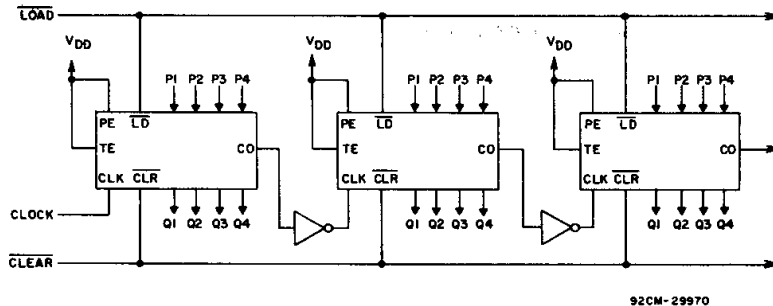


Fig. 19 — Cascaded counter packages in the ripple-clocked mode.

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--------------------------------------------|
| CD40160BF3A | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD40161BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD40161BF3A | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD40161BNSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD40161BPW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD40161BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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