

High Speed CMOS Logic Dual 4-Stage Static Shift Register

Features

- Maximum Frequency, Typically 60MHz
 $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$
- Positive-Edge Clocking
- Overriding Reset
- Buffered Inputs and Outputs
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{V}$

Description

The Harris CD74HC4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent Clock (CP) and Reset (MR) inputs as well as a single serial Data input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

The device can drive up to 10 low power Schottky equivalent loads. The CD74HC4015 is an enhanced version of equivalent CMOS types.

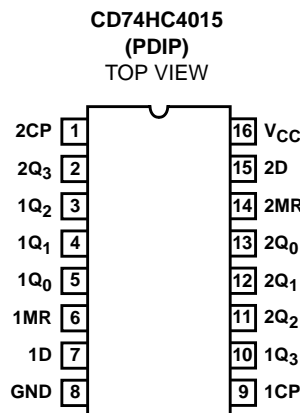
Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ\text{C}$)	PACKAGE	PKG. NO.
CD74HC4015E	-55 to 125	20 Ld PDIP	E16.3

NOTES:

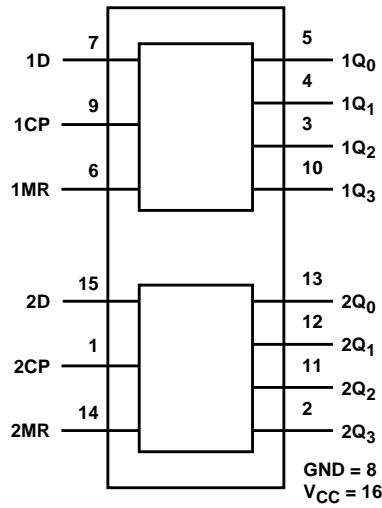
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout



CD74HC4015

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS			
CP	D	R	Q ₀	Q ₁	Q ₂	Q ₃
↑	l	L	L	q' ₀	q' ₁	q' ₂
↑	h	L	H	q' ₀	q' ₁	q' ₂
↓	X	L	q' ₀	q' ₁	q' ₂	q' ₃
X	X	H	L	L	L	L

NOTES:

H = High Voltage Level

h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

X = Don't Care.

↑ = Low to High Clock Transition

↓ = High to Low Clock Transition

q'_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

CD74HC4015

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	100ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			4	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA	

NOTE: For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

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Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f _{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Clock Pulse Width	t _W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
MR Pulse Width	t _W	2	150	-	190	-	225	-	ns
		4.5	30	-	38	-	45	-	ns
		6	26	-	33	-	38	-	ns
MR Recovery Time	t _{REC}	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns
Set-up Time, Data-In to CP	t _{SUL} , t _{SUH}	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time, Data-In to CP	t _H	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay (Figure 1) Clock to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	175	-	220	-	270	ns
			4.5	-	-	35	-	44	-	54	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	30	-	37	-	46	ns
MR to Q _n , (Clock High)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	64	-	83	ns
		C _L = 15pF	-	-	25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	47	-	54	-	71	ns
MR to Q _n , (Clock Low)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	325	-	400	-	490	ns
			4.5	-	-	65	-	81	-	98	ns
		C _L = 15pF	-	-	25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	55	-	69	-	83	ns
Output Transition Time (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f _{MAX}	C _L = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	C _L = 15pF	5	-	43	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per shift register.
5. P_D = V_{CC}² f_i + Σ C_L V_{CC}² where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

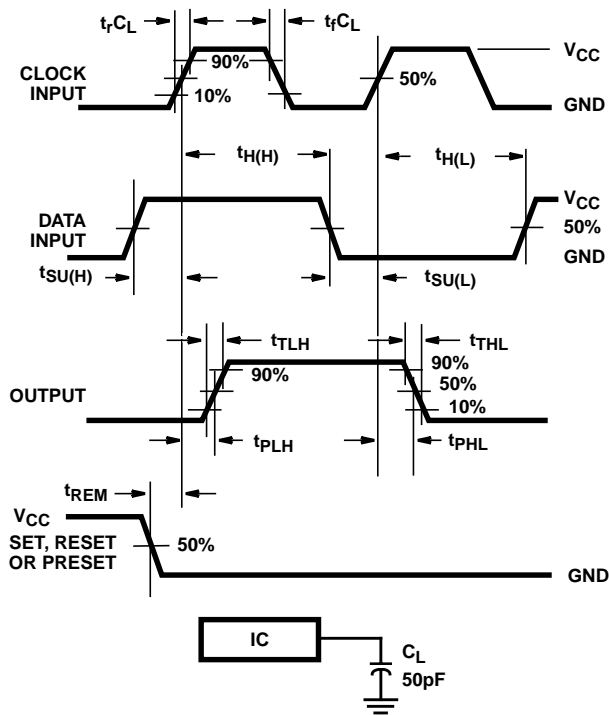


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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