

# CD74HC164, CD74HCT164

## High Speed CMOS Logic 8-Bit Serial-In/Parallel-Out Shift Register

### Features

- Buffered Inputs
- Asynchronous Master Reset
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V (Max)}$ ,  $V_{IH} = 2\text{V (Min)}$
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC164 and the CD74HCT164 are 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset (MR) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

### Ordering Information

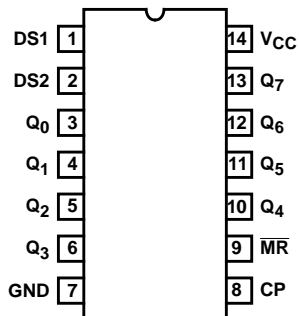
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC164E	-55 to 125	16 Ld PDIP	E14.3
CD74HCT164E	-55 to 125	16 Ld PDIP	E14.3
CD74HC164M	-55 to 125	16 Ld SOIC	M14.15
CD74HCT164M	-55 to 125	16 Ld SOIC	M14.15

#### NOTE:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

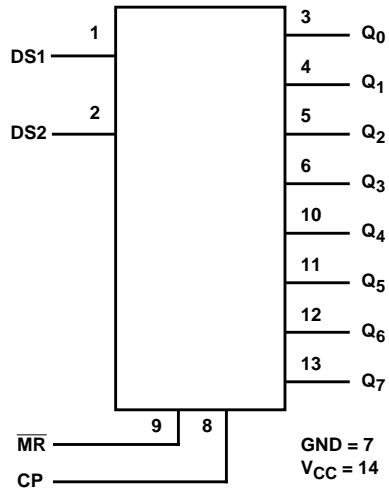
### Pinout

CD74HC164, CD74HCT164  
(PDIP, SOIC)  
TOP VIEW



**CD74HC164, CD74HCT164**

**Functional Diagram**



**TRUTH TABLE**

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q <sub>0</sub>	Q <sub>1</sub> - Q <sub>7</sub>
<b>RESET (CLEAR)</b>	L	X	X	X	L	L - L
Shift	H	↑	l	l	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	l	h	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	h	l	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	h	h	H	q <sub>0</sub> - q <sub>6</sub>

**NOTES:**

H = High Voltage Level.

h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.

l = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.

L = Low Voltage Level.

X = Don't Care.

↑ = Transition from Low to High Level.

q<sub>n</sub> = Lower Case Letters Indicate The State Of the Reference Input Clock Transition.

## CD74HC164, CD74HCT164

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	175
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

## CD74HC164, CD74HCT164

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ to GND	0	5.5	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	$\mu A$
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 3)	$\Delta I_{CC}$	$V_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	$\mu A$

NOTE:

4. For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
Date Shift-In (1, 2)	0.3
$\overline{MR}$	0.9
Clock	0.7

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu A$  max at 25°C.

### Prerequisite For Switching Function

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
Maximum Clock Frequency	$f_{MAX}$	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
$\overline{MR}$ Pulse Width	$t_w$	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns

## CD74HC164, CD74HCT164

### Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
CP Pulse Width	t <sub>w</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time	t <sub>SU</sub>	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time	t <sub>H</sub>	2	4	-	4	-	4	-	ns
		4.5	4	-	4	-	4	-	ns
		6	4	-	4	-	4	-	ns
MR to Clock, Removal Time	t <sub>REM</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
<b>HCT TYPES</b>									
Maximum Clock Frequency	f <sub>MAX</sub>	4.5	27	-	22	-	18	-	MHz
MR Pulse Width	t <sub>w</sub>	6	18	-	23	-	27	-	ns
CP Pulse Width	t <sub>w</sub>	4.5	18	-	23	-	27	-	ns
Set-up Time	t <sub>SU</sub>	6	12	-	15	-	18	-	ns
Hold Time	t <sub>H</sub>	4.5	4	-	4	-	4	-	ns
MR to Clock, Removal Time	t <sub>REM</sub>	6	16	-	20	-	24	-	ns

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, CP to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	170	212	255	ns
			4.5	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	29	36	43	ns
MR to Q <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
		C <sub>L</sub> = 15pF	5	11	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	24	30	36	ns
Output Transition Times	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	75	-	110	ns
			4.5	-	15	-	22	ns
			6	-	13	-	19	ns
Maximum Clock Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 15pF	5	60	-	-	-	MHz
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF

# CD74HC164, CD74HCT164

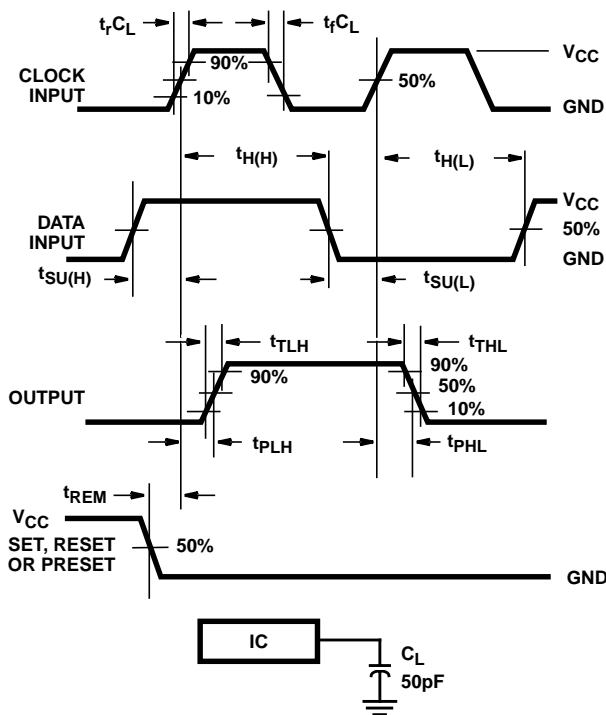
## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	47	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, CP to $Q_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	36	45	54	ns
		$C_L = 15\text{pF}$	5	15	-	-	-	ns
MR to $Q_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	38	46	57	ns
		$C_L = 15\text{pF}$	5	16	-	-	-	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	-	-	-	-	-	-	pF
Maximum Clock Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	-	54	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	49	10	10	10	pF

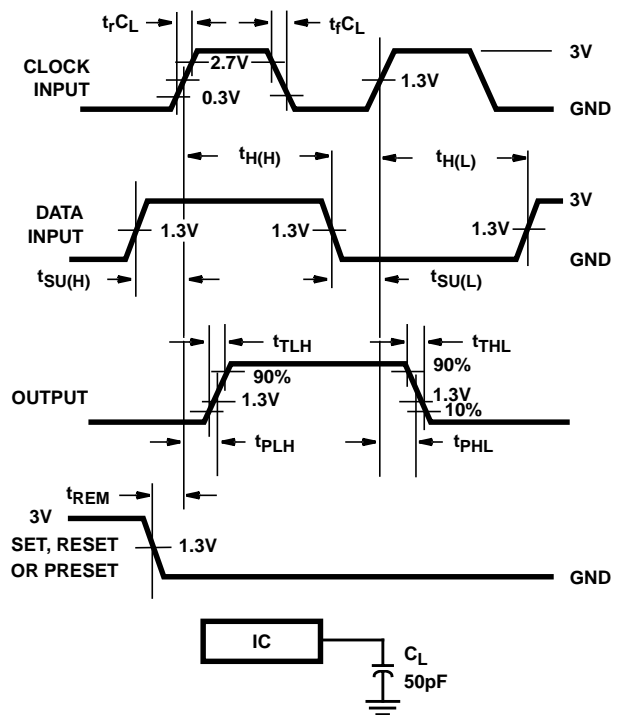
**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per device.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms



**FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**



**FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

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