

CD74HC93, CD74HCT93

High Speed CMOS Logic 4-Bit Binary Ripple Counter

Features

- Can Be Configured to Divide By 2, 8, and 16
- Asynchronous Master Reset
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The Harris CD74HC93 and CD74HCT93 are high speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two-section and a divide-by-eight-section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to innate state changes of the counter on the HIGH to LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2 is provided which overrides both clocks and resets (clears) all flip-flops.

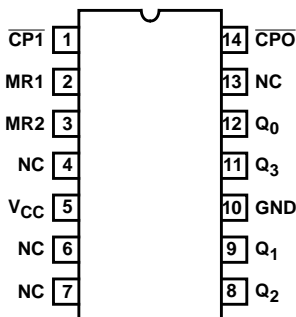
Because the output from the divide by two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

Pinout

CD74HC93, CD74HCT93
(PDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC93E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT93E	-55 to 125	14 Ld PDIP	E14.3
CD74HC93M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT93M	-55 to 125	14 Ld SOIC	M14.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

CD74HC93, CD74HCT93

TRUTH TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: H = High Voltage Level, L = Low Voltage Level

MODE SELECTION

RESET OUTPUTS		OUTPUTS			
MR1	MR2	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	Count	Count	Count	Count
H	L				
L	L				

NOTE: H = High Voltage Level, L = Low Voltage Level

CD74HC93, CD74HCT93

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
SOIC Package	175
Maximum Junction Temperature	$150^{\circ}C$
Maximum Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	$300^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	0.02	6	-	-	0.1	-	0.1	-	0.1	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	0	6	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD74HC93, CD74HCT93

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
CP0, CP1	0.6
MR1, MR2	0.4

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
Maximum Clock Frequency	f _{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
Clock Pulse Width CP0, CP1	t _w	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns

CD74HC93, CD74HCT93

Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Reset Pulse Width	t _W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Reset Removal Time	t _{REM}	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns

HCT TYPES

Maximum Clock Frequency	f _{MAX}	4.5	30	-	24	-	20	-	mHz
Clock Pulse Width CP0, CP1	t _W	4.5	16	-	20	-	24	-	ns
Reset Pulse Width	t _W	4.5	16	-	20	-	24	-	ns
Reset Removal Time	t _{REM}	4.5	10	-	13	-	15	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Time CP0 to Q0	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	125	-	155	-	190	ns
		C _L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C _L = 15pF	5	-	10	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	21	-	26	-	32	ns
CP1 to Q1	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
		C _L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C _L = 50pF	6	-	-	23	-	29	-	35	ns
CP1 to Q2	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	185	-	230	-	280	ns
		C _L = 50pF	4.5	-	-	37	-	46	-	56	ns
		C _L = 50pF	6	-	-	31	-	39	-	48	ns
CP1 to Q3	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	245	-	305	-	370	ns
		C _L = 50pF	4.5	-	-	49	-	61	-	74	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	42	-	52	-	63	ns
MR1, MR2 to Qn	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	155	-	195	-	235	ns
		C _L = 50pF	4.5	-	-	31	-	39	-	47	ns
		C _L = 15pF	5	-	13	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	26	-	33	-	40	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	C _{PD}	-	-	-	25	-	-	10	-	19	pF

CD74HC93, CD74HCT93

Switching Specifications Input t_r , $t_f = 6\text{ ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES											
Propagation Delay Time $\overline{CP0}$ to Q0	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{ pF}$	5	-	14	-	-	-	-	-	ns
$\overline{CP1}$ to Q1	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{ pF}$	5	-	-	-	-	-	-	-	ns
$\overline{CP1}$ to Q2	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$	4.5	-	-	46	-	58	-	69	ns
		$C_L = 15\text{ pF}$	5	-	-	-	-	-	-	-	ns
$\overline{CP1}$ to Q3	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$	4.5	-	-	58	-	73	-	87	ns
		$C_L = 15\text{ pF}$	5	-	24	-	-	-	-	-	ns
MR1, MR2 to Qn	t_{PLH}, t_{PHL}	$C_L = 50\text{ pF}$	4.5	-	-	33	-	41	-	50	ns
		$C_L = 15\text{ pF}$	5	-	13	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{ pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	$C_L = 50\text{ pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	-	-	-	25	-	-	-	-	-	pF

Test Circuits and Waveforms

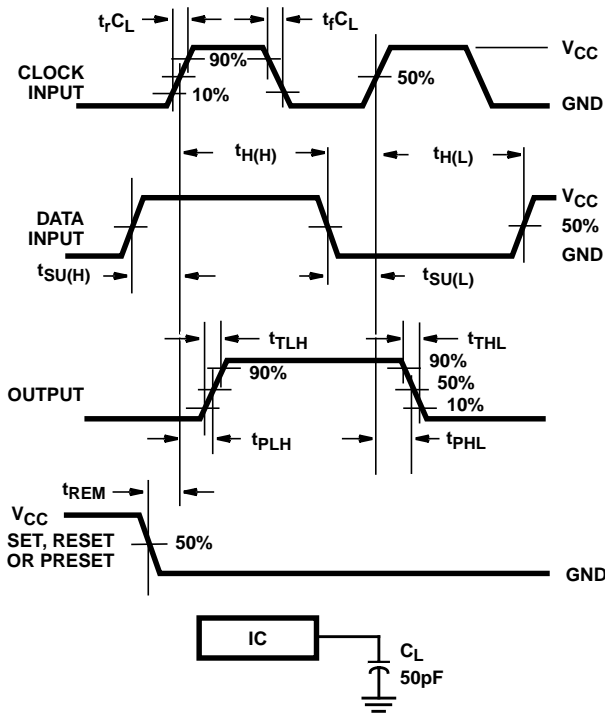


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

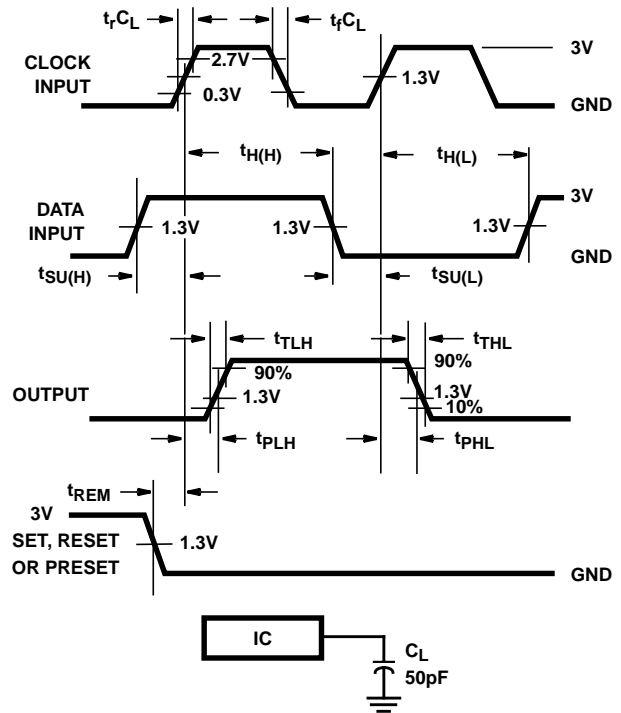


FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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