

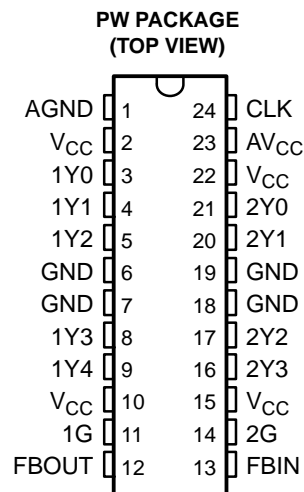
3.3-V PHASE-LOCK LOOP CLOCK DRIVER WITH POWER DOWN MODE

FEATURES

- Designed to Meet and Exceed PC133 SDRAM Registered DIMM Specification Rev. 1.1
- Spread Spectrum Clock Compatible
- Operating Frequency 20 MHz to 175 MHz
- Static Phase Error Distribution at 66 MHz to 166 MHz Is ± 125 ps
- Jitter (cyc - cyc) at 66 MHz to 166 MHz Is $|70|$ ps
- Advanced Deep Submicron Process Results in More Than 40% Lower Power Consumption Versus Current Generation PC133 Devices
- Auto Frequency Detection to Disable Device (Power-Down Mode)
- Available in Plastic 24-Pin TSSOP
- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs
- Separate Output Enable for Each Output Bank
- External Feedback (FBIN) Terminal Is Used to Synchronize the Outputs to the Clock Input
- 25- Ω On-Chip Series Damping Resistors
- No External RC Network Required
- Operates at 3.3 V

FEATURES

- DRAM Applications
- PLL Based Clock Distributors
- Non-PLL Clock Buffer



DESCRIPTION

The CDCVF2509A is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDCVF2509A operates at a 3.3-V V_{CC}. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK. Each bank of outputs is enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state. The device automatically goes into power-down mode when no input signal (< 1 MHz) is applied to CLK; the outputs go into a low state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Unlike many products containing PLLs, the CDCVF2509A does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDCVF2509A requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed by strapping AV_{CC} to ground to use as a simple clock buffer.

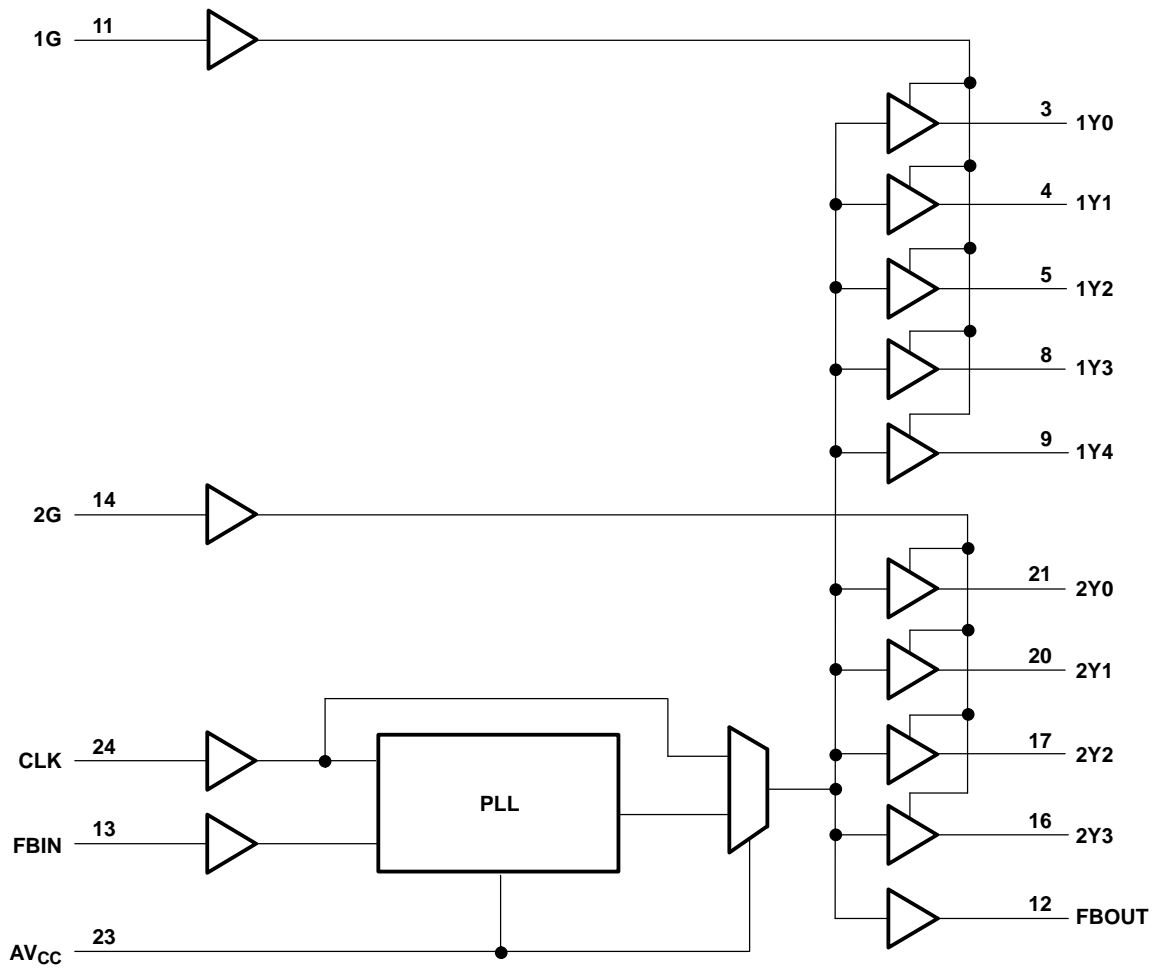
The CDCVF2509A is characterized for operation from 0°C to 85°C.

For application information, see application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (SLMA003) and *Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC)* (SCAA039).

FUNCTION TABLE

Inputs			Outputs		PLL
AVDD	1G/2G	CLK	1Y/2Y	FBOUT	
GND	H	L	L	L	Bypassed / Off
GND	H	H	H	H	Bypassed / Off
GND	L	L	L	L	Bypassed / Off
GND	L	H	L	H	Bypassed / Off
GND	L	Toggling	L	Toggling in phase to CLK	Bypassed / Off
3.3 V (nom)	L	H	L	L	On
3.3 V (nom)	L	Toggling	L	Toggling in phase to CLK	On
3.3 V (nom)	H	L	L	L	On
3.3 V (nom)	H	H	H	H	On
3.3 V (nom)	H	Toggling	Toggling in phase to CLK	Toggling in phase to CLK	On
3.3 V (nom)	X	< 1 MHz	L	L	Off

FUNCTIONAL BLOCK DIAGRAM



AVAILABLE OPTIONS

T _A	PACKAGE
	0°C to 85°C
CDCVF2509APWR	
CDCVF2509APW	

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDCVF2509A clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25- Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25- Ω series-damping resistor.
2Y (0:3)	16, 17, 21, 20	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25- Ω series-damping resistor.
AV _{CC}	23	Power	Analog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL. When AV _{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V _{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	UNIT
AV _{CC} Supply voltage range ⁽²⁾	AV _{CC} < V _{CC} + 0.7 V
V _{CC} Supply voltage range	–0.5 V to 4.3 V
V _I Input voltage range ⁽³⁾	–0.5 V to 4.6 V
V _O Voltage range applied to any output in the high or low state ⁽³⁾⁽⁴⁾	–0.5 V to V _{CC} + 0.5 V
I _{IK} Input clamp current (V _I < 0)	–50 mA
I _{OK} Output clamp current (V _O < 0 or V _O > V _{CC})	±50 mA
I _O Continuous output current (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) ⁽⁵⁾	0.7 W
T _{stg} Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) AV_{CC} **must not** exceed V_{CC} + 0.7 V

(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 4.6 V maximum.

(5) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, see the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book* (SCBD002).

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC} , AV _{CC}	Supply voltage	3	3.6	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
I _{OH}	High-level output current		-12	mA
I _{OL}	Low-level output current		12	mA
T _A	Operating free-air temperature	0	85	°C

(1) Unused inputs must be held high or low to prevent them from floating.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f _{clk}	Clock frequency	20	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time ⁽¹⁾		1	ms

(1) The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew and jitter parameters given in the *switching characteristics* table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} , AV _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA	3 V		-1.2	V
V _{OH}	High-level output voltage	I _{OH} = -100 µA	MIN to MAX		V _{CC} -0.2	V
		I _{OH} = -12 mA	3 V		2.1	
		I _{OH} = -6 mA	3 V		2.4	
V _{OL}	Low-level output voltage	I _{OL} = 100 µA	MIN to MAX		0.2	V
		I _{OL} = 12 mA	3 V		0.8	
		I _{OL} = 6 mA	3 V		0.55	
I _{OH}	High-level output current	V _O = 1 V	3 V		-28	mA
		V _O = 1.65 V	3.3 V		-36	
		V _O = 3.135 V	3.6 V		-8	
I _{OL}	Low-level output current	V _O = 1.95 V	3 V		30	mA
		V _O = 1.65 V	3.3 V		40	
		V _O = 0.4 V	3.6 V		10	
I _I	Input current	V _I = V _{CC} or GND	3.6 V		±5	µA
I _{CC} ⁽²⁾	Supply current (static, output not switching)	V _I = V _{CC} or GND, I _O = 0, Outputs: low or high	3.6 V, 0 V		40	µA
ΔI _{CC}	Change in supply current	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3.3 V to 3.6 V		500	µA
C _i	Input capacitance	V _I = V _{CC} or GND	3.3 V		2.5	pF
C _o	Output capacitance	V _O = V _{CC} or GND	3.3 V		2.8	pF

(1) For conditions shown as MIN or MAX, use the appropriate value specified under the *recommended operating conditions* section.

(2) For dynamic I_{CC} vs Frequency, see Figure 8 and Figure 9.

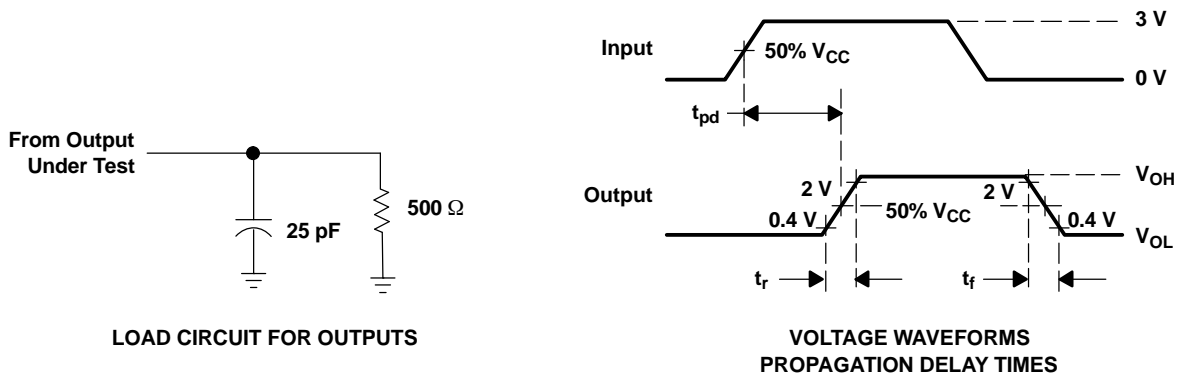
SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature, $C_L = 25 \text{ pF}$ (see Figure 1 and Figure 2)⁽¹⁾⁽²⁾

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}, AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			UNIT
			MIN	TYP	MAX	
Phase error time- static (normalized) (see Figure 3 through Figure 6)	$CLK \uparrow = 66 \text{ MHz to } 166 \text{ MHz}$	$FBIN \uparrow$	-125		125	ps
$t_{sk(o)}$ Output skew time ⁽³⁾	Any Y	Any Y			100	ps
Phase error time-jitter ⁽⁴⁾	$CLK = 66 \text{ MHz to } 100 \text{ MHz}$	Any Y or FBOUT	-50		50	ps
Jitter _(cycle-cycle) (see Figure 7)		Any Y or FBOUT		70		
	$CLK = 100 \text{ MHz to } 166 \text{ MHz}$	Any Y or FBOUT			65	
Duty cycle	$f_{(CLK)} > 60 \text{ MHz}$	Any Y or FBOUT	45%		55%	
t_r Rise time	$V_O = 0.4 \text{ V to } 2 \text{ V}$	Any Y or FBOUT	0.3		1.1	ns/V
t_f Fall time	$V_O = 2 \text{ V to } 0.4 \text{ V}$	Any Y or FBOUT	0.3		1.1	ns/V
t_{PLH} Low-to-high propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns
t_{PHL} High-to-low propagation delay time, bypass mode	CLK	Any Y or FBOUT	1.8		3.9	ns

- (1) The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
- (2) These parameters are not production tested.
- (3) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
- (4) Calculated per PC DRAM SPEC ($t_{\text{phase error, static-jitter}}_{\text{(cycle-to-cycle)}}$).

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 133 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 1.2 \text{ ns}$, $t_f \leq 1.2 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

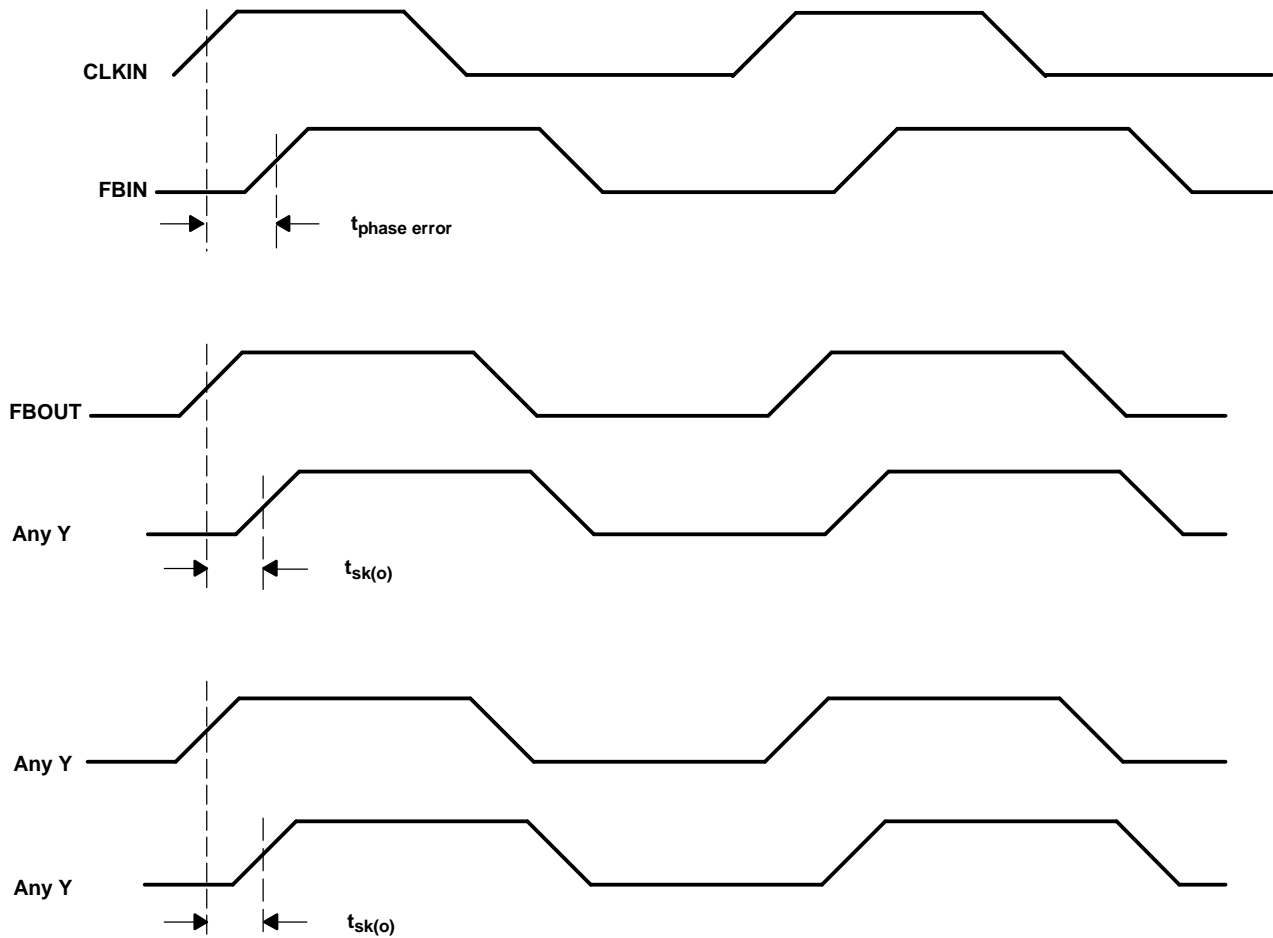


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

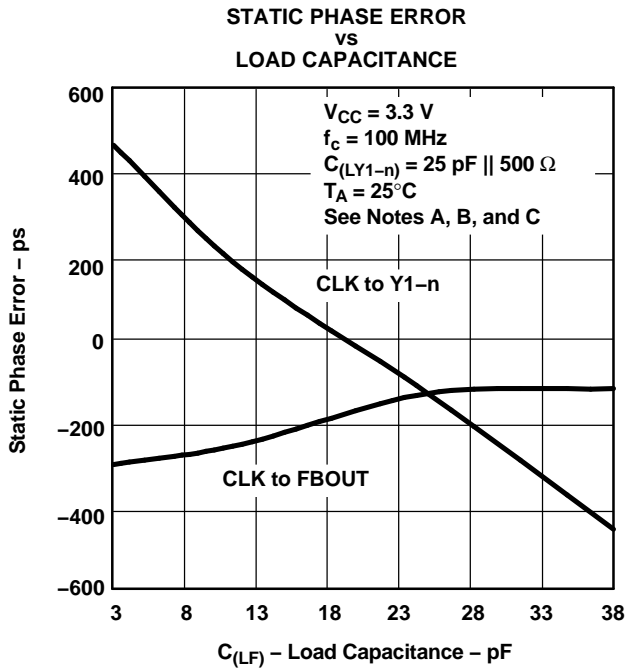


Figure 3.

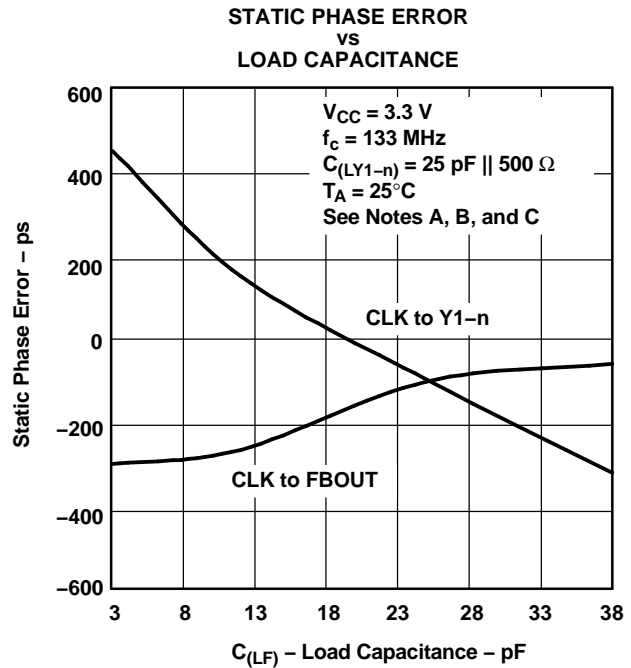


Figure 4.

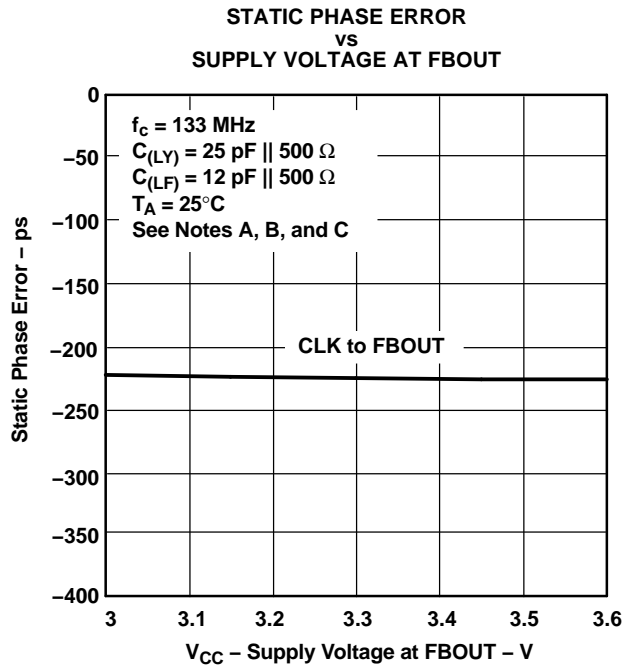


Figure 5.

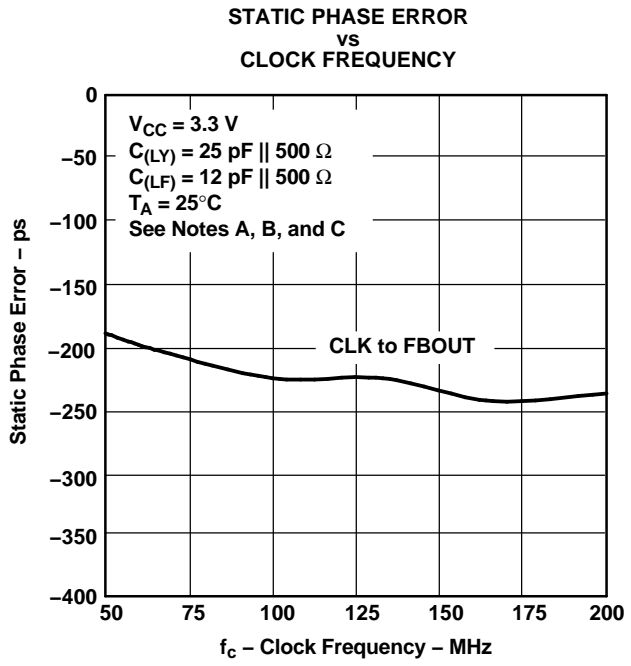


Figure 6.

- A. Trace length FBOUT to FBIN = 5 mm, $Z_0 = 50\Omega$
- B. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}
- C. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN

TYPICAL CHARACTERISTICS (continued)

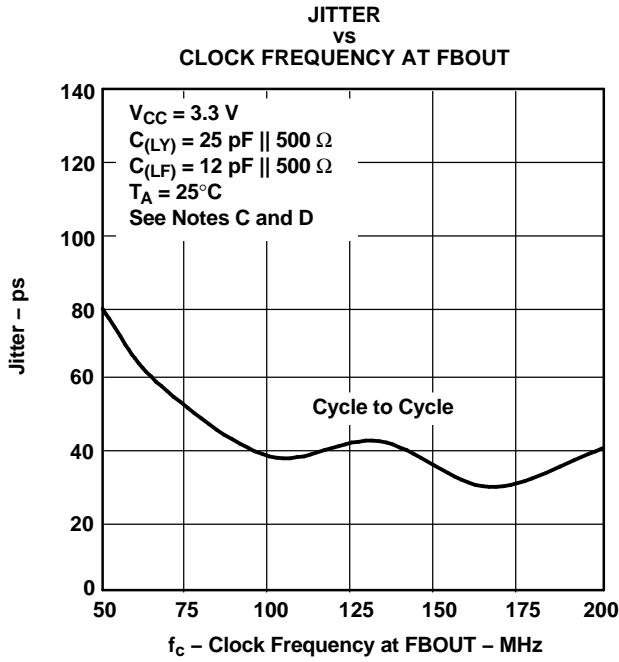


Figure 7.

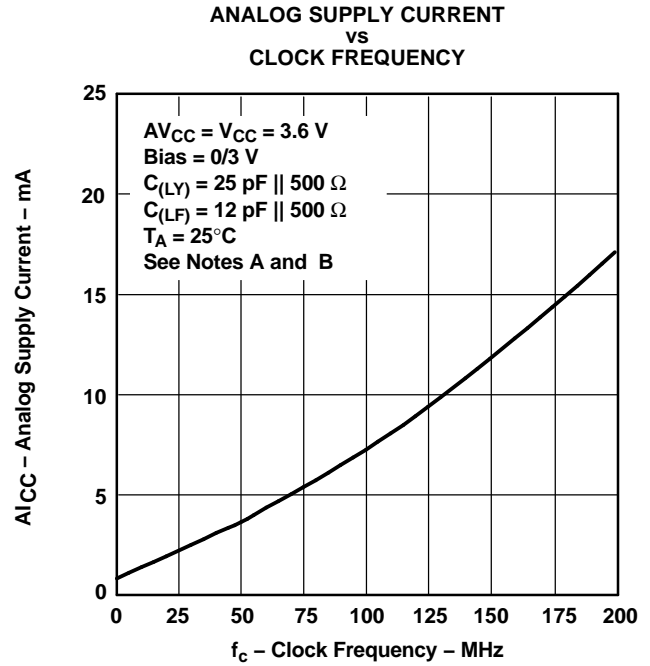


Figure 8.

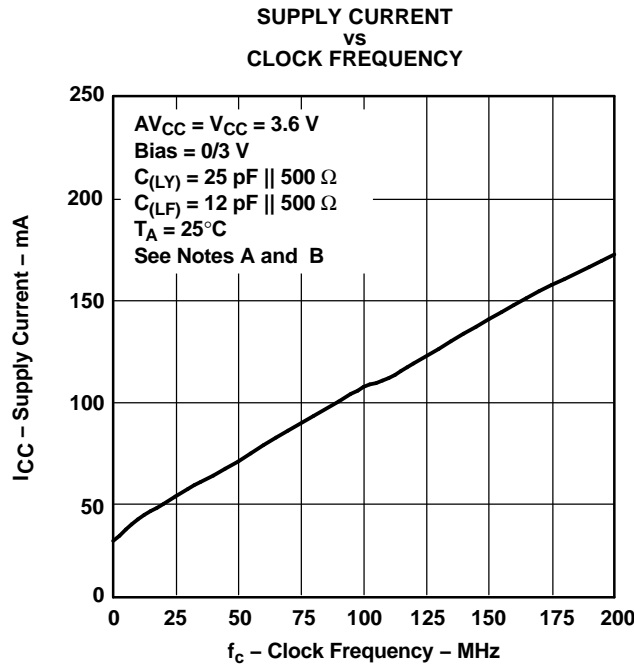


Figure 9.

- A. Trace length FBOUT to FBIN = 5 mm, $Z_0 = 50\Omega$
- B. $C_{(LY)}$ = Lumped capacitive load Y_{1-n}
- C. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN
- D. $C_{(LFx)}$ = Lumped feedback capacitance at FBOUT = FBIN.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCVF2509APW	ACTIVE	TSSOP	PW	24	60	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCVF2509APWR	ACTIVE	TSSOP	PW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

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Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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